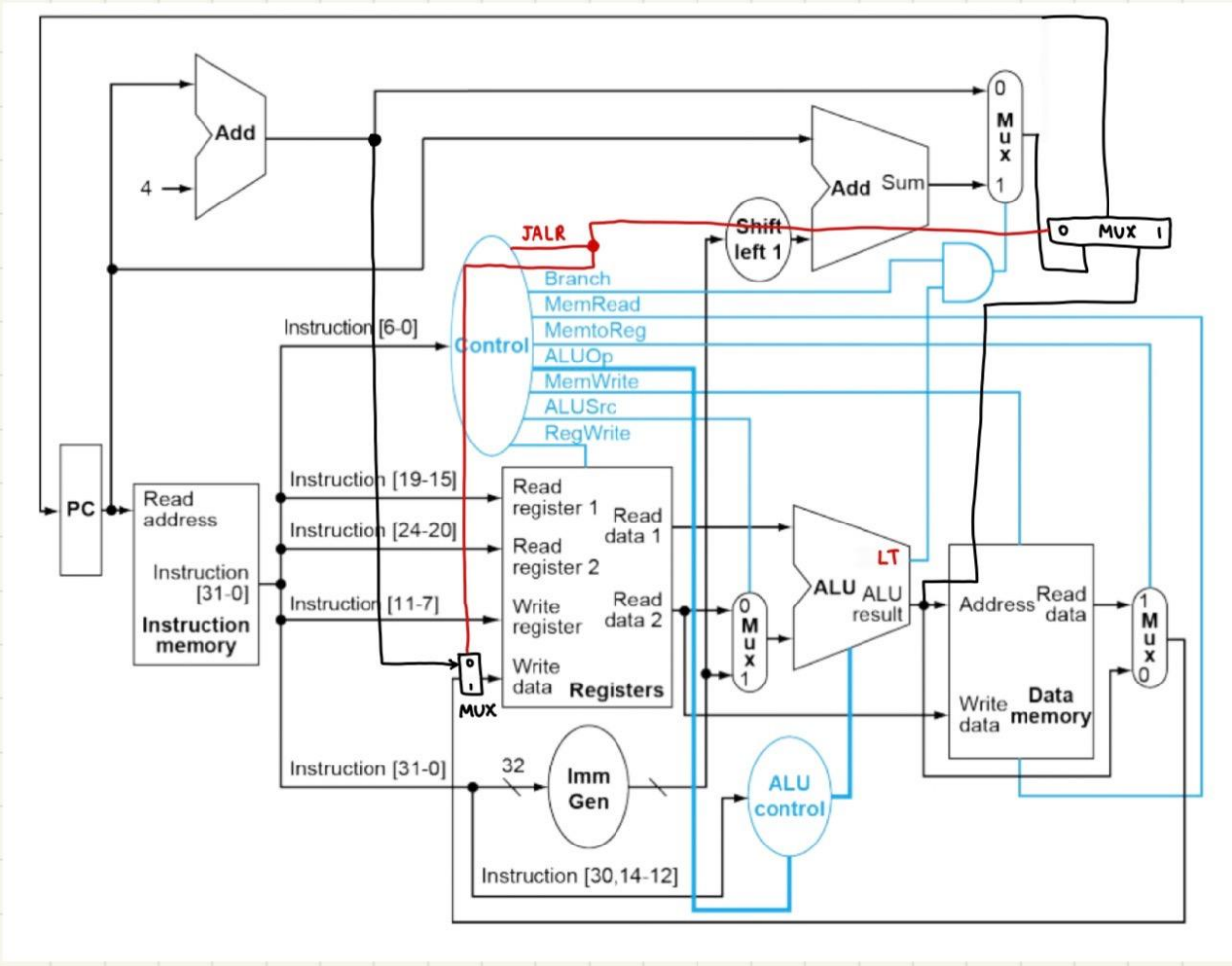
1. There are 13 cycles for the “all” trace – 12 non-ZERO instructions, and 1 ZERO instruction.
2. The “all” program has 2 R-type instructions. If the first BLT (PC = 0x0c) were taken, the program would only execute the first of these instructions. But the branch condition wasn’t satisfied, so the second R-type instruction was executed.
3. Since this is a single-cycle processor, CPI = 1, and thus IPC = 1.

This is my design of the controller and datapath:



In my implementation, I encapsulated the control codes with an enum of instructions called Op, whose values include ADD, SRA, BLT, NONE, etc. Through the use of various if-statements, I implemented the MUXes that select between two inputs. Although I didn't explicitly use control codes, the general idea I had was as follows:

Instruction	Opcode	Branch	Link	Mem Read	Mem Write	Memto Reg	RegWrite	ALUSrc	ALUOp
ADD	0110011	0	0	0	0	0	1	0	0001
SUB	0110011	0	0	0	0	0	1	0	0010
ADDI	0010011	0	0	0	0	0	1	1	0001
XOR	0110011	0	0	0	0	0	1	0	0011
ANDI	0010011	0	0	0	0	0	1	1	0100
SRA	0110011	0	0	0	0	0	1	0	0101
LW	0000011	0	0	1	0	1	1	1	0001
SW	0100011	0	0	0	1	0	0	1	0001
BLT	1100011	1	0	0	0	0	0	0	0010
JALR	1100111	0	1	0	0	0	1	1	0001