6.5900 Self-Assessment Test
RV32I Handout

http://csg.csail.mit.edu/6.5900/

Here is a brief summary of the RISC-V instructions used in the self-assessment test. The self assessment test uses the RV32I variant. There are 31 32-bit general-purpose registers (x1 to x31), and register x0 is hardwired to 0. Memory is byte-addressible, and a word in memory is defined to be 32-bit wide.

Instruction	Syntax	Description	Execution
ADD	`add rd, rs1, rs2`	Add	`reg[rd] <= reg[rs1] + reg[rs2]`
ADDI	`addi rd, rs1, constant`	Add Immediate	`reg[rd] <= reg[rs1] + constant`
SUB	`sub rd, rs1, rs2`	Subtract	`reg[rd] <= reg[rs1] - reg[rs2]`
LW	`lw rd, offset(rs1)`	Load Word	`reg[rd] <= mem[addr + 3: addr]`
SW	`sw rs2, offset(rs1)`	Store Word	`mem[addr + 3: addr] <= reg[rs2]`
BEQ	`beq rs1, rs2, label`	Branch if =	`pc <= (reg[rs1] == reg[rs2]) ? label: pc + 4`
BNE	`bne rs1, rs2, label`	Branch if ≠	`pc <= (reg[rs1] != reg[rs2]) ? label: pc + 4`

Note:

- *offset* and *constant* are signed 12-bit values that are sign-extended to 32-bit values
- *label* is a 32-bit memory address or its alias name
- *addr* is a load/store address as calculated by `reg[rs1] + offset`