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Senior Memory Layout Engineer 8882203862 | New Delhi, India

Professional Summary:

8 years of experience as a Memory Layout designer in ST Microelectronics (Subcontractor through Zia Semiconductor Pvt Ltd).

- Experience in Planning and development of layout activities (including time and resource allocation).
- Professional experience in development of layout of basic leaf cells in FDSOI 28nm, 40nm, 65nm and 90nm technologies.
- Basic Layout training in FINFET 7nm and FDSOI 14nm.
- Experience in Development of Custom Cuts and Compiler products along with verifications like DRC/LVS, DFMs such as LFD, OPC, VRC and other top-level checks like Abstract checks, Library checks, etc. needed in QA before final delivery.
- Experience in Delivery of test chip cuts, Prelim/Final LEF and Compiler Products.

HIGHLIGHTS

1. Excellent in leaf cell layout development of I/O and ROWDECODER.
2. Hands on experience in compiler development from scratch to delivery.
3. Very Good understanding of EM/IR issues and their corrections.
4. Good knowledge of layout effects like WPE, STI, LOD, Latch up and Antenna effect.
5. Understanding of different types of Memory architecture and floor planning.
6. Good Understanding of schematics and netlists.

TECHNICAL Skills

• Layout Design	Cadence Virtuoso, ICFB and Synopsys Custom Compiler
• Verification (DRC/LVS)	Mentor graphics - Calibre
• Top-level Verifications	Crossfire Tool, ADOC tool
• Scripting Knowledge	Unix, Shell and Cadence Virtuoso skill
• Extraction	Star_rcxt
• EM/IR simulation	Customsim

SOFT Skills

- Successfully managed a project leading a team of 5 and delivered it on time.
- Regularly Communicating with code and standard cell team for activities like programming cells and debugging cut development/generation.
- Actively provide guidance and support to juniors.

Professional experience in SRAM Memory Layouts:

Techno Node: 28nm FDSOI (STM Process)

Types of Compilers: SPHD, SPHS, DPHD, PRF2HD with HP, BB and LL variants.

- **Projects:**
  - Implementing HV marker for both GEONEXT and SAMSUNG compilers supporting Body bias up to 1.1V.
  - SPHD mux 8 cut development from SPHS compiler (bit cell change).
  - Implementing SCAN-CHAIN in PRF2HD compiler in both IO and CTRL blocks.
  - SPHS compiler development from scratch.
  - Feature addition and Design changes in PRF2HD, SPHDULV compilers.
  - Bugfix and Implementation of Retention in SPL1_CACHE compiler.
  - DRC/DFM updates in multiple compilers.

- **Responsibilities:**
  - Planning and overlooking all layout activities in last project leading a team of 5
  - Development of LIO blocks in multiple compilers
  - Development of ROWDECODER, Dummy Row dec and Redundancy Row dec.
  - Development of DCOL block and ARRAY power cells.
  - Design changes and updates in CTRL block.
  - Provide Extraction of Leaf cells.
  - EM and IR improvements.
  - Final verifications (compiler level DRC/LVS/DFMs).
  - Prelim, test chip and Final product delivery.

- **Challenges:**
  - Understanding different type of flavors in compilers like HP, BB and LL in flip well/traditional well with LVT, SVT and HVT layers. Performing verifications.
  - Cut development from scratch and its LVS.
  - Cut list improvement in SPHS compiler to cover all possible range and parameters.
  - Placement and routing of IO block in reduced width since SPHD bit cell is used inside SPHS architecture. Critical nodes matching and signal shielding.

Techno Node: 40nm (STM process)

- **Projects:**
  - Porting of SPHS compiler to SPHSHD compiler.
  - CMOSM40 SPHD_ULV compiler development from scratch.
  - Design changes and DRC/DFM updates in multiple compilers.

- **Responsibilities:**
  - Development of GIO and GCTRL blocks.
  - Development of Redundancy ROWDEC and Retention block.
  - Management of Power cells in DCOL and Core array.
  - EM and IR improvements.
  - Final verifications (compiler level DRC/LVS/DFMs).
  - Prelim, test chip and Final product delivery.

- **Challenges:**
  - Regular and DFM improved layout with poly alignment across different blocks.

Techno Nodes: 65nm, 90nm (STM process)

- **Projects:**
  - Latch up corrections in DPHD 65nm.
  - Compiler development in BCD9S.
  - DRC/DFM updates in multiple compilers.
- **Responsibilities:**
  - Strap insertion in CTRL, I/O and Bit cell array for DPHD 65nm.
  - Development of I/O block in 90nm.
  - Top level verifications and Product delivery.
- **Challenges:**
  - LVS issues in bit cell array.
  - First Project delivery experience.

Techno node: 7nm FinFet (Samsung aligned process) and 14nm FDSOI (STM process).

Zia Semiconductor internal projects for training.

- Knowledge of critical DRCs of base layers and metal layers.
- Leaf cell Layout development of Mux4 IO in 7nm and ROWDEC in 14nm.
- Understanding of dual patterning and associated metal DRCs.

Academic Qualifications:

Education	UNIVERSITY/ BOARD	Year of Passing	Percentage
BTech (E&C)	JMI	2012	**7.57 (CPI)**
XII Standard	ISC Board	2008	**86.83%**
X Standard	ICSE Board	2006	**84.5%**