DESIGN SPEC DOCUMENT

ECE-593: Fundamentals of Pre-Silicon Validation
Maseeh College of Engineering and Computer Science
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Project Name: Verification of AXI4-Lite Slave Interface

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Project Name	Verification of AXI4-Lite Slave Interface
Location	Portland, OR
Start Date	April 15, 2025
Estimated Finish Date	May 25, 2025
Completed Date	May 22, 2025

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Design Features:

AXI4-Lite Protocol Compliance

- Implements all 5 AXI4-Lite channels (AW, W, B, AR, R)
- Follows ARM AXI4-Lite specification

Configurable Widths

- Address width = 4 bits
- Data width = 32 bits

Register File

- 4 internal registers
- Each 32-bit wide
- Addressable via top 2 bits of 4-bit address

Byte-Wise Write Support

- Uses 4-bit WSTRB for selective byte access
- Supports partial writes to registers

Handshake Protocol

- Valid/Ready signaling for all channels
- Ensures safe transaction completion

Memory-Mapped Access

- Registers appear as memory space
- Enables integration with software/CPU

Synchronous Design

- Clocked via ACLK
- Reset via ARESETn (active-low)

Project Description:

This project implements and verifies a memory-mapped AXI4-Lite Slave Interface that allows a master to interact with internal registers via read/write transactions. Byte-wise updates are supported via WSTRB. The design was verified through both class-based and UVM-based SystemVerilog environments, including scoreboard-based checking, functional coverage, and concurrent access tests using two independent agents.

Important Signals/Flags

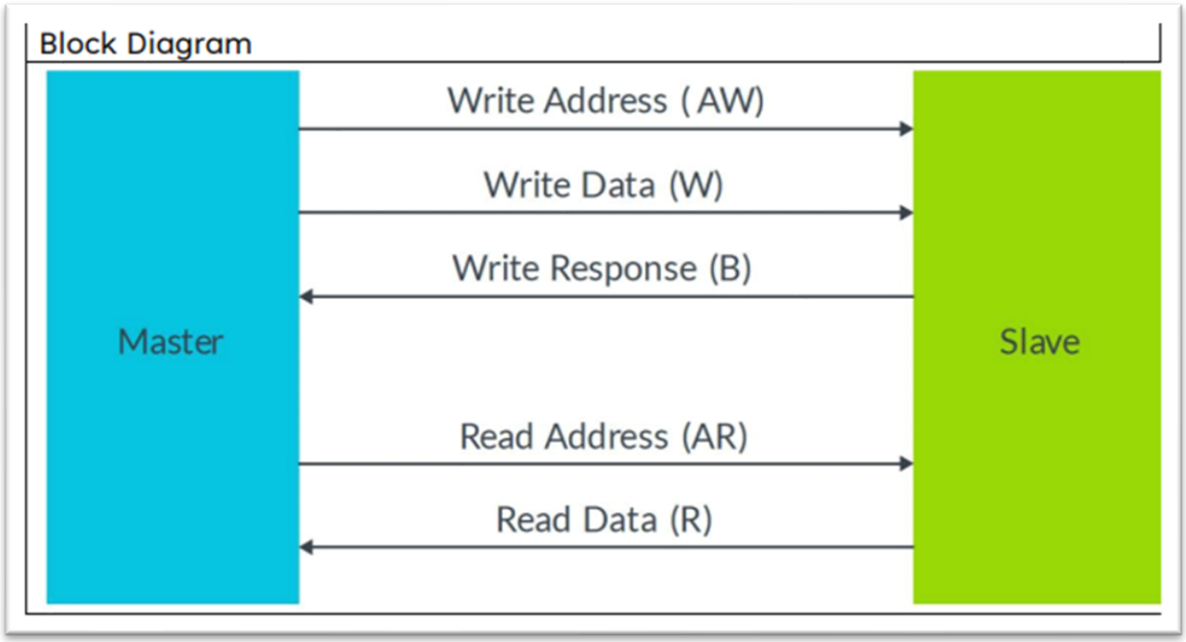
- ACLK: System clock
- ARESETn: Active-low reset
- AWADDR / AWVALID / AWREADY: Write address
- WDATA / WSTRB / WVALID / WREADY: Write data
- BVALID / BREADY: Write response
- ARADDR / ARVALID / ARREADY: Read address
- RDATA / RVALID / RREADY: Read data

Design Signals

- parameter ADDR_WIDTH = 4
- parameter DATA_WIDTH = 32
- input logic ACLK
- input logic ARESETn
- input logic [3:0] AWADDR, ARADDR
- input logic [31:0] WDATA
- input logic [3:0] WSTRB
- output logic [31:0] RDATA

- Valid/ready signals for all 5 AXI4-Lite channels

Block Diagram



References/Citations

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