regfile.v :- [Register file]

→ has option to reset all registers to zero
→ register 0 is hardcoded to zero.
→ write enable is single bit.

control.v : [control unit]

input : instruction [31:0]

outputs : → alusrc [1:0] :- decides whether immediate generate is used or not and higher bit denotes position of immediate reg.

→ memtoreg
decides whether dmem output or alu output should be used as indata for register file

→ regwrite
write enable for regfile

→ memwrite [3:0]
write enable for dmem

→ branch
high if it's a branch type instr.

→ aluop [1:0]
0 0 → ld/sw
0 1 → b type
1 0 → R-type
1 1 → ALU not used

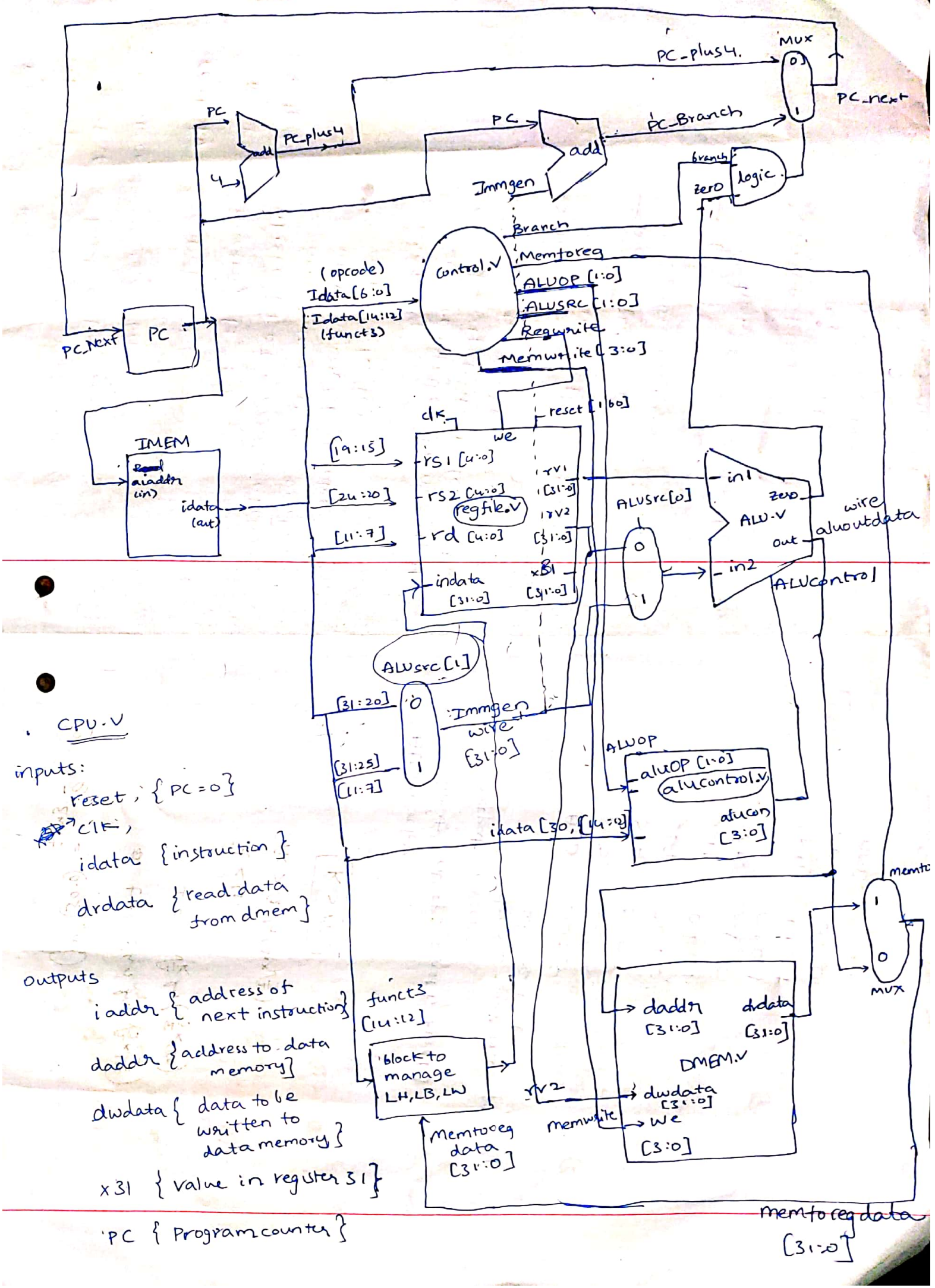
ALUControl.v

input ALUop, funct7, funct3

output ALUcon:

decides what ALU operation will be used

ADD	0000
SUB	1000
SLL	0001
SLT	0010
SLTU	0011
XOR	0100
SRL	0101
SRA	1101
OR	0110
AND	0111



CPU.V

inputs:

reset, { PC = 0 }

clk,

idata { instruction }

drdata { read data from dmem }

outputs

iaddr { address of next instruction }

daddr { address to data memory }

dwdata { data to be written to data memory }

x31 { value in register 31 }

PC { Program counter }