



# Mini Project Presentation

## UVM based Verification & Physical Design of APB Bridge

*by*

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VLSI Design

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VLSI Design

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# Presentation Outline

1. Introduction
2. Objectives
3. Block Diagram
4. FSM
5. Work done/Results
6. Conclusion
7. References



# 1. Introduction

- Advanced Peripheral Bus (APB) - Connects peripheral devices to a CPU in embedded systems.
- Highly configurable and allow multiple devices on a single bus.
- Compatible with other bus-based protocols.
- Widespread use highlights its value in electronics and computing.



## 2. Objectives

1. To verify RTL design code associated with APB bridge using Universal Verification Methodology.
2. To obtain Physical Design of APB bridge.

# 3. Block Diagram

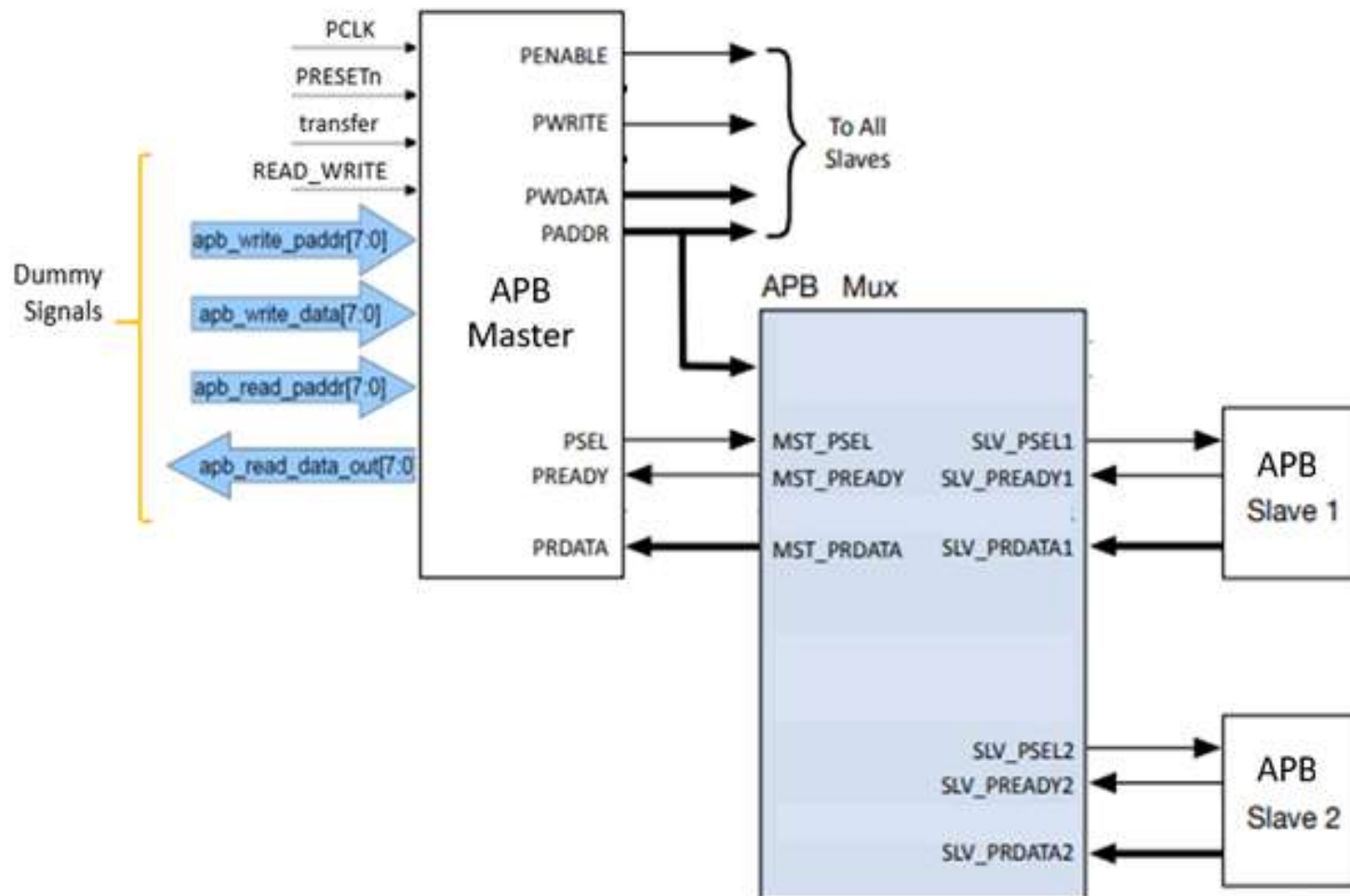


Figure 1: APB interface diagram

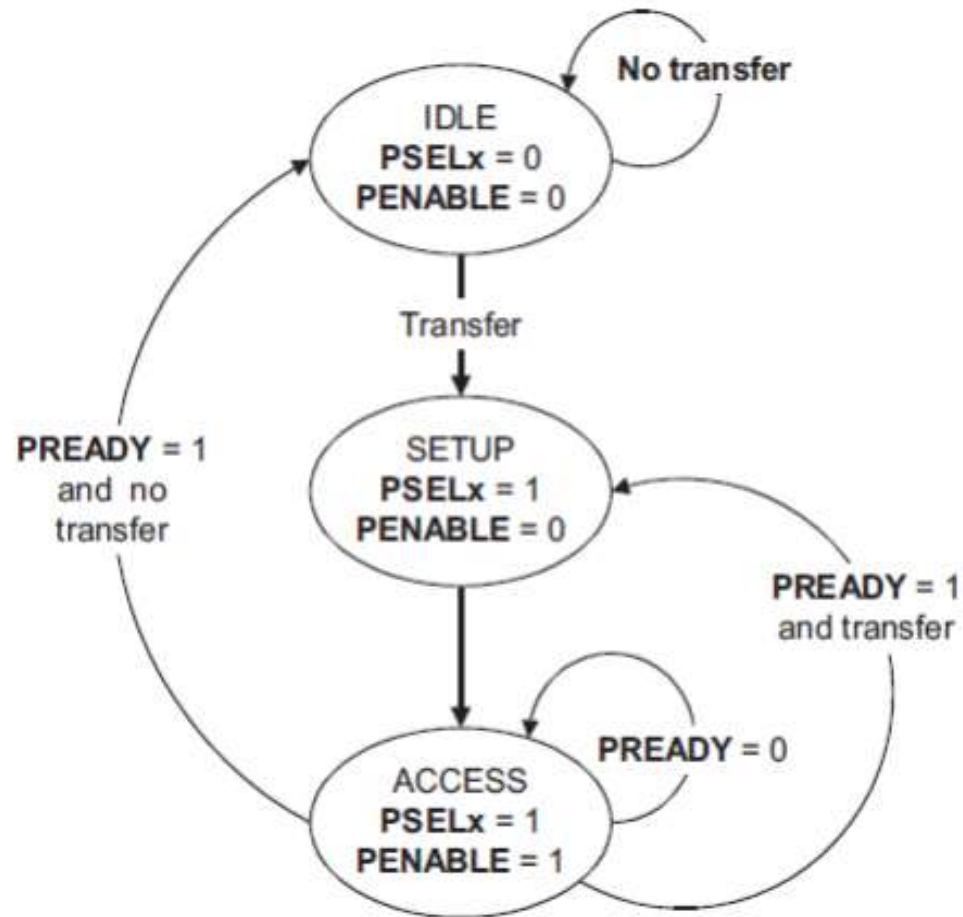


Figure 2: FSM states



# 5. Work done/Results

```
msis@centos:uvm
File Edit View Search Terminal Help
with 'UVM_OBJECT_MUST_HAVE_CONSTRUCTOR undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.
(Specify +UVM_NO_RELNOTES to turn off this notice)

UVM INFO @ 0: reporter [RNTST] Running test my test...
UVM INFO apb_protocol.sv(45) @ 5: reporter [I AM THE DUT] THE DATA HAS BEEN RANDOMIZED. WRITE_ADDRESS = x,WRITE_DATA = x, READ_ADDRESS = x
UVM WARNING my_test.svh(19) @ 10: uvm_test_top [] HI, I AM UVM
UVM INFO apb_protocol.sv(45) @ 15: reporter [I AM THE DUT] THE DATA HAS BEEN RANDOMIZED. WRITE_ADDRESS = 46,WRITE_DATA = 115, READ_ADDRESS = 10
UVM INFO apb_protocol.sv(45) @ 25: reporter [I AM THE DUT] THE DATA HAS BEEN RANDOMIZED. WRITE_ADDRESS = 57,WRITE_DATA = 234, READ_ADDRESS = 12
UVM INFO apb_protocol.sv(45) @ 35: reporter [I AM THE DUT] THE DATA HAS BEEN RANDOMIZED. WRITE_ADDRESS = 13,WRITE_DATA = 216, READ_ADDRESS = 12
UVM INFO apb_protocol.sv(45) @ 45: reporter [I AM THE DUT] THE DATA HAS BEEN RANDOMIZED. WRITE_ADDRESS = 43,WRITE_DATA = 61, READ_ADDRESS = 4
UVM INFO apb_protocol.sv(45) @ 55: reporter [I AM THE DUT] THE DATA HAS BEEN RANDOMIZED. WRITE_ADDRESS = 17,WRITE_DATA = 24, READ_ADDRESS = 63
UVM INFO /home/installs/INCISIVE152/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 55: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extra
ct' phase

--- UVM Report catcher Summary ---

Number of demoted UVM_FATAL reports : 0
Number of demoted UVM_ERROR reports : 0
Number of demoted UVM_WARNING reports: 0
Number of caught UVM_FATAL reports : 0
Number of caught UVM_ERROR reports : 0
Number of caught UVM_WARNING reports : 0

--- UVM Report Summary ---

** Report counts by severity
UVM INFO : 8
UVM WARNING : 1
UVM ERROR : 0
UVM_FATAL : 0
** Report counts by id
[] 1
[I AM THE DUT] 6
[RNTST] 1
[TEST_DONE] 1
Simulation complete via $finish{} at time 55 NS + 49
/home/installs/INCISIVE152/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_root.svh:457 $finish:
ncsim> exit
[msis@centos uvm]$
```

Fig 3: Previous UVM report summary

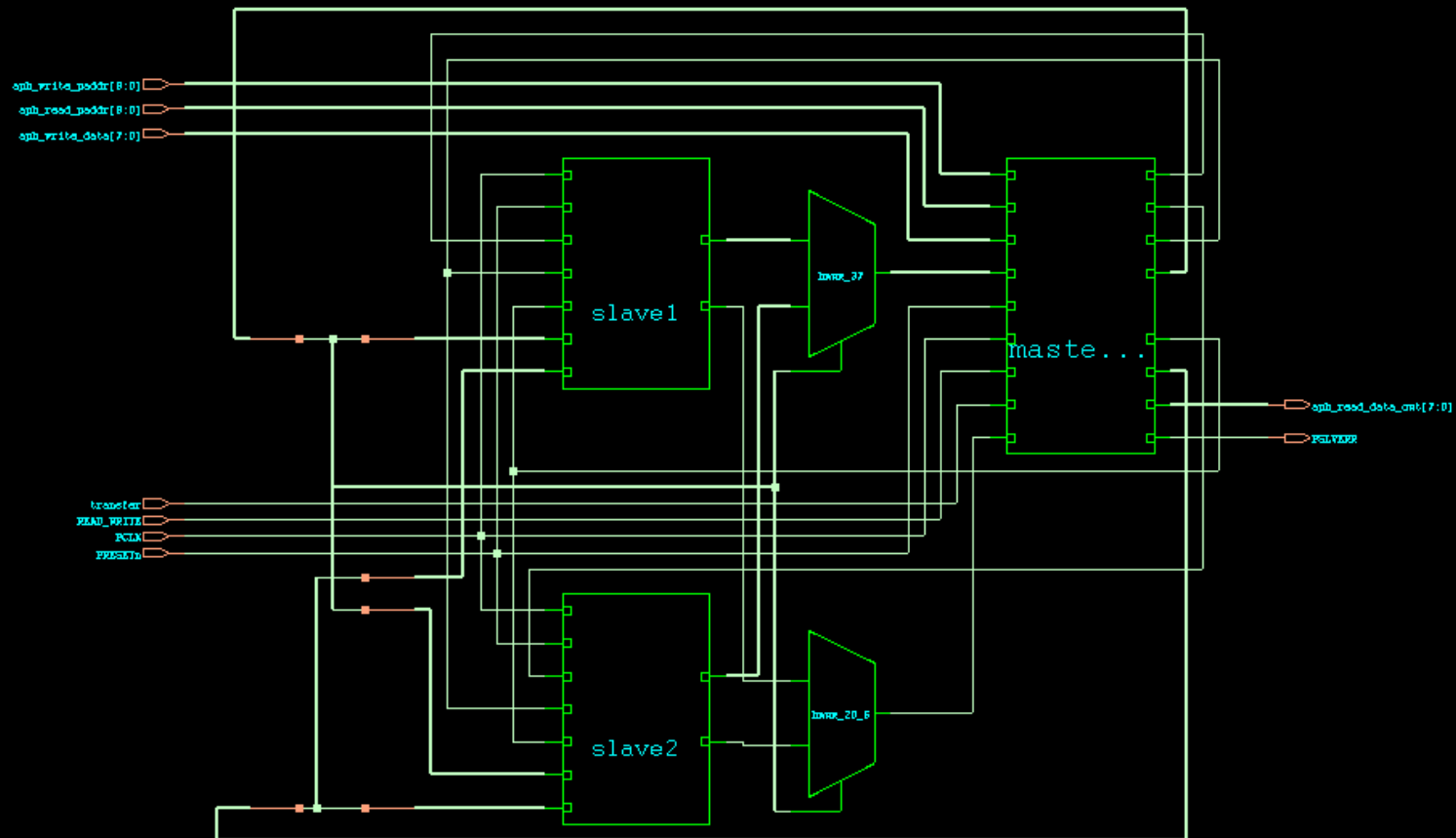


## 5. Work Done/Results

Sl.no	Operation type	Test case
1	Normal Operation Testing	Write on to the slave -1 (8x i.e contiguous memory)
2		Write on to the slave -2 (8x)
3		Write using generated random data
4		Read from Slave 1
5		Read from Slave 2
6	Error injection	Write transfer without write address
7		Read transfer without read address
8		Write transfer without valid write data

Table 1: Test cases for verification (UVM)







# 5. Work done/Results

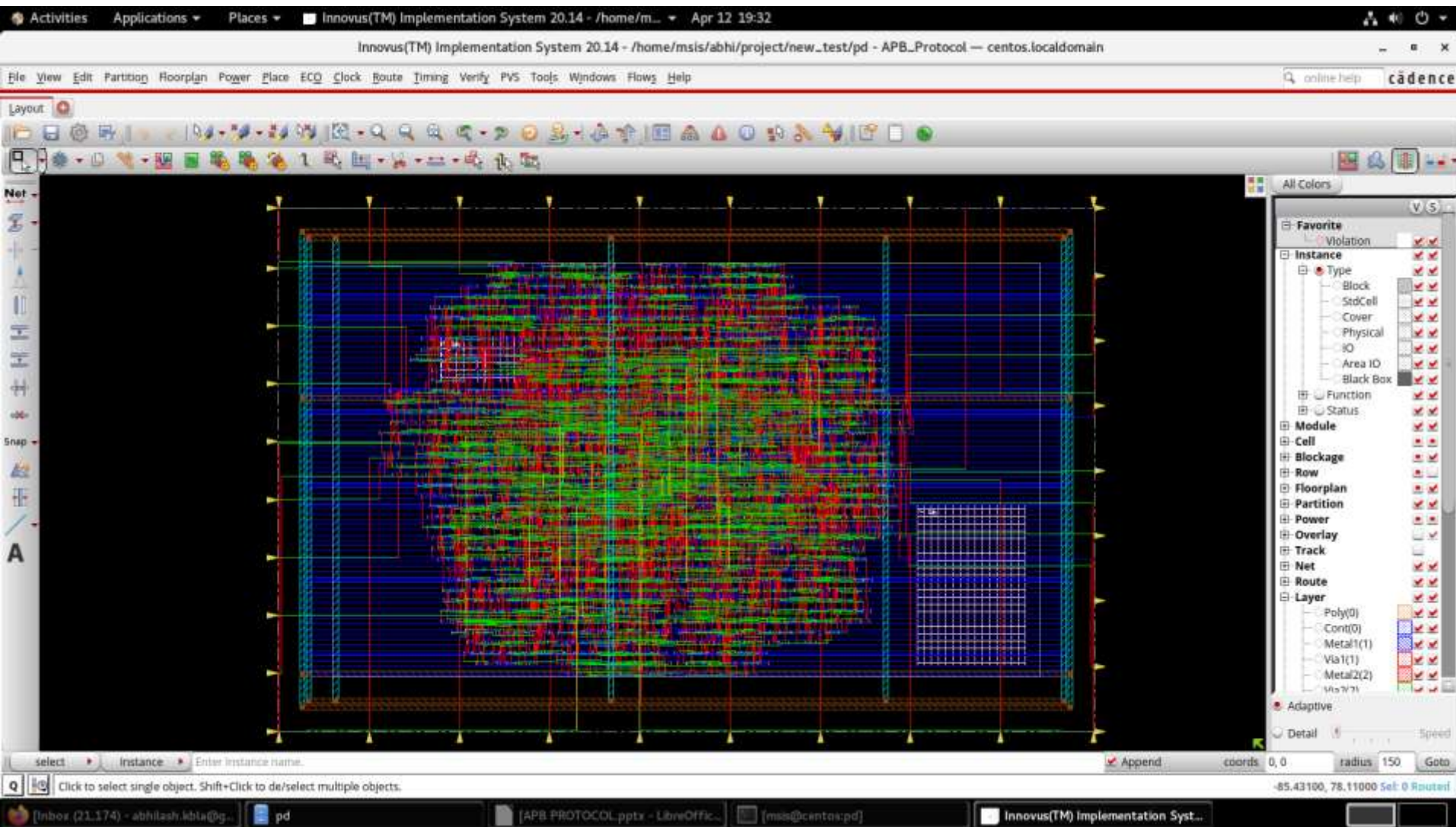


Fig 5: Previous Physical Design



# 5. Work done/Results

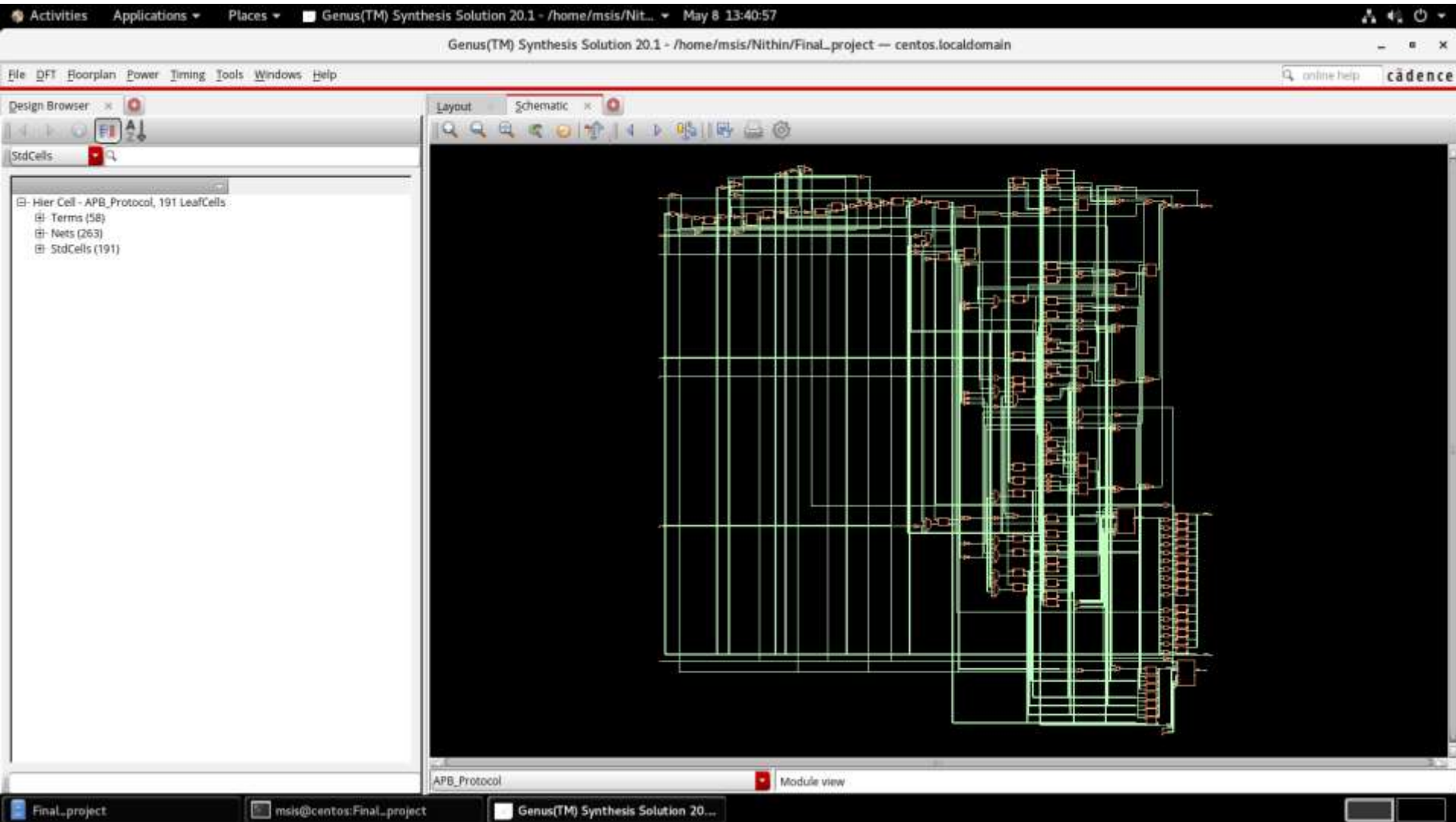


Fig 6: GUI schematic



# 5. Work done/Results

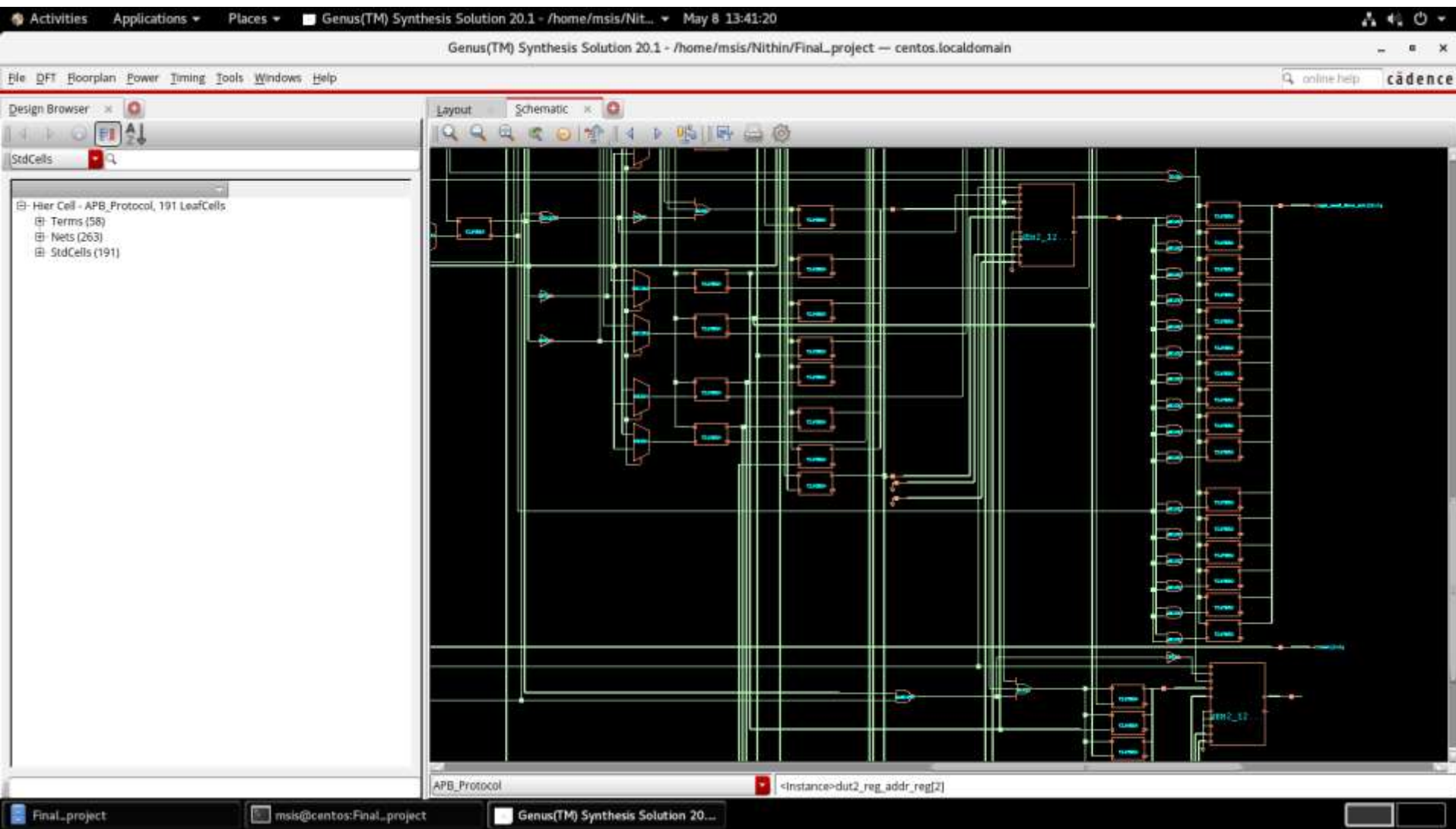


Fig 7: GUI schematic displaying Memory blocks



## 5. Work done/Results

```
constraint.sdc
File Edit View

create_clock -name PCLK -period 20 [get_ports PCLK]
set_input_delay -clock PCLK -max 3 <apb_write_data>
set_output_delay -clock PCLK -max 3 <apb_read_data_out>
set_clock_uncertainty 1 [get_clocks PCLK]
```

Property	Value
Library	fast.lib MEM2_128X16.lib
Clock frequency	50MHz
Area	1,00,000 squm
Slack	19336.2ps
Cell count	191

```
qor
File Edit View

-----
Generated by: Genus(TM) Synthesis Solution 20.11-s111_1
Generated on: May 05 2023 12:34:20 pm
Module: APB_Protocol
Technology libraries: gpdwM45wc
MEM2_128X16 1.1
Operating conditions: fast (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
-----

Timing
-----

Clock Period:
PCLK 20000.0

-----
Cost Critical Violating
Group Path Slack TNS Paths
-----
default No paths 0.0 -
PCLK 19336.2 0.0 0
Total 0.0 0
-----

Instance Count
-----
Leaf Instance Count 191
Physical Instance count 0
Sequential Instance Count 62
Combinational Instance Count 129
Hierarchical Instance Count 0

Area
-----
Cell Area 100000.000
Physical Cell Area 0.000
Total Cell Area (Cell+Physical) 100000.000
Net Area 0.000
Total Area (Cell+Physical+Net) 100000.000

Max Fanout 32 (n_138)
Min Fanout 0 (dut2_PRDATA1)
Average Fanout 2.1
Terms to net ratio 3.2129
Terms to instance ratio 4.4241
Runtime 11.578836 seconds
Elapsed Runtime 12 seconds
Genus peak memory usage 1289.91
Innovus peak memory usage no_value
Hostname centos.localdomain
```

Fig 8: Constraints and Report summary





# 5. Work done/Results

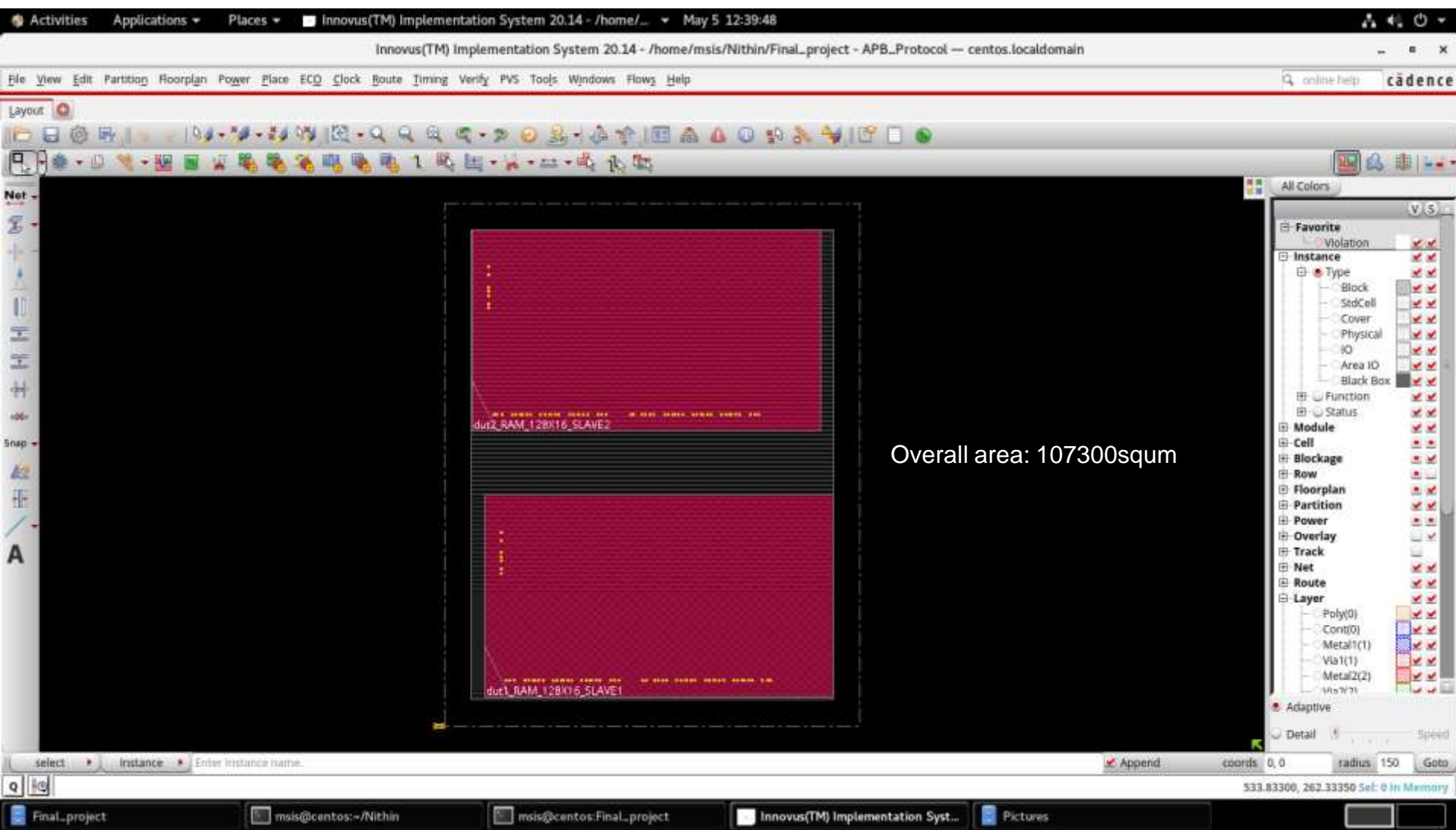


Fig 9: Floor planning



# 5. Work done/Results

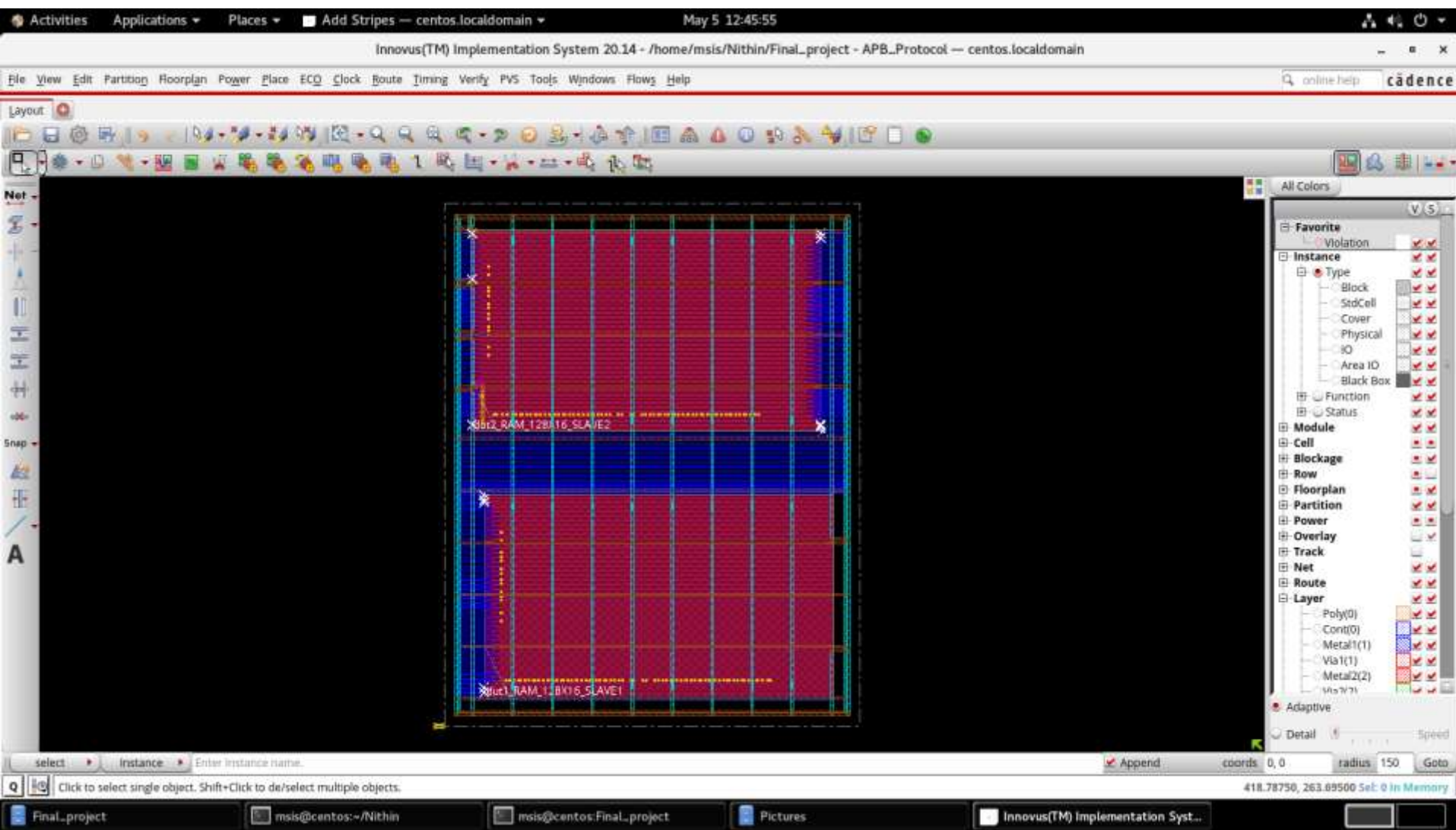


Fig 10: Power planning



# 5. Work done/Results

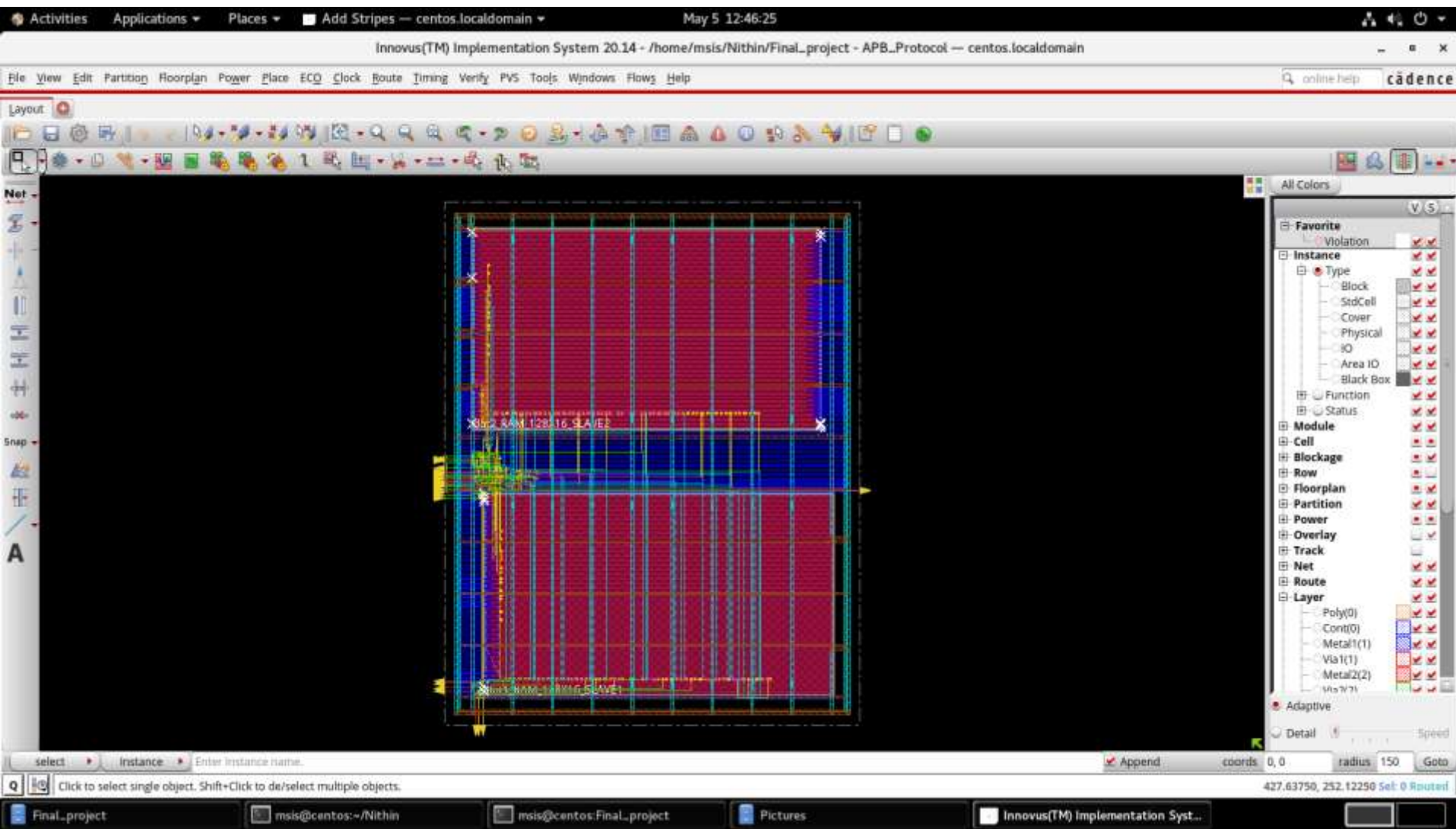


Fig 11: Standard cell placement with wiring



## 5. Work done/Results

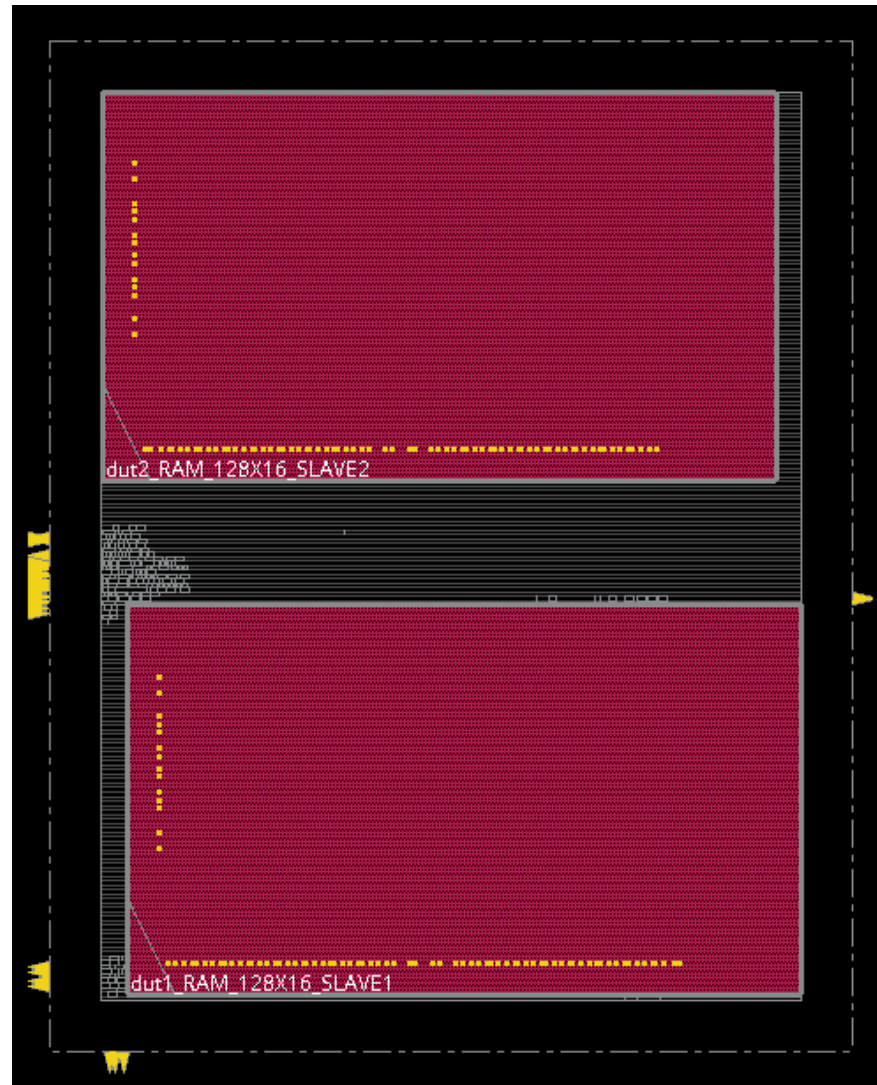


Fig 12: Standard cells placement

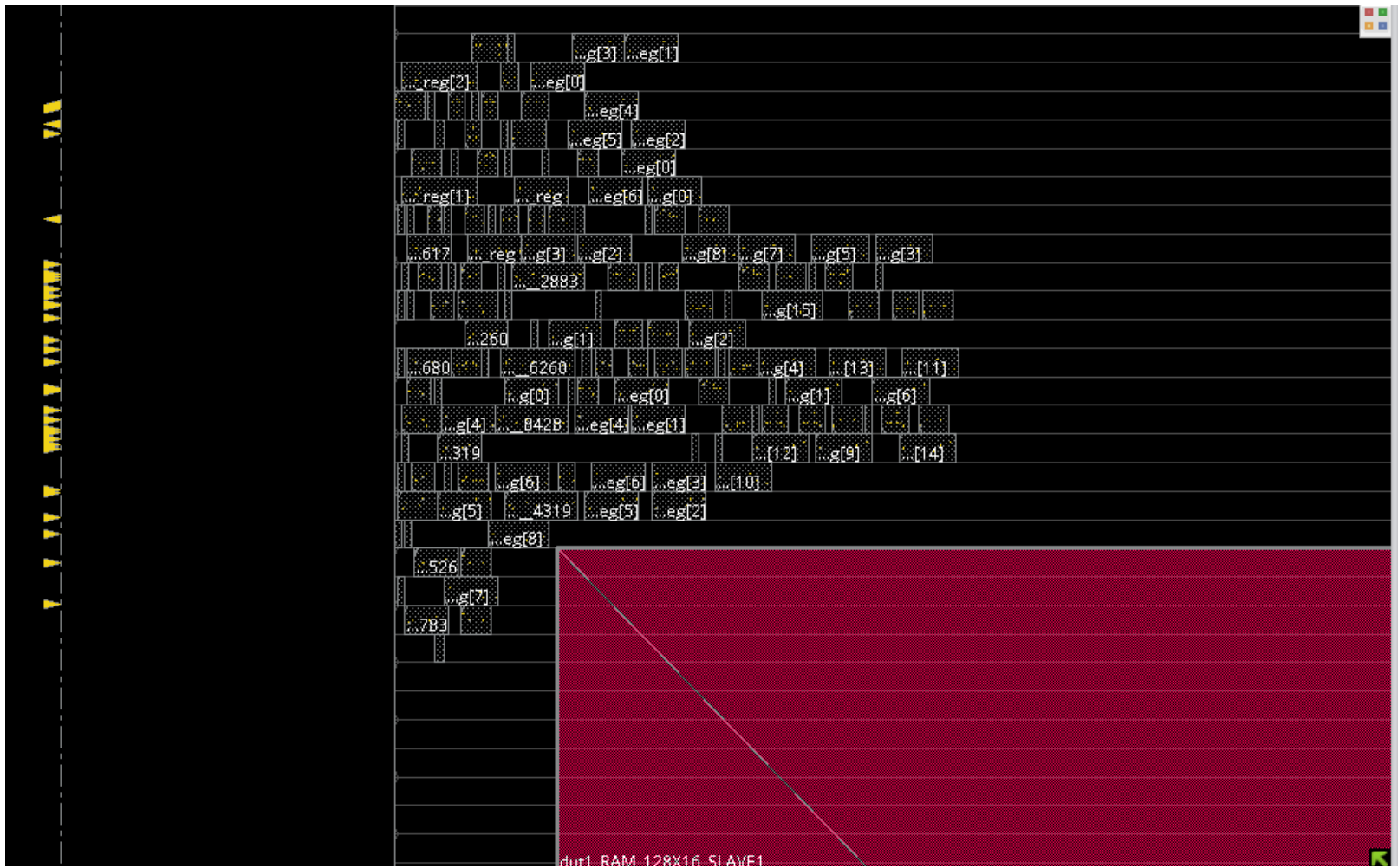


Fig 13: Standard cells placement



# 5. Work done/Results

Activities Applications Places Optimization — centos.localdomain May 5 12:59:37  
msis@centos:Final\_project

File Edit View Search Terminal Help

Start delay calculation (fullDC) (1 T). (MEM=1554.48)  
Total number of fetched objects 348  
AAE\_INFO: Total number of nets for which stage creation was skipped for all views 0  
End delay calculation. (MEM=1581.69 CPU=0:00:00.0 REAL=0:00:00.0)  
End delay calculation (fullDC). (MEM=1581.69 CPU=0:00:00.0 REAL=0:00:00.0)  
\*\*\* Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0 totSessionCpu=0:02:12 mem=1581.7M)

Initial Summary

Setup views included:  
slow

Setup mode	all
WNS (ns):	17.699
TNS (ns):	0.000
Violating Paths:	0
All Paths:	5

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 3.820%

\*\*\*optDesign ... cpu = 0:00:02, real = 0:00:02, mem = 1519.5M, totSessionCpu=0:02:12 \*\*  
\*\*\* InitOpt #2 [finish] : cpu/real = 0:00:01.7/0:00:01.7 (1.0), totSession cpu/real = 0:02:11.6/0:15:49.8 (0.1), mem = 1551.9M  
\*\* INFO : this run is activating medium effort placeOptDesign flow  
\*\*Info: (IMPSP-307): Design contains fractional 17 cells.  
\*\*Info: (IMPSP-307): Design contains fractional 17 cells.  
\*\*\* Starting optimizing excluded clock nets MEM= 1551.9M \*\*\*  
\*info: No excluded clock nets to be optimized.

Timing Analysis — centos.localdomain

Basic Advanced

☐ Use Existing Extraction and Timing Data

**Design Stage**

☐ Pre-Place ☒ Pre-CTS ☐ Post-CTS ☐ Post-Route ☐ Sign-Off

**Analysis Type**

☒ Setup ☐ Hold

**Reporting Options**

Number of Paths: 50  
Report file(s) Prefix: APB\_Protocol\_preCTS  
Output Directory: timingReports

OK Apply Cancel Help

Final\_project msi@centos:~/Nithin msi@centos:Final\_proje Pictures Innovus(TM) Implementa... [Optimization — centos... Timing Analysis — centos...

Fig 14: Pre-CTS setup timing report



# 5. Work done/Results

The screenshot shows a terminal window with a timing analysis report and a 'Timing Analysis' dialog box. The terminal output includes design settings, delay calculations, and a 'timeDesign Summary' table. The dialog box is configured for a Pre-CTS hold analysis.

**Design Settings:**

- Design Stage: PreRoute
- Design Name: APB\_Protocol
- Design Mode: 90nm
- Analysis Mode: MMC Non-OCV
- Parasitics Mode: No SPEF/RCDB
- Signoff Settings: SI Off

**Delay Calculations:**

- Calculate delays in BcWc mode...
- Start delay calculation (fullDC) (1 T). (MEM=1532,57)
- \*\*\* Calculating scaling factor for tbest libraries using the default operating condition of each library.
- Total number of fetched objects 348
- AAE\_INFO: Total number of nets for which stage creation was skipped for all views 0
- End delay calculation. (MEM=1559.78 CPU=0:00:00.0 REAL=0:00:00.0)
- End delay calculation (fullDC). (MEM=1559.78 CPU=0:00:00.1 REAL=0:00:00.0)
- Turning on fast DC mode.
- \*\*\* Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0 totSessionCpu=0:00:00.1)

**timeDesign Summary**

Hold mode	all	reg2reg	default
WNS (ns):	-0.007	0.156	-0.007
TNS (ns):	-0.013	0.000	-0.013
Violating Paths:	2	0	2
All Paths:	5	3	5

**Reported timing to dir timingReports**

- Total CPU time: 0.19 sec
- Total Real time: 0.0 sec
- Total Memory Usage: 1495.265625 Mbytes
- \*\*\* timeDesign #1 [finish] : cpu/real = 0:00:00.2/0:00:00.2 (1.0), totSession cpu/real = 0:02:24.4/0:16:41.9 (0.1), mem = 1495.3M

**Timing Analysis Dialog Box:**

- Basic tab selected
- Use Existing Extraction and Timing Data: ☐
- Design Stage: ☐ Pre-Place ☒ Pre-CTS ☐ Post-CTS ☐ Post-Route ☐ Sign-Off
- Analysis Type: ☐ Setup ☒ Hold
- Reporting Options:
  - Number of Paths: 50
  - Report file(s) Prefix: APB\_Protocol\_preCTS
  - Output Directory: timingReports
- Buttons: OK, Apply, Cancel, Help

Fig 15: Pre-CTS hold timing report



## 5. Work done/Results

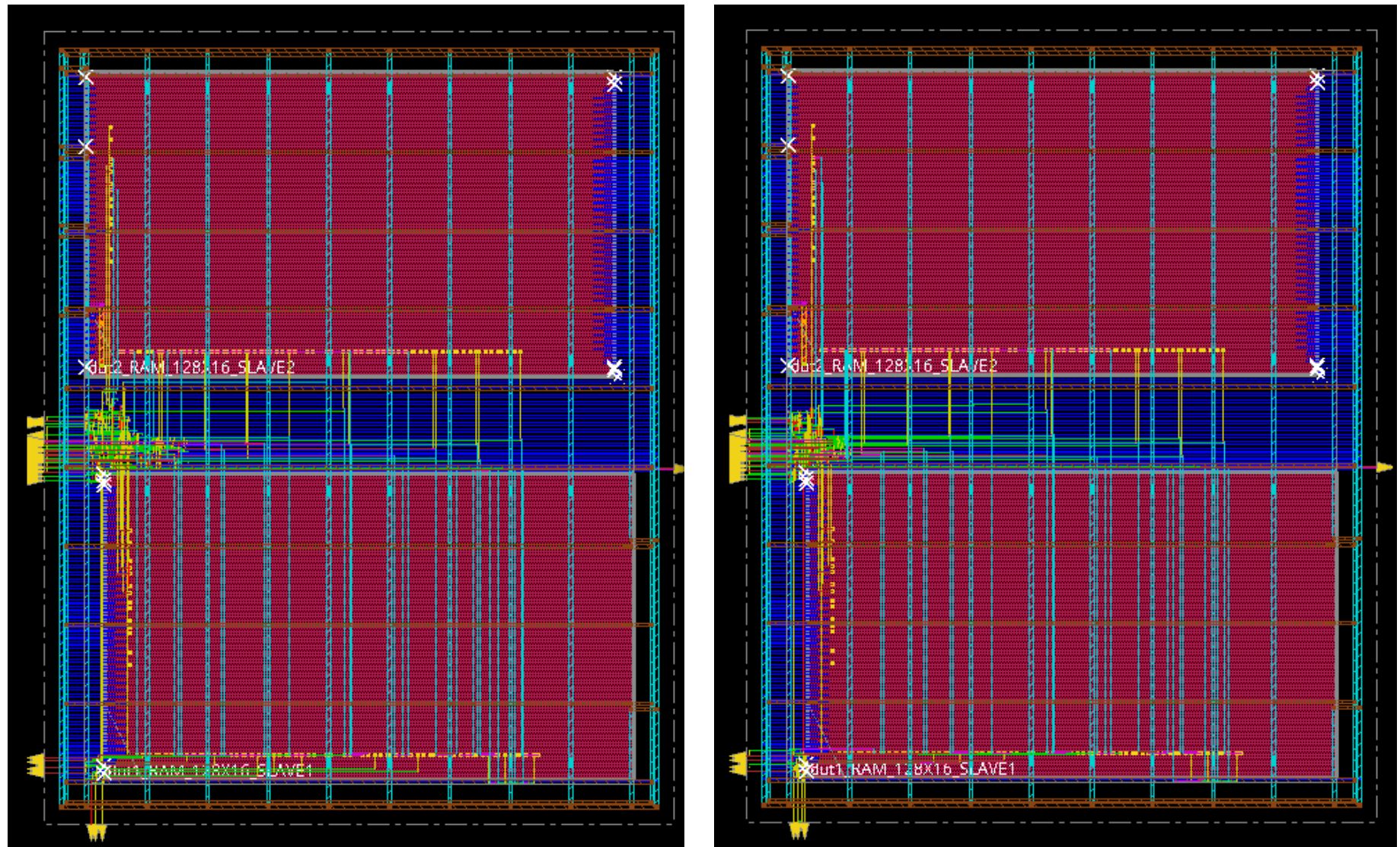


Fig 16: Pre & Post CTS design Optimization changes



# 5. Work done/Results

Activities Applications Places Optimization — centos.localdomain May 5 13:01:01  
msis@centos:Final\_project

File Edit View Search Terminal Help

```
*** optDesign #2 [finish] : cpu/real = 0:00:03.3/0:00:03.8 (0.9), totSession cpu/real = 0:02:37.7/0:17:32.4 (0.1), mem = 1628.7M
innovus 1> *** timeDesign #2 [begin] : totSession cpu/real = 0:02:39.8/0:17:52.3 (0.1), mem = 1628.7M
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1565.7M)
```

-----  
timeDesign Summary  
-----

Setup views included:  
slow

Setup mode	all	reg2reg	default
WNS (ns):	17.756	18.829	17.756
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	5	3	5

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	0 (0)	0.000	0 (0)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 3.842%

Routing Overflow: 0.00% H and 0.00% V

-----  
Reported timing to dir timingReports  
Total CPU time: 0.1 sec  
Total Real time: 0.0 sec  
Total Memory Usage: 1582.414062 Mbytes  
\*\*\* timeDesign #2 [finish] : cpu/real = 0:00:00.1/0:00:00.1 (1.1), totSession cpu/real = 0:02:39.9/0:17:52.4 (0.1), mem = 1582.4M  
innovus 1>

Timing Analysis — centos.localdomain

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☒ Post-CTS ☐ Post-Route ☐ Sign-Off

Analysis Type

☒ Setup ☐ Hold

Reporting Options

Number of Paths: 50

Report file(s) Prefix: APB\_Protocol\_postCTS

Output Directory: timingReports

OK Apply Cancel Help

Final\_project msis@centos:~/Nithin msis@centos:Final\_proje Pictures Innovus(TM) Implementa... Optimization — centos.L... Timing Analysis — centos...

Fig 17: Post-CTS setup timing report





# 5. Work done/Results

\*\*\*\*\*  
# Design Stage: PreRoute  
# Design Name: APB Protocol  
# Design Mode: 90nm  
# Analysis Mode: MMMC Non-OCV  
# Parasitics Mode: No SPEF/RCDB  
# Signoff Settings: SI Off  
\*\*\*\*\*  
Calculate delays in BcWc mode..  
Start delay calculation (fullDC) (1 T). (MEM=1568.92)  
\*\*\* Calculating scaling factor for tbest libraries using the default operating condition of each library.  
Total number of fetched objects 350  
AAE INFO: Total number of nets for which stage creation was skipped for all views 0  
End delay calculation. (MEM=1596.13 CPU=0:00:00.0 REAL=0:00:00.0)  
End delay calculation (fullDC). (MEM=1596.13 CPU=0:00:00.0 REAL=0:00:00.0)  
\*\*\* Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0 totSession

-----  
timeDesign Summary  
-----  
Hold views included:  
fast

Hold mode	all	reg2reg	default
WNS (ns):	0.019	0.156	0.019
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	5	3	5

Density: 3.842%  
Routing Overflow: 0.00% H and 0.00% V  
-----  
Reported timing to dir timingReports  
Total CPU time: 0.18 sec  
Total Real time: 0.0 sec  
Total Memory Usage: 1530.617188 Mbytes  
\*\*\* timeDesign #3 [finish] : cpu/real = 0:00:00.2/0:00:00.2 (1.0), totSession cpu/real = 0:02:41.3/0:18:04.4 (0.1), mem = 1530.6M  
innovus 1>

Timing Analysis — centos.localdomain

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☒ Post-CTS ☐ Post-Route ☐ Sign-Off

Analysis Type

☐ Setup ☒ Hold

Reporting Options

Number of Paths: 50

Report file(s) Prefix: APB\_Protocol\_postCTS

Output Directory: timingReports

OK Apply Cancel Help

Fig 18: Post-CTS hold timing report

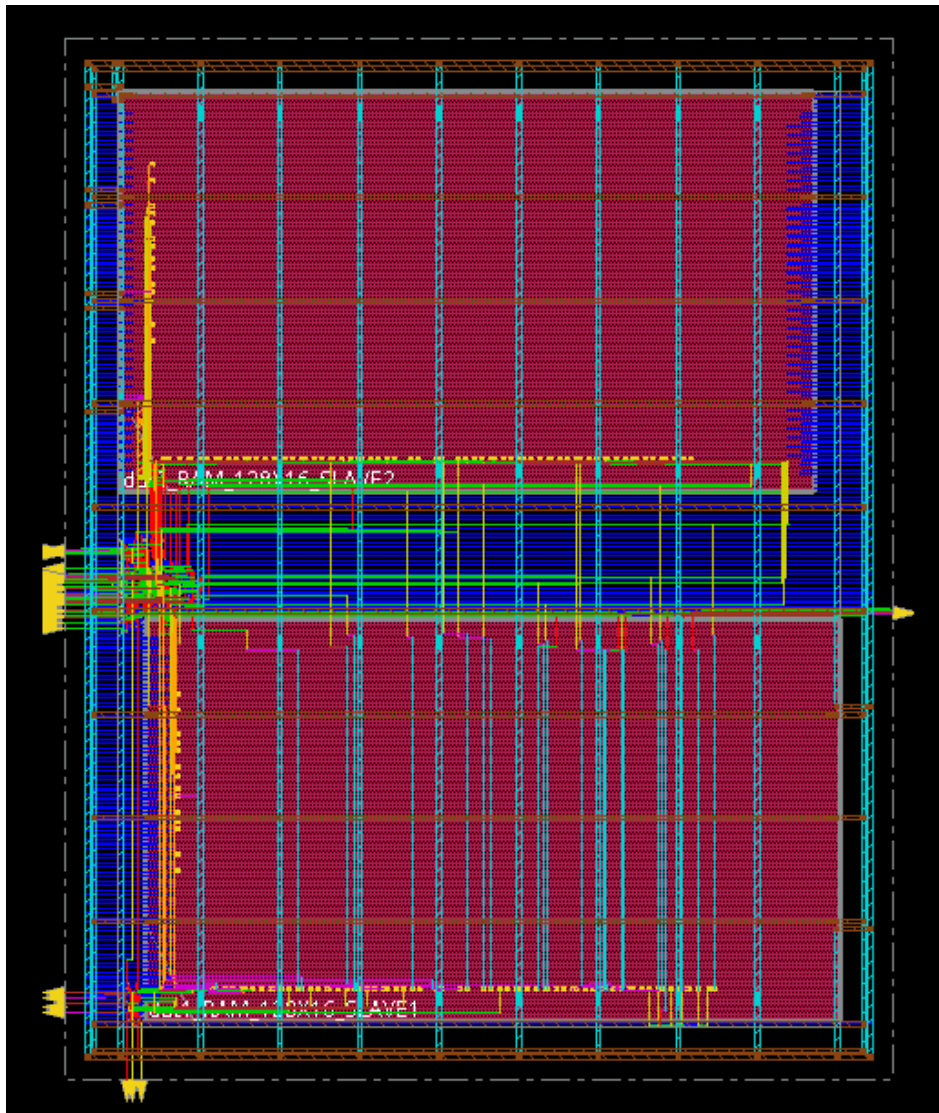


Fig 19: Post Routing



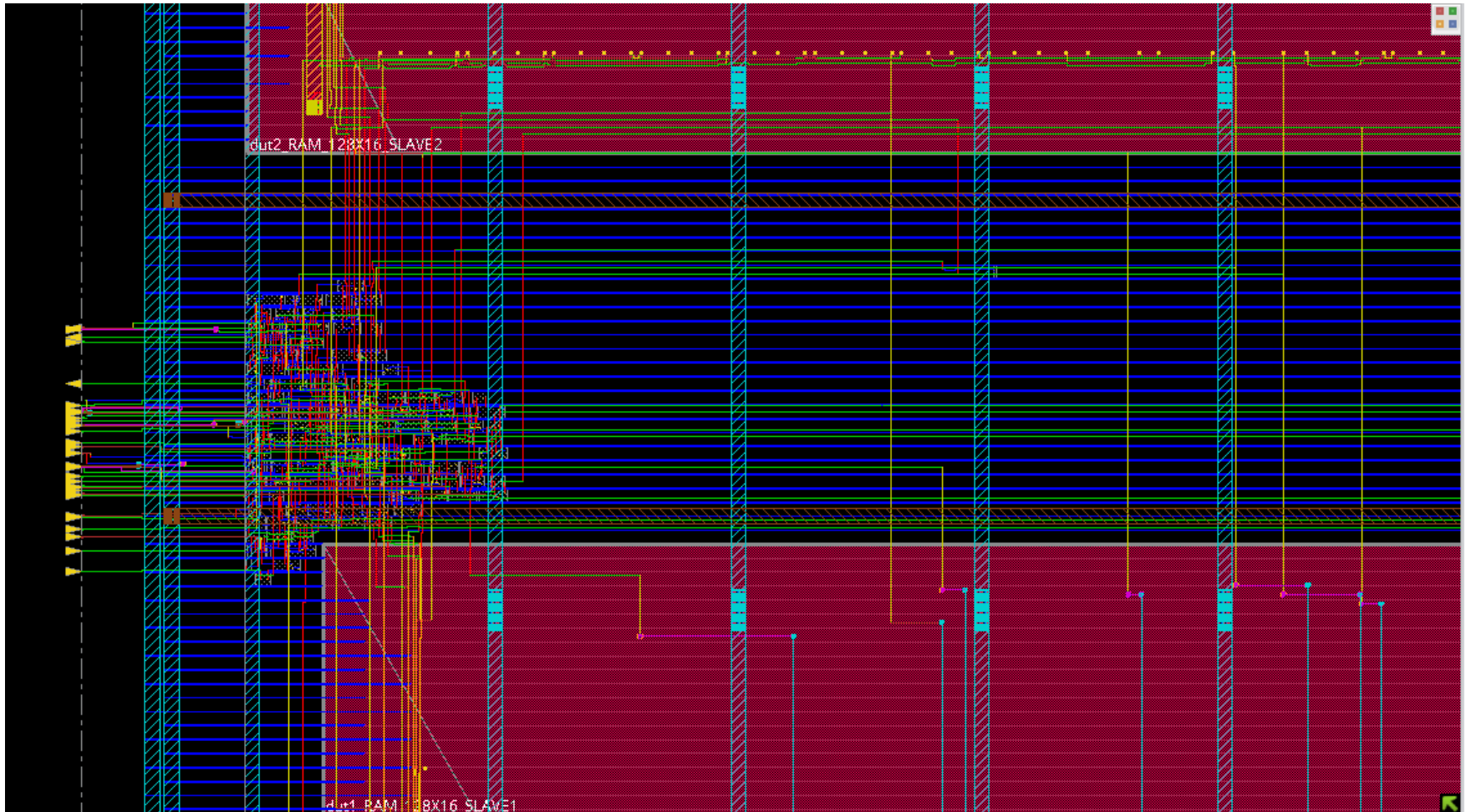


Fig 20: Post Routing standard cell connection close up



# 5. Work done/Results

The screenshot shows a terminal window with a timing analysis report and a dialog box for timing analysis setup.

**Timing Analysis Summary**

Setup mode	all	reg2reg	default
WNS (ns):	17.779	18.841	17.779
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	5	3	5

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)
max_cap	0 (0)	0.000	0 (0)
max_tran	1 (2)	-0.021	1 (2)
max_fanout	0 (0)	0	0 (0)
max_length	0 (0)	0	0 (0)

Density: 3.842%

Total number of glitch violations: 0

Reported timing to dir timingReports

Total CPU time: 0.73 sec

Total Real time: 1.0 sec

Total Memory Usage: 1610.90625 Mbytes

Reset AAE Options

\*\*\* timeDesign #4 [finish] : cpu/real = 0:00:00.7/0:00:01.1 (0.7), totSession cpu/real = 0:02:56.5/0:19:25.1 (0.2), mem = 1610.9M

innovus 2>

**Timing Analysis — centos.localdomain**

Basic Advanced

Use Existing Extraction and Timing Data

**Design Stage**

☐ Pre-Place ☐ Pre-CTS ☐ Post-CTS ☒ Post-Route ☐ Sign-Off

**Analysis Type**

☒ Setup ☐ Hold

**Reporting Options**

Number of Paths: 50

Report file(s) Prefix: APB\_Protocol\_postRoute

Output Directory: timingReports

OK Apply Cancel Help

Fig 21: Post Routing setup timing report



# 5. Work done/Results

AAE INFO-618: Total number of nets in the design is 356, 98.0 percent of the nets selected for SI analysis  
End delay calculation. (MEM=1611 CPU=0:00:00.0 REAL=0:00:00.0)  
End delay calculation (fullDC). (MEM=1611 CPU=0:00:00.2 REAL=0:00:00.0)  
Loading CTE timing window with TwFlowType 0.. (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 1611.0M)  
Add other clocks and setupCteToAAEClockMapping during iter 1  
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 1611.0M)  
Starting SI iteration 2  
Start delay calculation (fullDC) (1 T). (MEM=1575.12)  
Glitch Analysis: View fast -- Total Number of Nets Skipped = 0.  
Glitch Analysis: View fast -- Total Number of Nets Analyzed = 350.  
Total number of fetched objects 350  
AAE INFO: Total number of nets for which stage creation was skipped for all views 0  
AAE INFO-618: Total number of nets in the design is 356, 20.5 percent of the nets selected for SI analysis  
End delay calculation. (MEM=1619.81 CPU=0:00:00.0 REAL=0:00:00.0)  
End delay calculation (fullDC). (MEM=1619.81 CPU=0:00:00.0 REAL=0:00:00.0)  
\*\*\* Done Building Timing Graph (cpu=0:00:00.3 real=0:00:00.0 totSession

timeDesign Summary

Hold views included:  
fast

Hold mode	all	reg2reg	default
WNS (ns):	0.018	0.154	0.018
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	5	3	5

Density: 3.842%

Reported timing to dir timingReports  
Total CPU time: 0.7 sec  
Total Real time: 1.0 sec  
Total Memory Usage: 1551.085938 Mbytes  
Reset AAE Options:  
\*\*\* timeDesign #5 [finish] : cpu/real = 0:00:00.7/0:00:01.0 (0.7), totSession cpu/real = 0:02:58.3/0:19:36.4 (0.2), mem = 1551.1M  
innovus 2>

Timing Analysis — centos.localdomain

Basic Advanced

☐ Use Existing Extraction and Timing Data

Design Stage

☐ Pre-Place ☐ Pre-CTS ☐ Post-CTS ☒ Post-Route ☐ Sign-Off

Analysis Type

☐ Setup ☒ Hold

Reporting Options

Number of Paths: 50

Report file(s) Prefix: APB\_Protocol\_postRoute

Output Directory: timingReports

OK Apply Cancel Help

Fig 22: Post Routing hold timing report



## 5. Work done/Results

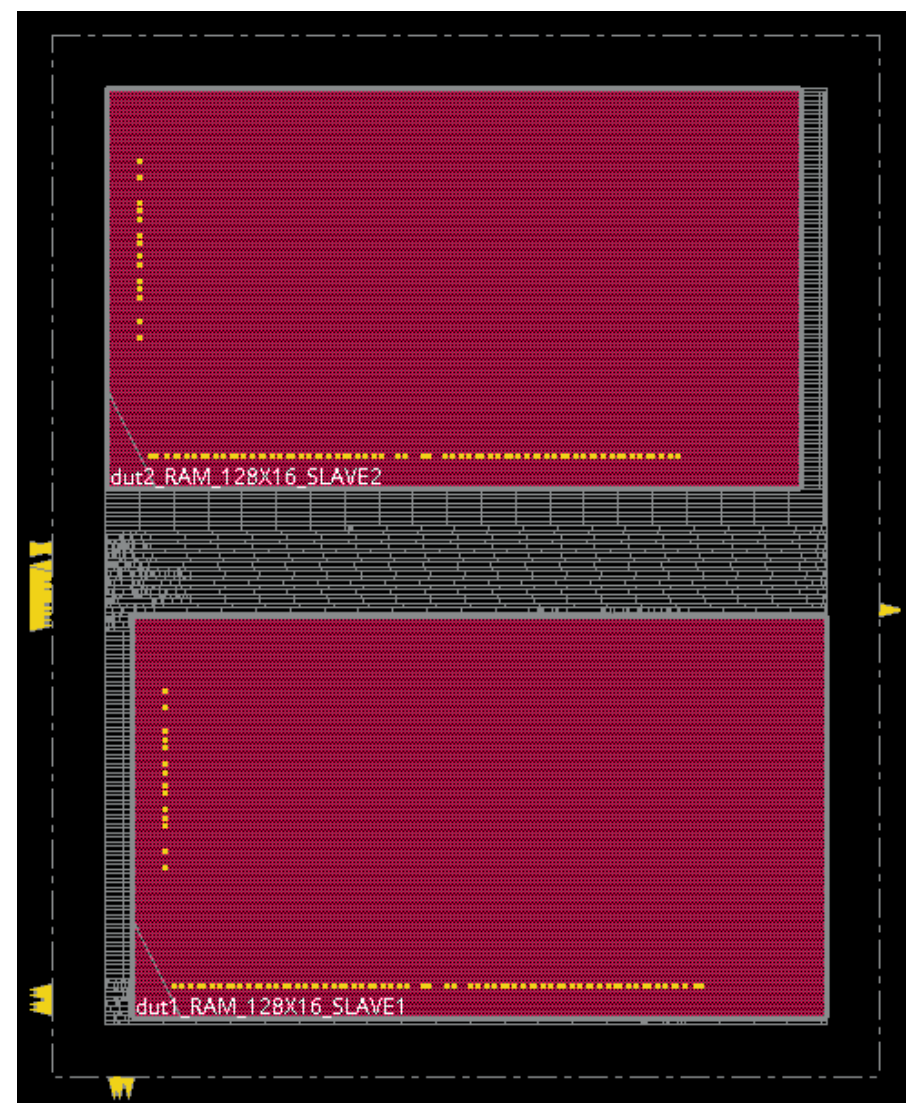
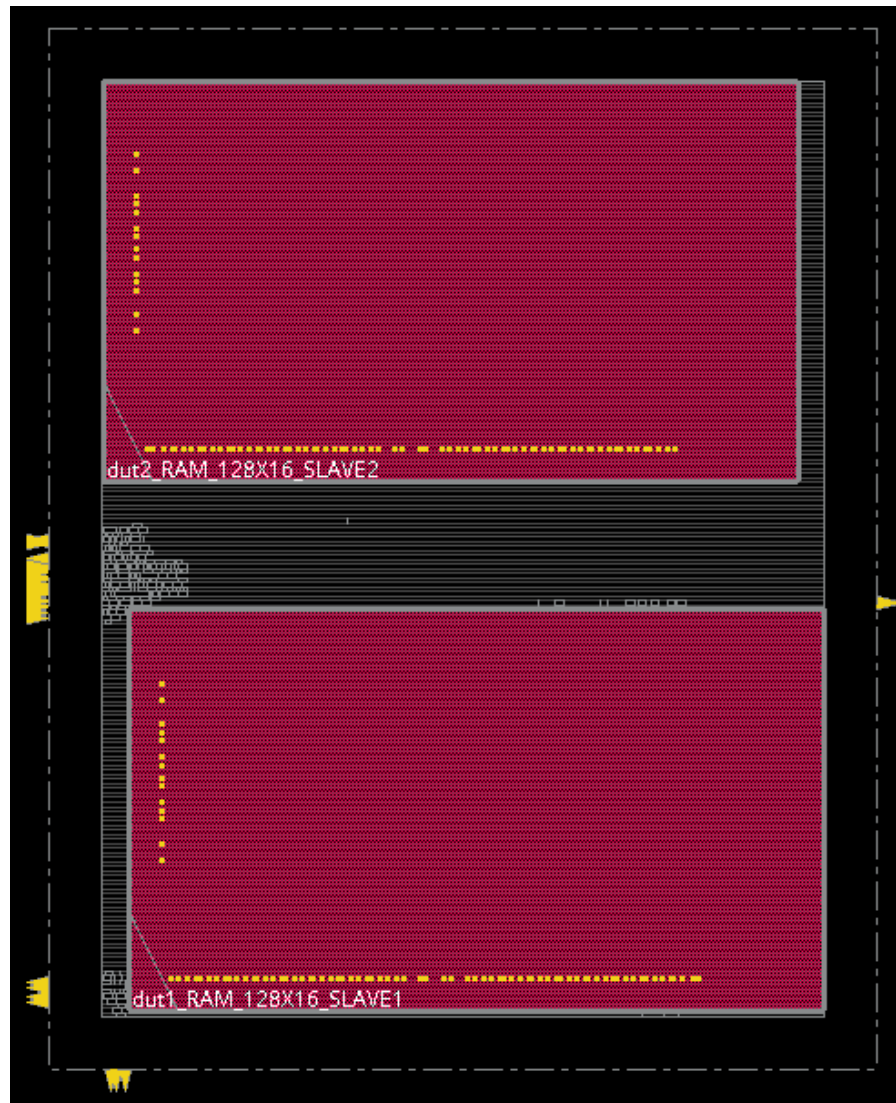


Fig 23: Adding fillers



# 5. Work done/Results

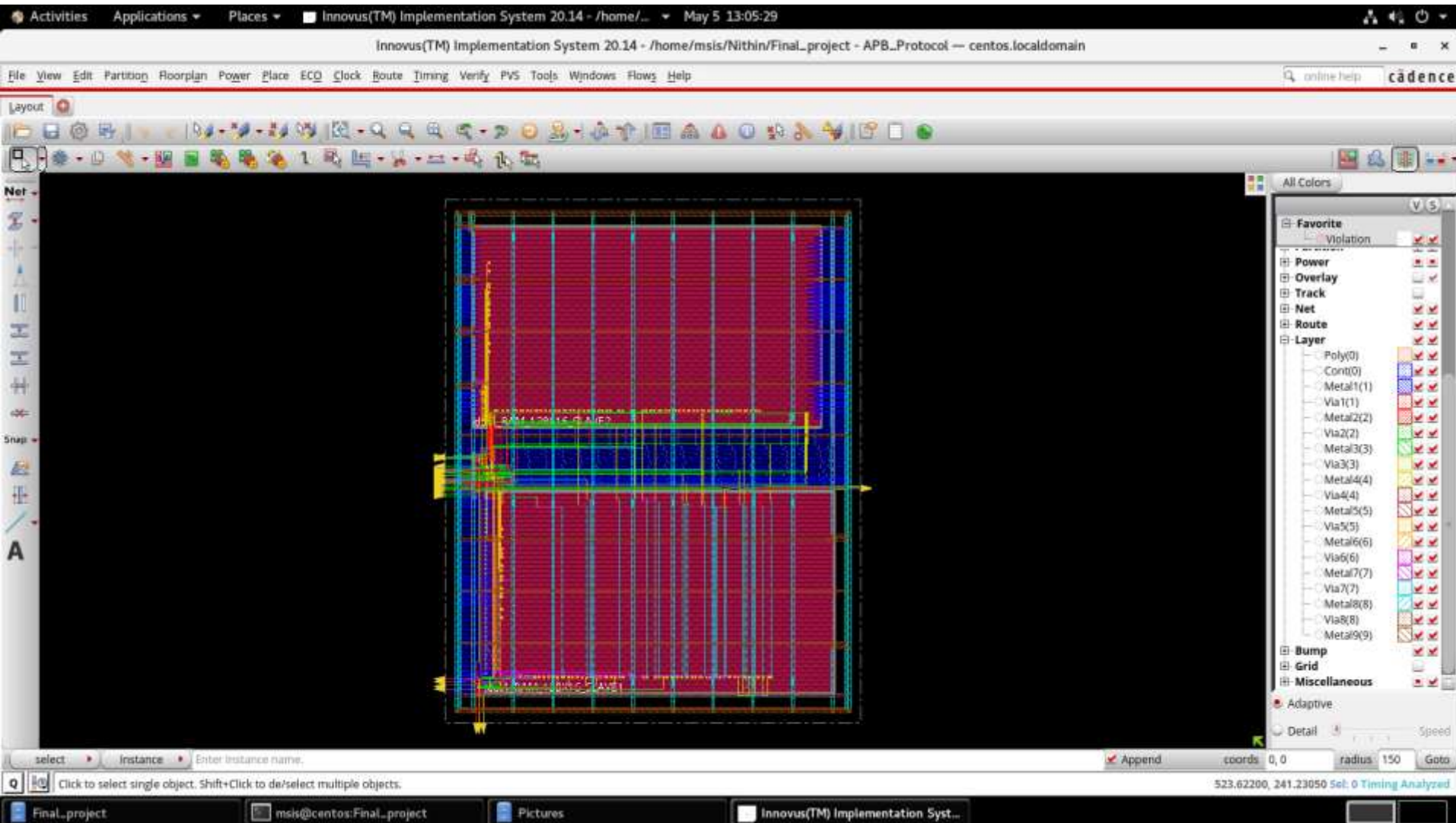


Fig 24: Final Design



## 5. Work done/Results

### Timing Report Summary

Sl. No	Stage	Setup timing (in ns)	Hold timing (in ns)
1	Pre CTS	17.699	-0.07
2	Post CTS	17.756	0.019
3	Post Routing	17.779	0.018





# 5. Work done/Results

```
Activities Applications Places Terminal May 5 13:04:15
msis@centos:Final_project

File Edit View Search Terminal Help
VERIFY DRC ..... Sub-Area: {155.520 0.000 233.280 78.720} 3 of 20
VERIFY DRC ..... Sub-Area : 3 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {233.280 0.000 310.000 78.720} 4 of 20
VERIFY DRC ..... Sub-Area : 4 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 78.720 77.760 157.440} 5 of 20
VERIFY DRC ..... Sub-Area : 5 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {77.760 78.720 155.520 157.440} 6 of 20
VERIFY DRC ..... Sub-Area : 6 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {155.520 78.720 233.280 157.440} 7 of 20
VERIFY DRC ..... Sub-Area : 7 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {233.280 78.720 310.000 157.440} 8 of 20
VERIFY DRC ..... Sub-Area : 8 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 157.440 77.760 236.160} 9 of 20
VERIFY DRC ..... Sub-Area : 9 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {77.760 157.440 155.520 236.160} 10 of 20
VERIFY DRC ..... Sub-Area : 10 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {155.520 157.440 233.280 236.160} 11 of 20
VERIFY DRC ..... Sub-Area : 11 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {233.280 157.440 310.000 236.160} 12 of 20
VERIFY DRC ..... Sub-Area : 12 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 236.160 77.760 314.880} 13 of 20
VERIFY DRC ..... Sub-Area : 13 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {77.760 236.160 155.520 314.880} 14 of 20
VERIFY DRC ..... Sub-Area : 14 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {155.520 236.160 233.280 314.880} 15 of 20
VERIFY DRC ..... Sub-Area : 15 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {233.280 236.160 310.000 314.880} 16 of 20
VERIFY DRC ..... Sub-Area : 16 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 314.880 77.760 389.880} 17 of 20
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {77.760 314.880 155.520 389.880} 18 of 20
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {155.520 314.880 233.280 389.880} 19 of 20
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {233.280 314.880 310.000 389.880} 20 of 20
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.4 ELAPSED TIME: 0.00 MEM: 0.0M) ***

Innovus 2>
```

Fig 25: DRC check



## 5. Work done/Results

### UVM

Sl.no	Operation type	Test case
1	Normal Operation Testing	Write on to the slave -1 (8x i.e contiguous memory)
2		Write on to the slave -2 (8x)
3		Write using generated random data
4		Read from Slave 1
5		Read from Slave 2
6	Error injection	Write transfer without write address
7		Read transfer without read address
8		Write transfer without valid write data

Table 1: Test cases for verification





# 5. Work done/Results

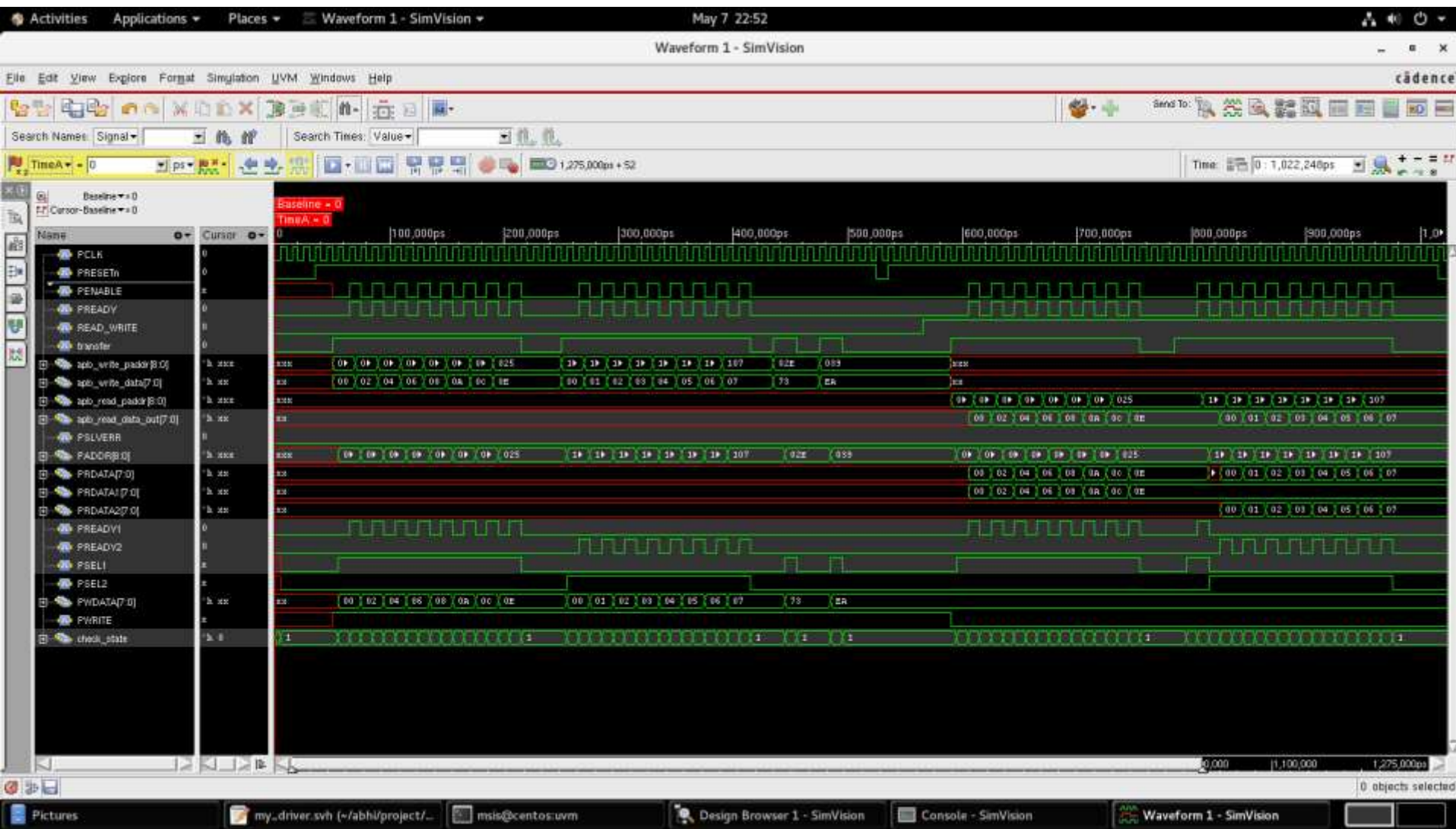


Fig 26: Simulation Results



# 5. Work done/Results

```
SLAVE 1 WRITE OPERATION 8X

UVM_INFO my_monitor.svh(38) @ 65000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name                Type      Size  Value
-----
seq                 seq_item -    @3755
apb_write_paddr     integral 9     'h1e
apb_write_data      integral 8     'h0
apb_read_paddr      integral 9     'h0XXX
PSLVERR             integral 1     'h0
apb_read_data_out   integral 8     'h0xx
-----

UVM_INFO my_monitor.svh(38) @ 85000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name                Type      Size  Value
-----
seq                 seq_item -    @3755
apb_write_paddr     integral 9     'h1f
apb_write_data      integral 8     'h2
apb_read_paddr      integral 9     'h0XXX
PSLVERR             integral 1     'h0
apb_read_data_out   integral 8     'h0xx
-----

UVM_INFO my_monitor.svh(38) @ 105000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name                Type      Size  Value
-----
seq                 seq_item -    @3755
apb_write_paddr     integral 9     'h20
apb_write_data      integral 8     'h4
apb_read_paddr      integral 9     'h0XXX
PSLVERR             integral 1     'h0
apb_read_data_out   integral 8     'h0xx
-----

UVM_INFO my_monitor.svh(38) @ 125000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name                Type      Size  Value
-----
seq                 seq_item -    @3755
apb_write_paddr     integral 9     'h21
apb_write_data      integral 8     'h6
apb_read_paddr      integral 9     'h0XXX
```

Fig 27: Write to Slave 1



# 5. Work done/Results

```
Activities Applications Places Terminal May 7 19:43
msis@centos:uvm

File Edit View Search Terminal Help
SLAVE 2 WRITE OPERATION BX
UVM_INFO my_monitor.svh(38) @ 265000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name          Type      Size  Value
-----
seq           seq_item -    @3755
apb_write_paddr integral 9    'h100
apb_write_data integral 8    'h0
apb_read_paddr integral 9    'h0xxx
PSLVERR       integral 1    'h0
apb_read_data_out integral 8    'h0xx
UVM_INFO my_monitor.svh(38) @ 285000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name          Type      Size  Value
-----
seq           seq_item -    @3755
apb_write_paddr integral 9    'h101
apb_write_data integral 8    'h1
apb_read_paddr integral 9    'h0xxx
PSLVERR       integral 1    'h0
apb_read_data_out integral 8    'h0xx
UVM_INFO my_monitor.svh(38) @ 305000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name          Type      Size  Value
-----
seq           seq_item -    @3755
apb_write_paddr integral 9    'h102
apb_write_data integral 8    'h2
apb_read_paddr integral 9    'h0xxx
PSLVERR       integral 1    'h0
apb_read_data_out integral 8    'h0xx
UVM_INFO my_monitor.svh(38) @ 325000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name          Type      Size  Value
-----
seq           seq_item -    @3755
apb_write_paddr integral 9    'h103
apb_write_data integral 8    'h3
apb_read_paddr integral 9    'h0xxx
```

Fig 28: Write to Slave 2



# 5. Work done/Results

```
Activities Applications Places Terminal May 7 19:48
msis@centos:uvm

File Edit View Search Terminal Help

UVM_INFO my_driver.svh(61) @ 435000: uvm_test_top.env.agent.driver [DRIVER] DRIVING RANDOMIZED VALUES
-----
Name                               Type      Size  Value
-----
req                                seq_item  -     @3767
apb_write_paddr                    integral  9     'h2e
apb_write_data                     integral  8     'h73
apb_read_paddr                    integral  9     'h0Xxx
PSLVERR                           integral  1     'h0
apb_read_data_out                 integral  8     'h0xx
begin_time                        time      64    435000
depth                             int       32    'd2
parent sequence (name)            string    3     seq
parent sequence (full name)       string   36    uvm_test_top.env.agent.sequencer.seq
sequencer                        string    32    uvm_test_top.env.agent.sequencer
-----

UVM_INFO my_monitor.svh(38) @ 445000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name                               Type      Size  Value
-----
seq                                seq_item  -     @3755
apb_write_paddr                    integral  9     'h2e
apb_write_data                     integral  8     'h73
apb_read_paddr                    integral  9     'h0Xxx
PSLVERR                           integral  1     'h0
apb_read_data_out                 integral  8     'h0xx
-----

UVM_INFO my_driver.svh(61) @ 475000: uvm_test_top.env.agent.driver [DRIVER] DRIVING RANDOMIZED VALUES
-----
Name                               Type      Size  Value
-----
req                                seq_item  -     @3798
apb_write_paddr                    integral  9     'h39
apb_write_data                     integral  8     'hea
apb_read_paddr                    integral  9     'h0Xxx
PSLVERR                           integral  1     'h0
apb_read_data_out                 integral  8     'h0xx
begin_time                        time      64    475000
depth                             int       32    'd2
parent sequence (name)            string    3     seq
parent sequence (full name)       string   36    uvm_test_top.env.agent.sequencer.seq
sequencer                        string    32    uvm_test_top.env.agent.sequencer
-----
```

Fig 29: Driving Randomized Values





# 5. Work done/Results

```
Activities Applications Places Terminal May 7 20:03
msis@centos:uvm
File Edit View Search Terminal Help
-----
SLAVE 1 READ OPERATION 8X
UVM_INFO my_monitor.svh(38) @ 605000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name          Type      Size  Value
-----
seq            seq_item -    @3755
apb_write_paddr integral 9    'h0Xxx
apb_write_data integral 8    'h0xx
apb_read_paddr integral 9    'h1e
PSLVERR        integral 1    'h0
apb_read_data_out integral 8    'h0xx
-----
UVM_INFO my_monitor.svh(55) @ 625000: uvm_test_top.env.agent.monitor [MONITOR] Read Item received
-----
Name          Type      Size  Value
-----
seq            seq_item -    @3755
apb_write_paddr integral 9    'h0Xxx
apb_write_data integral 8    'h0xx
apb_read_paddr integral 9    'h1f
PSLVERR        integral 1    'h0
apb_read_data_out integral 8    'h0
-----
UVM_INFO my_monitor.svh(55) @ 645000: uvm_test_top.env.agent.monitor [MONITOR] Read Item received
-----
Name          Type      Size  Value
-----
seq            seq_item -    @3755
apb_write_paddr integral 9    'h0Xxx
apb_write_data integral 8    'h0xx
apb_read_paddr integral 9    'h20
PSLVERR        integral 1    'h0
apb_read_data_out integral 8    'h2
-----
UVM_INFO my_monitor.svh(55) @ 665000: uvm_test_top.env.agent.monitor [MONITOR] Read Item received
-----
Name          Type      Size  Value
-----
seq            seq_item -    @3755
apb_write_paddr integral 9    'h0Xxx
apb_write_data integral 8    'h0xx
```

Fig 30: Read from Slave 1



# 5. Work done/Results

```
Activities Applications Places Terminal May 7 20:08
msis@centos:uvm
File Edit View Search Terminal Help
-----
SLAVE 2 READ OPERATION 8X
UVM_INFO my_monitor.svh(55) @ 815000: uvm_test_top.env.agent.monitor [MONITOR] Read Item received
-----
Name          Type      Size  Value
-----
seq            seq_item -    @3755
apb_write_paddr integral 9    'h0Xxx
apb_write_data integral 8    'h0xx
apb_read_paddr integral 9    'h100
PSLVERR        integral 1    'h0
apb_read_data_out integral 8    'he
-----
UVM_INFO my_monitor.svh(55) @ 835000: uvm_test_top.env.agent.monitor [MONITOR] Read Item received
-----
Name          Type      Size  Value
-----
seq            seq_item -    @3755
apb_write_paddr integral 9    'h0Xxx
apb_write_data integral 8    'h0xx
apb_read_paddr integral 9    'h101
PSLVERR        integral 1    'h0
apb_read_data_out integral 8    'h0
-----
UVM_INFO my_monitor.svh(55) @ 855000: uvm_test_top.env.agent.monitor [MONITOR] Read Item received
-----
Name          Type      Size  Value
-----
seq            seq_item -    @3755
apb_write_paddr integral 9    'h0Xxx
apb_write_data integral 8    'h0xx
apb_read_paddr integral 9    'h102
PSLVERR        integral 1    'h0
apb_read_data_out integral 8    'h1
-----
UVM_INFO my_monitor.svh(55) @ 875000: uvm_test_top.env.agent.monitor [MONITOR] Read Item received
-----
Name          Type      Size  Value
-----
seq            seq_item -    @3755
apb_write_paddr integral 9    'h0Xxx
apb_write_data integral 8    'h0xx
```

Fig 31: Read from Slave 2



# 5. Work done/Results

```
OSDLERROR: (null)/top/sv/ sv_export.so: cannot open shared object file: No such file or directory or file is not valid ELFCLASS64 library..
ncsim: *W,DSEM2009: This SystemVerilog design is simulated as per IEEE 1800-2009 SystemVerilog simulation semantics. Use -disable_sem2009 option for turning off SV 2009 simulation semantics.
ncsim> source /home/installs/INCISIVE152/tools/inca/files/ncsimrc
ncsim> source /home/installs/INCISIVE152/tools/methodology/UVM/CDNS-1.1d/additions/sv/files/tcl/uvm_sim.tcl
ncsim> run

-----
CDNS-UVM-1.1d (15.20-s086)
(C) 2007-2013 Mentor Graphics Corporation
(C) 2007-2013 Cadence Design Systems, Inc.
(C) 2006-2013 Synopsys, Inc.
(C) 2011-2013 Cypress Semiconductor Corp.
-----

***** IMPORTANT RELEASE NOTES *****

You are using a version of the UVM library that has been compiled
with 'UVM_NO_DEPRECATED' undefined.
See http://www.eda.org/svdb/view.php?id=3313 for more details.

You are using a version of the UVM library that has been compiled
with 'UVM_OBJECT_MUST_HAVE_CONSTRUCTOR' undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.

(Specify +UVM_NO_RELNOTES to turn off this notice)

UVM_INFO @ 0: reporter [RNTST] Running test my_test...
UVM_INFO my_monitor.svh(38) @ 85000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name                Type      Size  Value
-----
seq                  seq_item  -      @3755
  apb_write_paddr     integral  9      'h22
  apb_write_data      integral  8      'h0xx
  apb_read_paddr      integral  9      'h0Xxx
  PSLVERR             integral  1      'h1
  apb_read_data_out   integral  8      'h0xx
-----
Simulation complete via $finish(1) at time 105 NS + 0
./my_driver.svh:88          $finish;
ncsim> exit
[msis@centos uvm]$
```

Fig 32: Invalid write data



# 5. Work done/Results

```
OSDLERROR: (null)/top/sv/ sv_export.so: cannot open shared object file: No such file or directory or file is not valid ELFCLASS64 library..
ncsim: *W,DSEM2009: This SystemVerilog design is simulated as per IEEE 1800-2009 SystemVerilog simulation semantics. Use -disable_sem2009 option for turning off SV 2009 simulation semantics.
ncsim> source /home/installs/INCISIVE152/tools/inca/files/ncsimrc
ncsim> source /home/installs/INCISIVE152/tools/methodology/UVM/CDNS-1.1d/additions/sv/files/tcl/uvm_sim.tcl
ncsim> run

-----
CDNS-UVM-1.1d (15.20-s086)
(C) 2007-2013 Mentor Graphics Corporation
(C) 2007-2013 Cadence Design Systems, Inc.
(C) 2006-2013 Synopsys, Inc.
(C) 2011-2013 Cypress Semiconductor Corp.
-----

***** IMPORTANT RELEASE NOTES *****

You are using a version of the UVM library that has been compiled
with 'UVM_NO_DEPRECATED' undefined.
See http://www.eda.org/svdb/view.php?id=3313 for more details.

You are using a version of the UVM library that has been compiled
with 'UVM_OBJECT_MUST_HAVE_CONSTRUCTOR' undefined.
See http://www.eda.org/svdb/view.php?id=3770 for more details.

(Specify +UVM_NO_RELNOTES to turn off this notice)

UVM_INFO @ 0: reporter [RNTST] Running test my_test...
UVM_INFO my_monitor.svh(38) @ 35000: uvm_test_top.env.agent.monitor [MONITOR] Written Item received
-----
Name                Type      Size  Value
-----
seq                  seq_item  -      @3755
  apb_write_paddr    integral  9      'h0Xxx
  apb_write_data     integral  8      'h0xx
  apb_read_paddr     integral  9      'h0Xxx
  PSLVERR            integral  1      'h1
  apb_read_data_out  integral  8      'h0xx
-----
Simulation complete via $finish(1) at time 45 NS + 0
./my_driver.svh:58          $finish;
ncsim> exit
[msis@centos uvm]$
```

Fig 33: Invalid Write address





# 5. Work done/Results

```
UVM_INFO my_monitor.svh(55) @ 95000: uvm_test_top.env.agent.monitor [MONITOR] Read Item received
-----
Name                Type      Size  Value
-----
seq                 seq_item  -    @3755
apb_write_paddr     integral  9    'h0xxx
apb_write_data      integral  8    'h0xx
apb_read_paddr      integral  9    'h0xxx
PSLVERR             integral  1    'h1
apb_read_data_out   integral  8    'h0xx
-----
Simulation complete via $finish(1) at time 105 NS + 0
./my_driver.svh:74      $finish;
ncsim> exit
[msis@centos uvm]$
[msis@centos uvm]$
```

Fig 34: Invalid Read address



# 5. Work done/Results

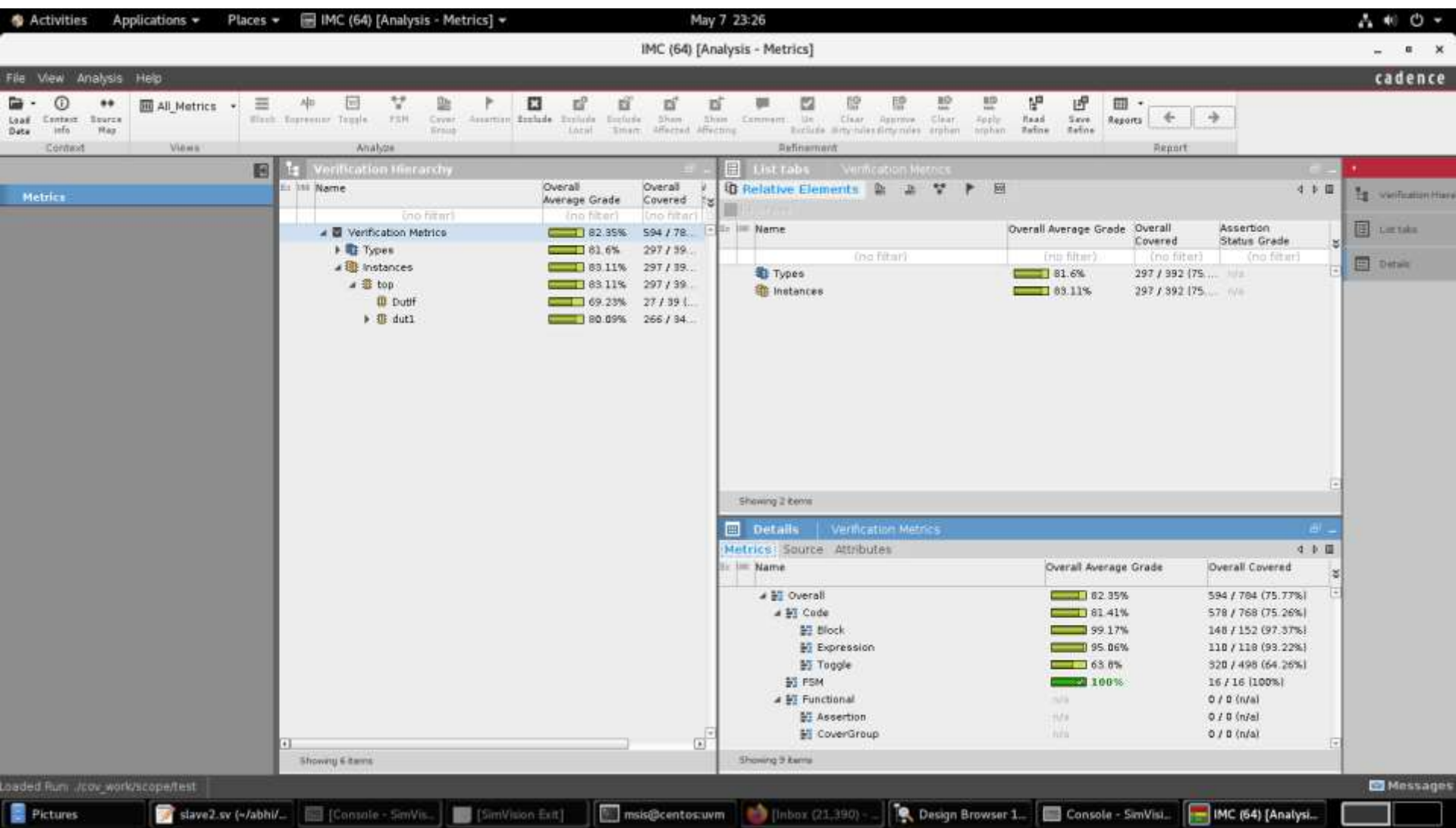


Fig 35: Verification Metrics



# 5. Work done/Results

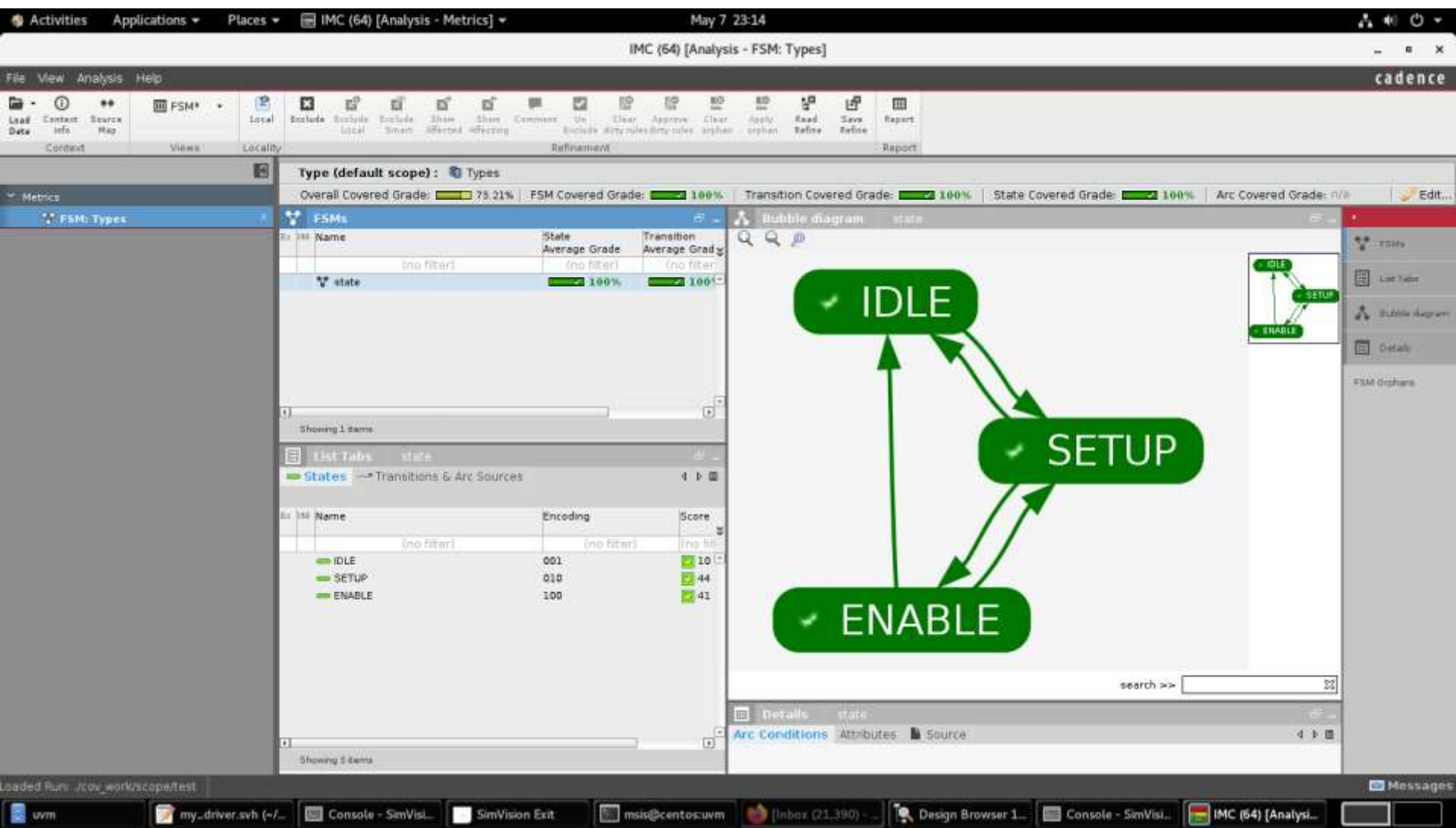


Fig 36: FSM Coverage



## 6. Conclusion

- Physical Design implemented for the design by creating macros for both the slaves and optimizing the design complexity.
- Verified using Universal Verification Methodology (UVM) and verification metrics generated.



# 7. References

- AMBA APB Protocol Specification – ARM
- Verification of Advanced Peripheral Bus Protocol (APB V2.0) - Meghana Jain H K1, Dr. Punith Kumar M B, Student, Professor, Dept of Electronics and Communication Engineering, P.E.S College of Engineering, Karnataka, India





THANK YOU...