UVM based Verification & Physical Design of APB Bridge

by

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Presentation Outline

1. Introduction
2. Objectives
3. Block Diagram
4. FSM
5. Work done/Results
6. Conclusion
7. References

1. Introduction

- Advanced Peripheral Bus (APB) - Connects peripheral devices to a CPU in embedded systems.
- Highly configurable and allow multiple devices on a single bus.
- Compatible with other bus-based protocols.
- Widespread use highlights its value in electronics and computing.

2. Objectives

1. To verify RTL design code associated with APB bridge using Universal Verification Methodology.
2. To obtain Physical Design of APB bridge.

3. Block Diagram

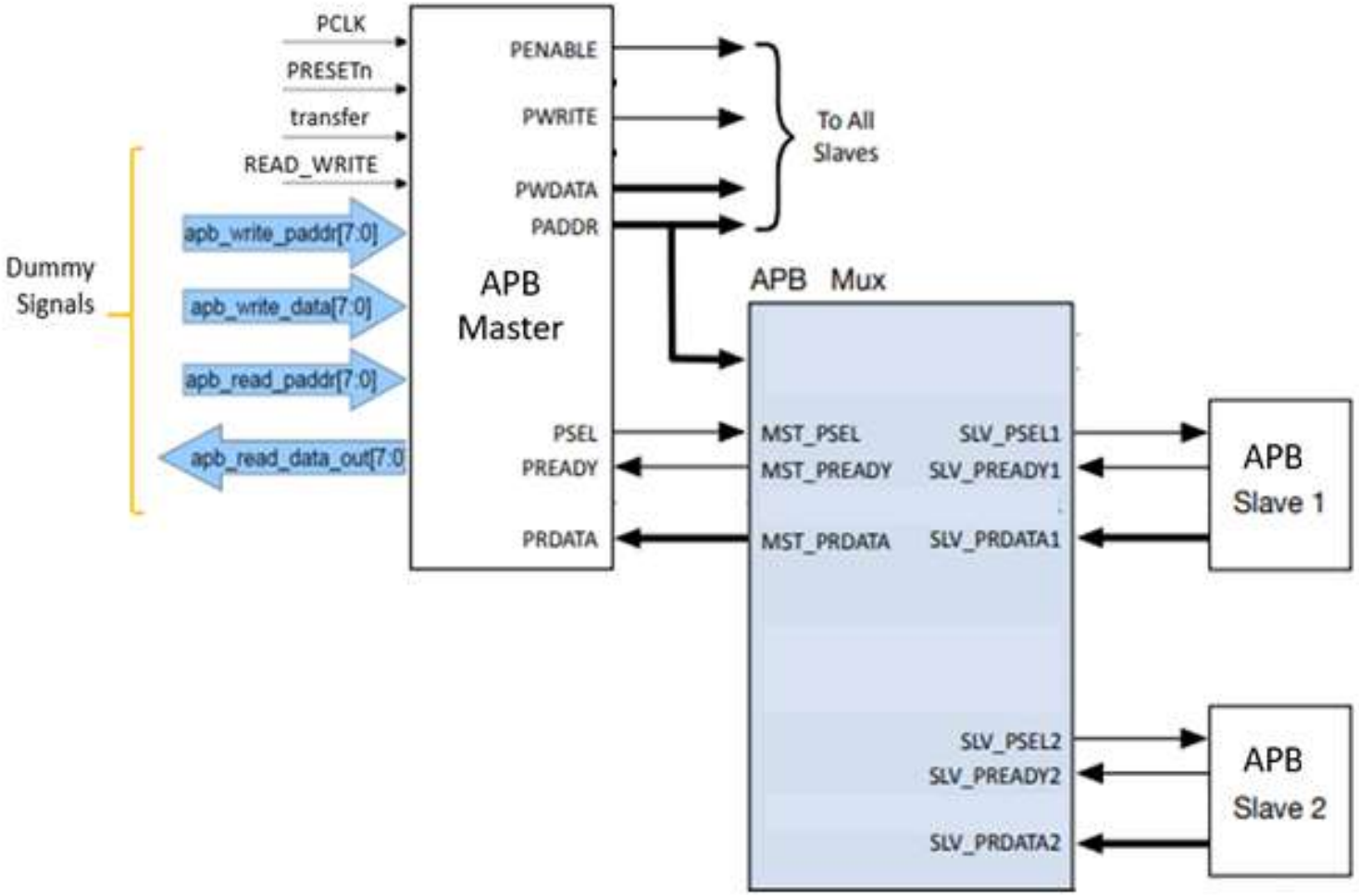

Figure 1: APB interface diagram

4. FSM

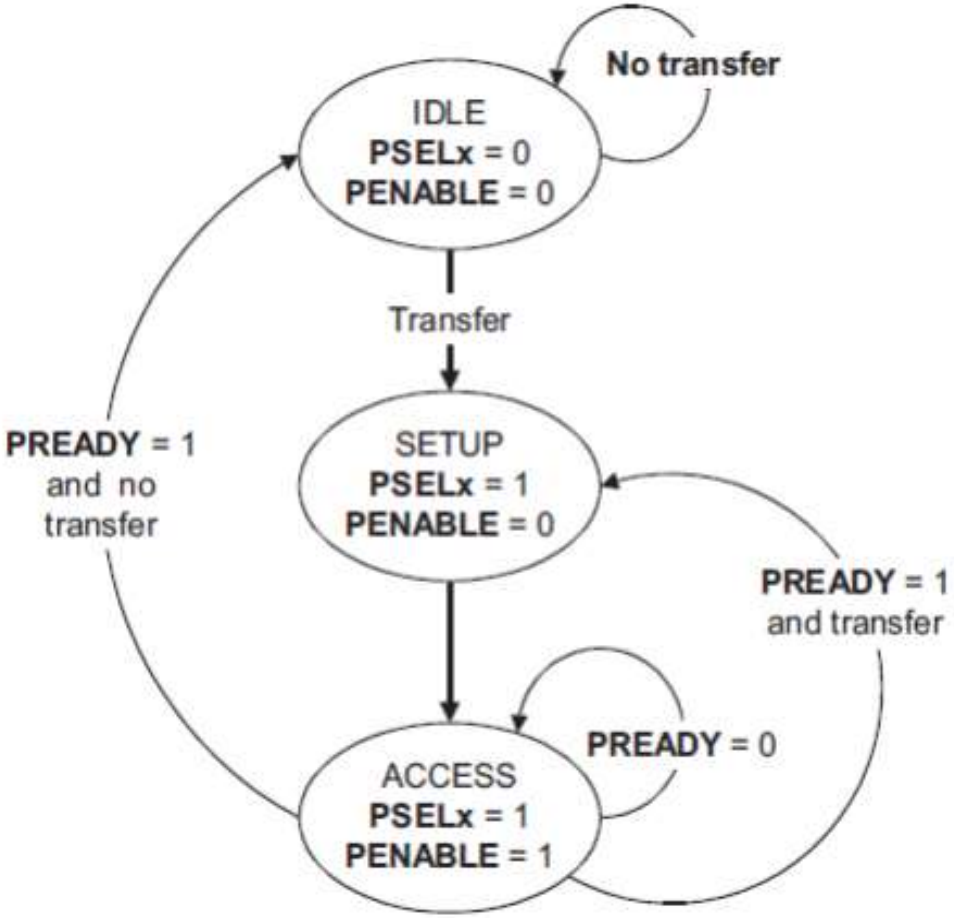

Figure 2: FSM states

5. Work done/Results

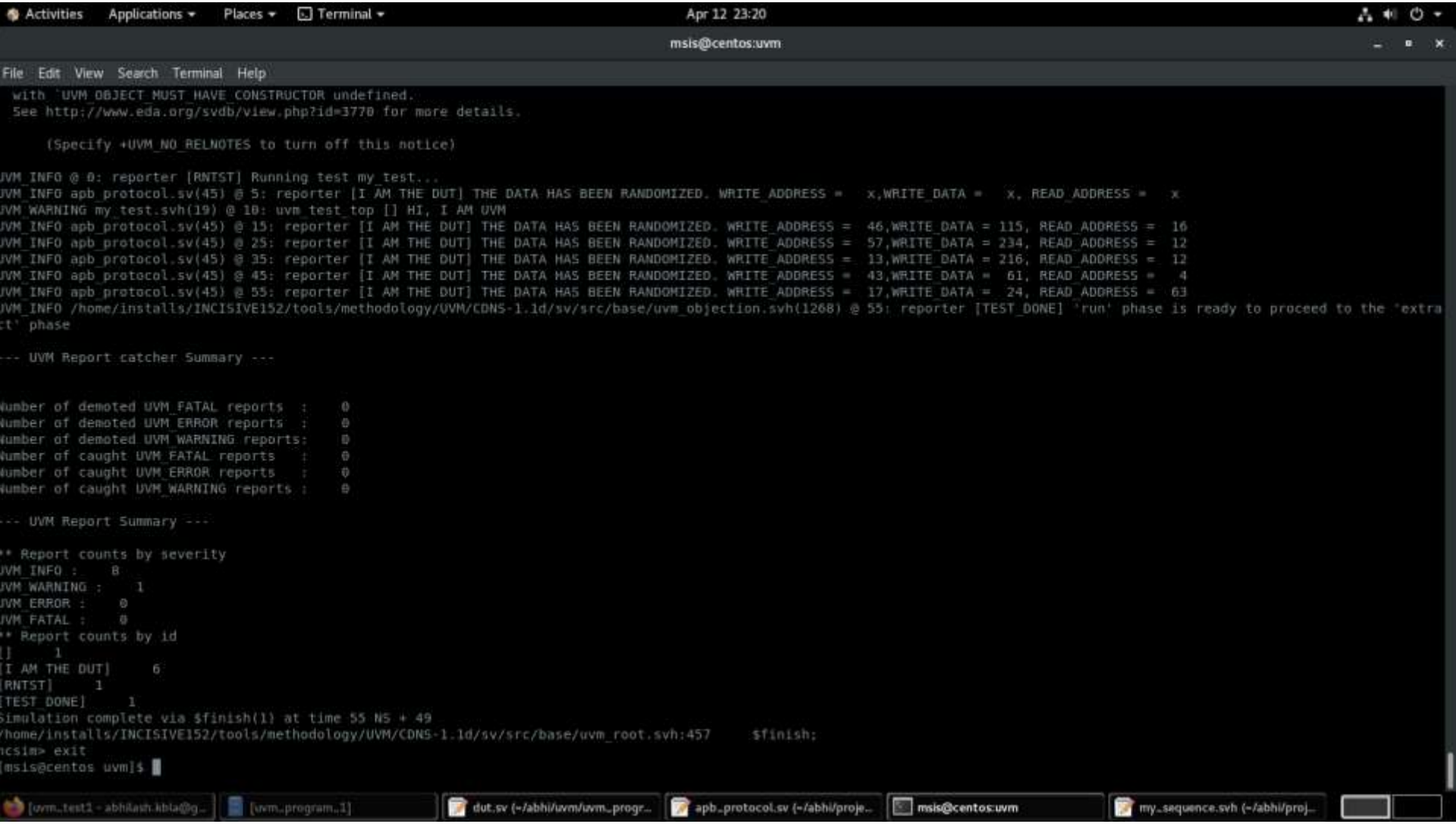

Fig 3: Previous UVM report summary

5. Work Done/Results

Sl.no	Operation type	Test case
1	Normal Operation Testing	Write on to the slave -1 (8x i.e contiguous memory)
2		Write on to the slave -2 (8x)
3		Write using generated random data
4		Read from Slave 1
5		Read from Slave 2
6	Error injection	Write transfer without write address
7		Read transfer without read address
8		Write transfer without valid write data

Table 1: Test cases for verification (UVM)

5. Work done/Results

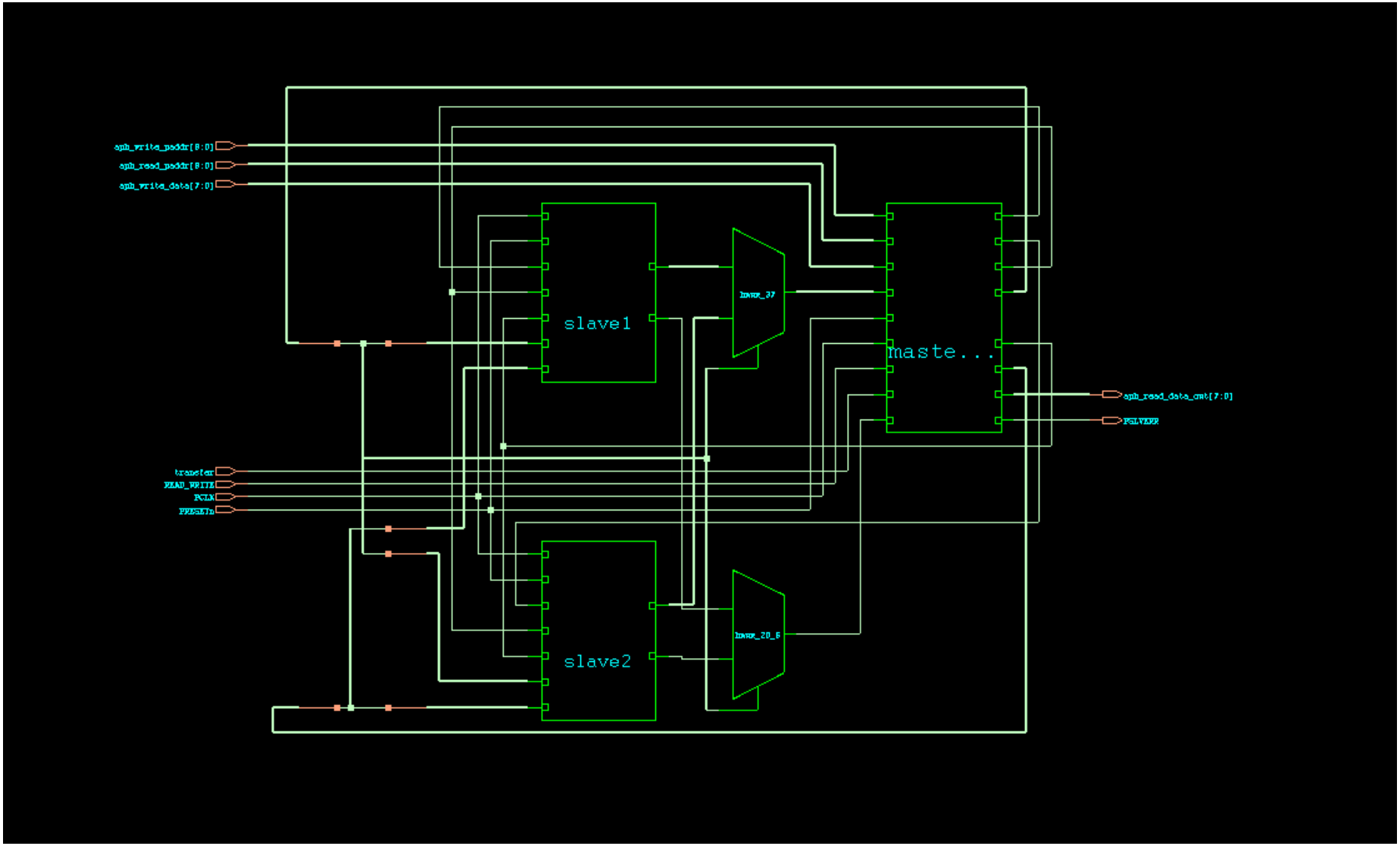

Fig 4: Previous GUI schematic

5. Work done/Results

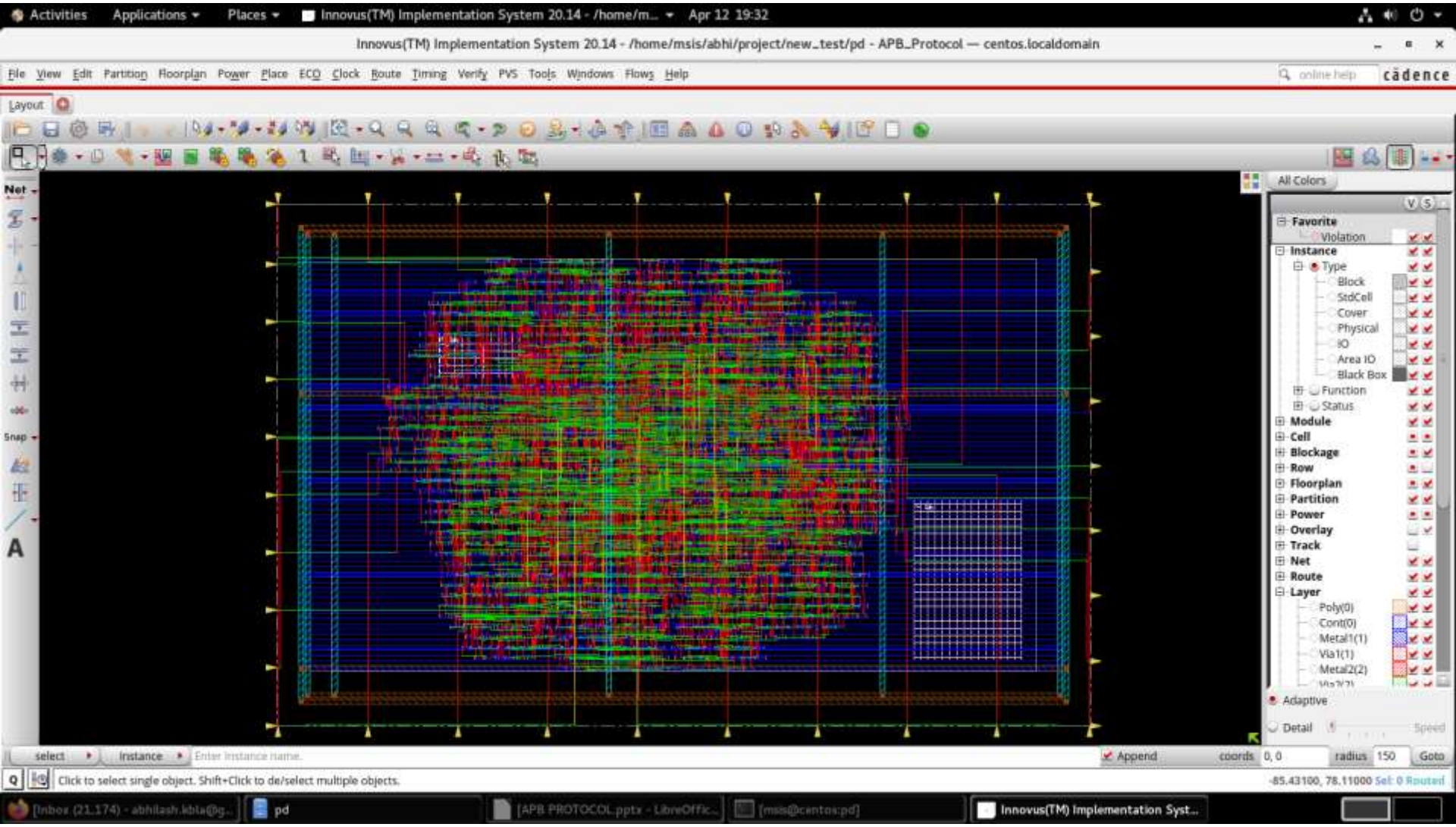

Fig 5: Previous Physical Design

5. Work done/Results

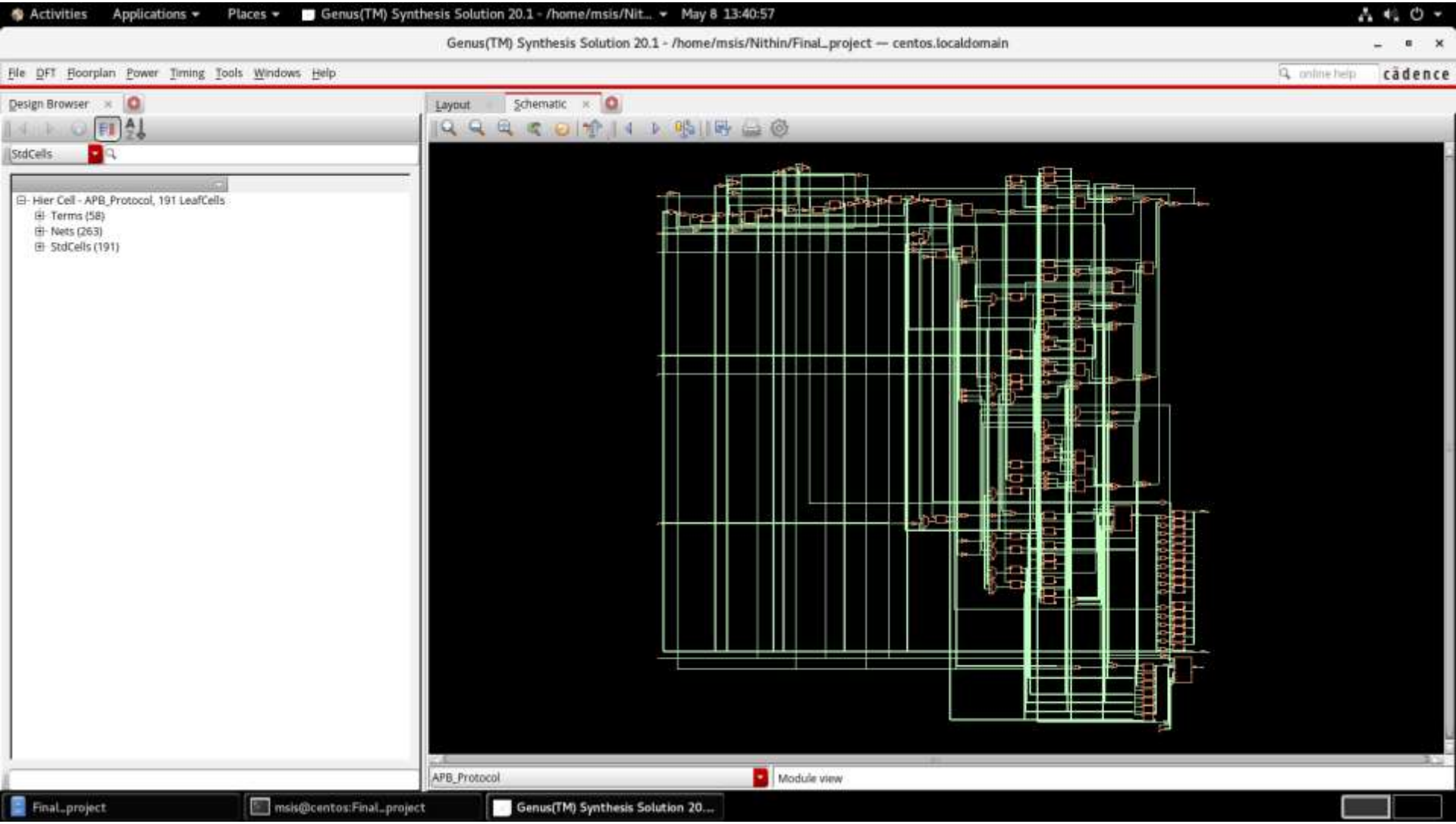

Fig 6: GUI schematic

5. Work done/Results

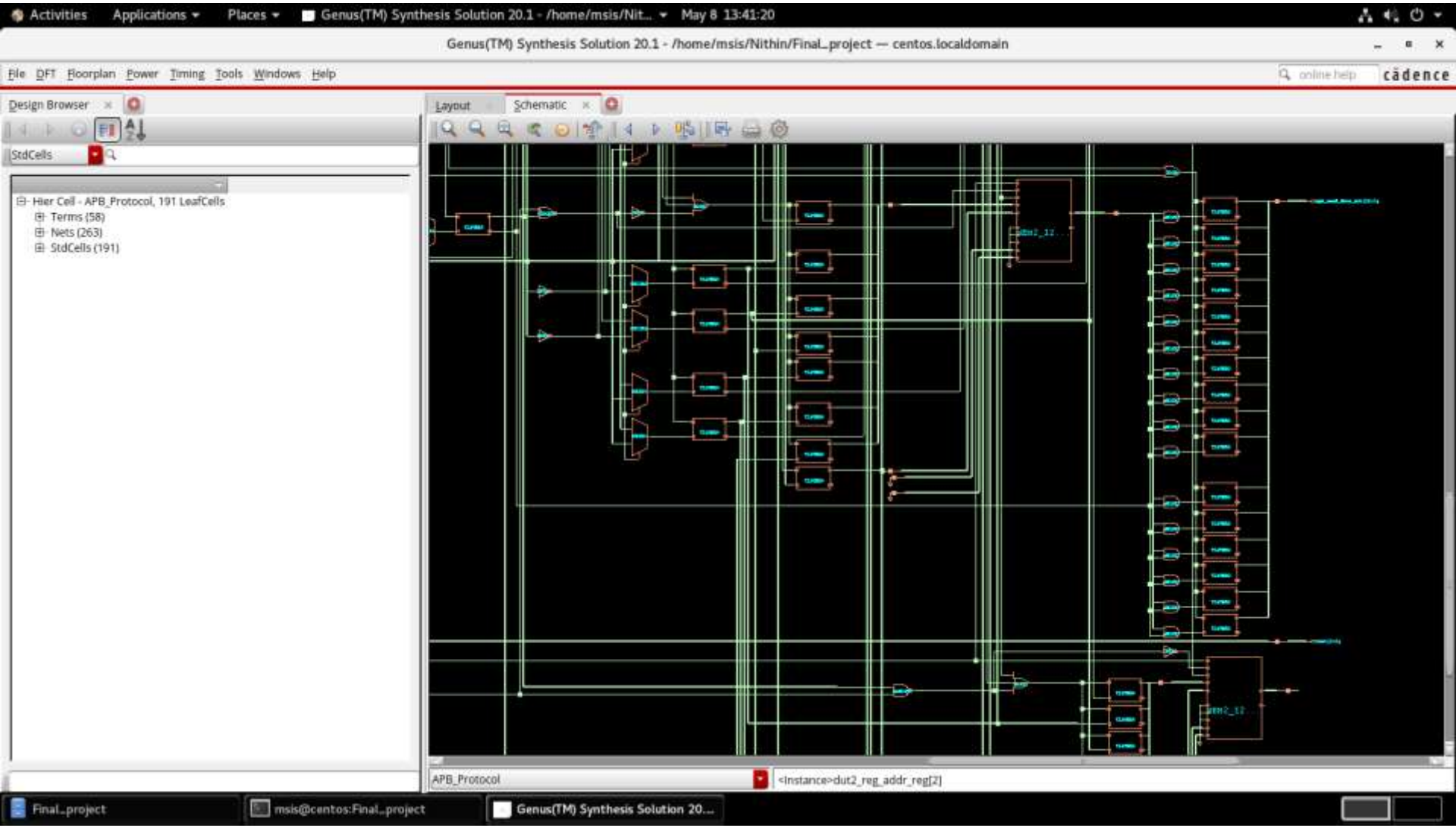

Fig 7: GUI schematic displaying Memory blocks

5. Work done/Results

constraint.sdc

File Edit View

```
create_clock -name PCLK -period 20 [get_ports PCLK]
set_input_delay -clock PCLK -max 3 <apb_write_data>
set_output_delay -clock PCLK -max 3 <apb_read_data_out>
set_clock_uncertainity 1 [get_clocks PCLK]
```

Property	Value
Library	fast.lib MEM2_128X16.lib
Clock frequency	50MHz
Area	1,00,000 squm
Slack	19336.2ps
Cell count	191

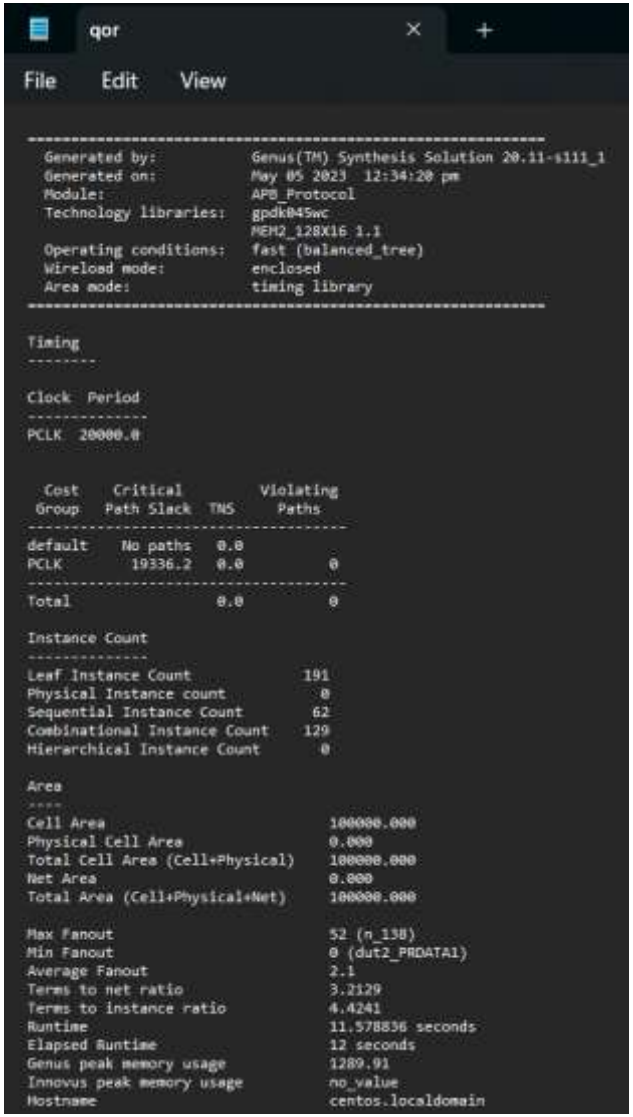

Fig 8: Constraints and Report summary

5. Work done/Results

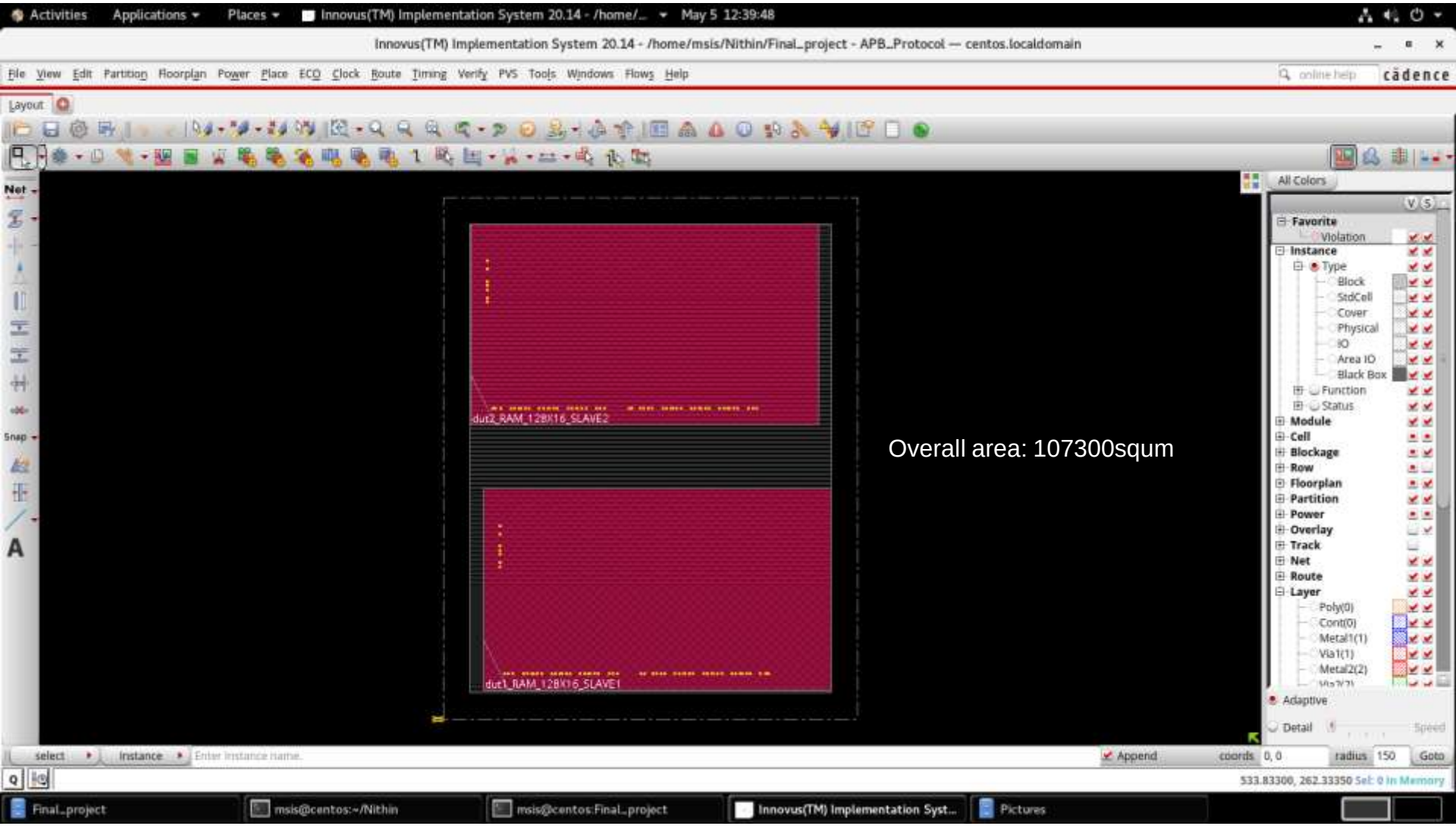

Fig 9: Floor planning

5. Work done/Results

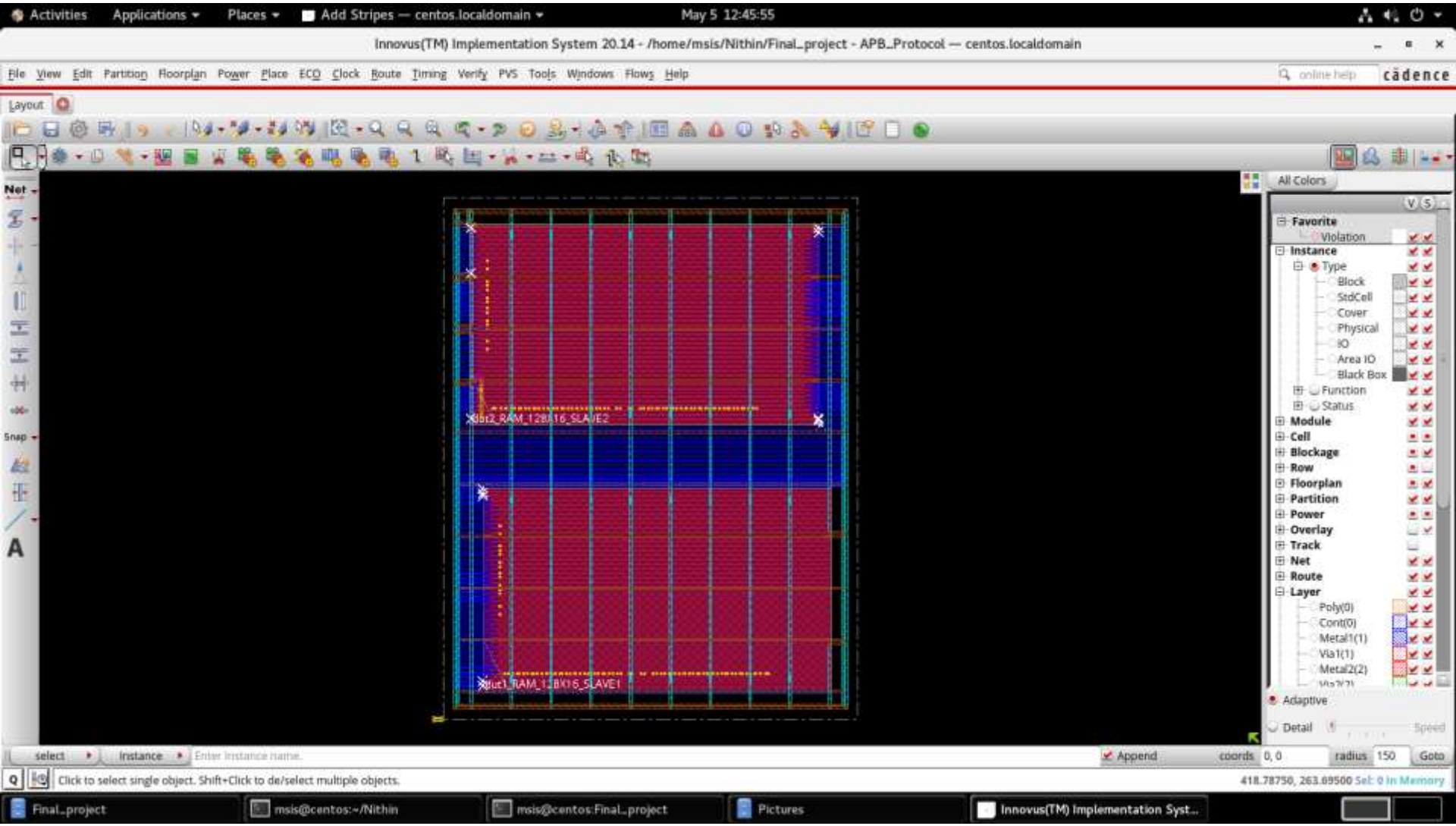

Fig 10: Power planning

5. Work done/Results

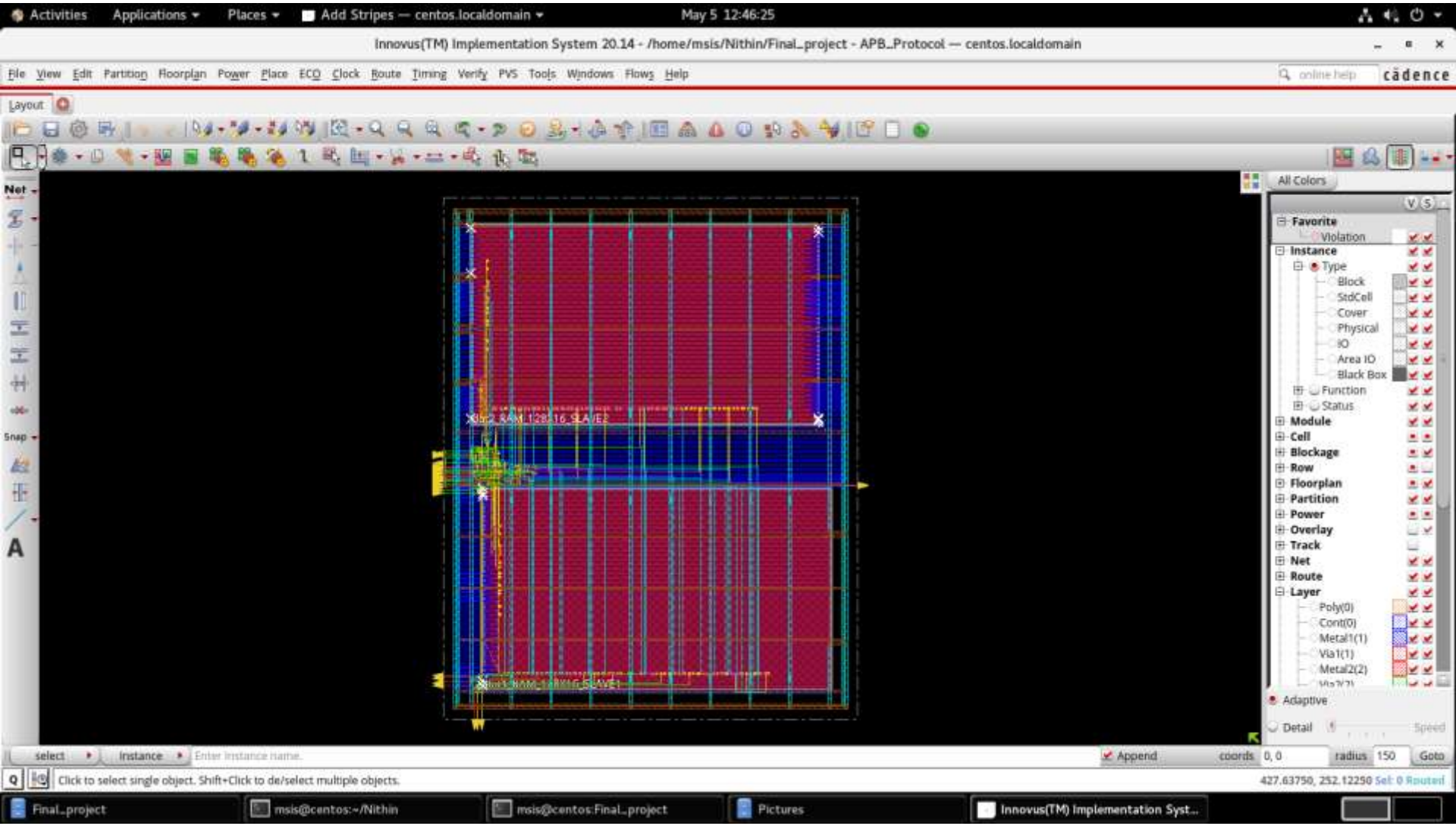

Fig 11: Standard cell placement with wiring

5. Work done/Results

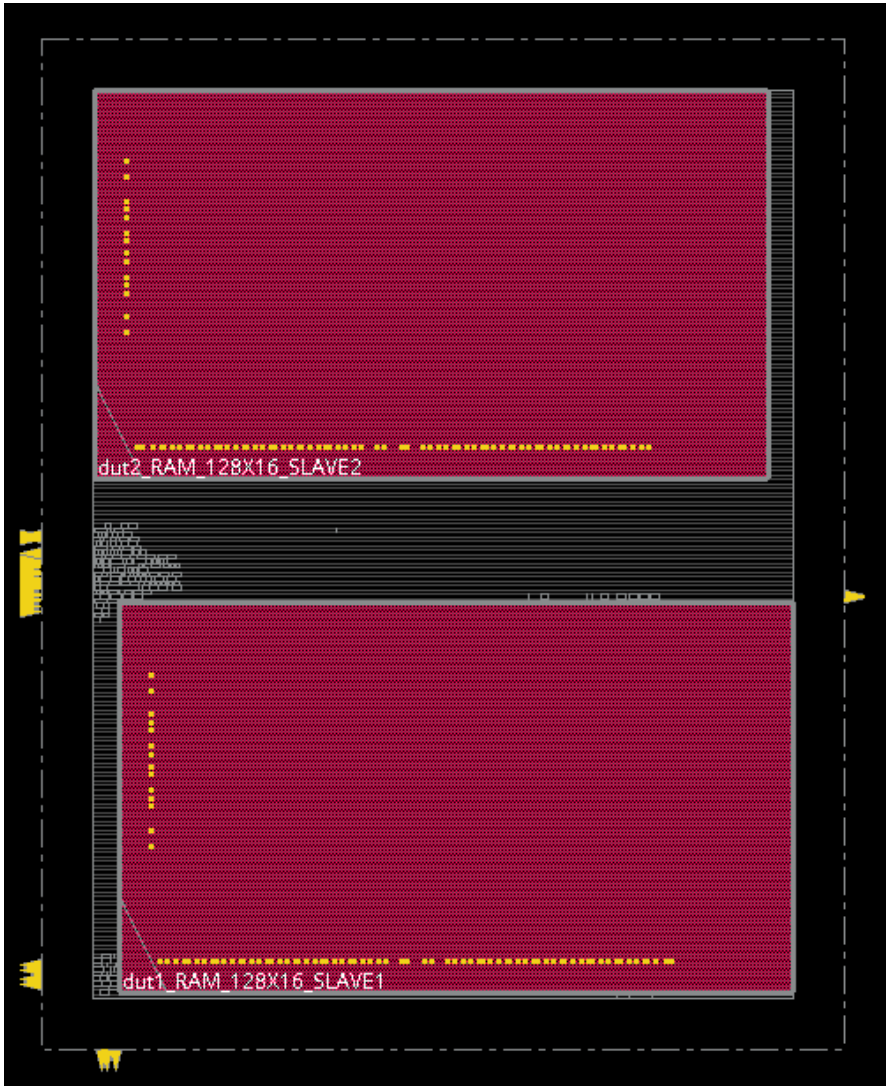

Fig 12: Standard cells placement

5. Work done/Results

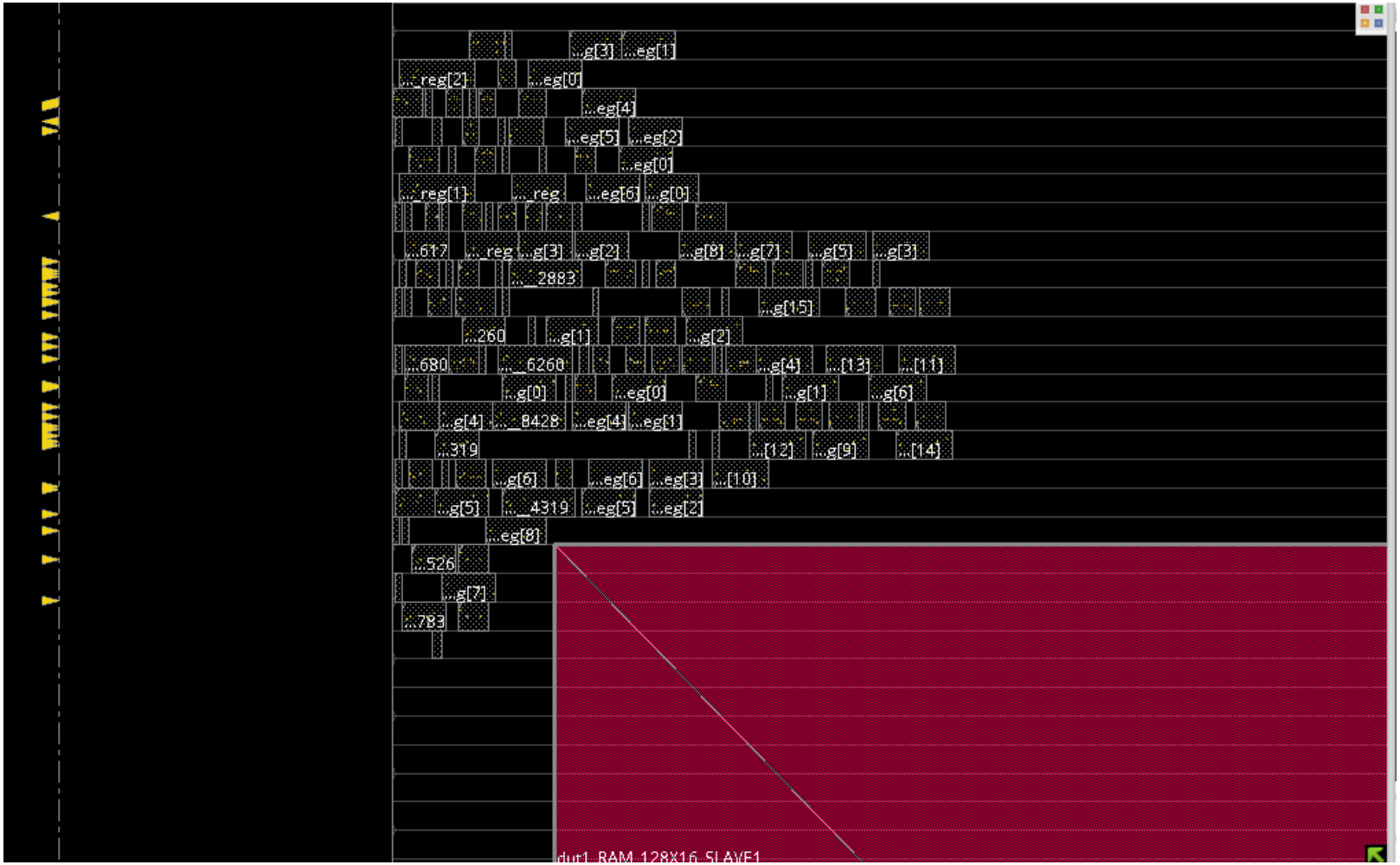

Fig 13: Standard cells placement

5. Work done/Results

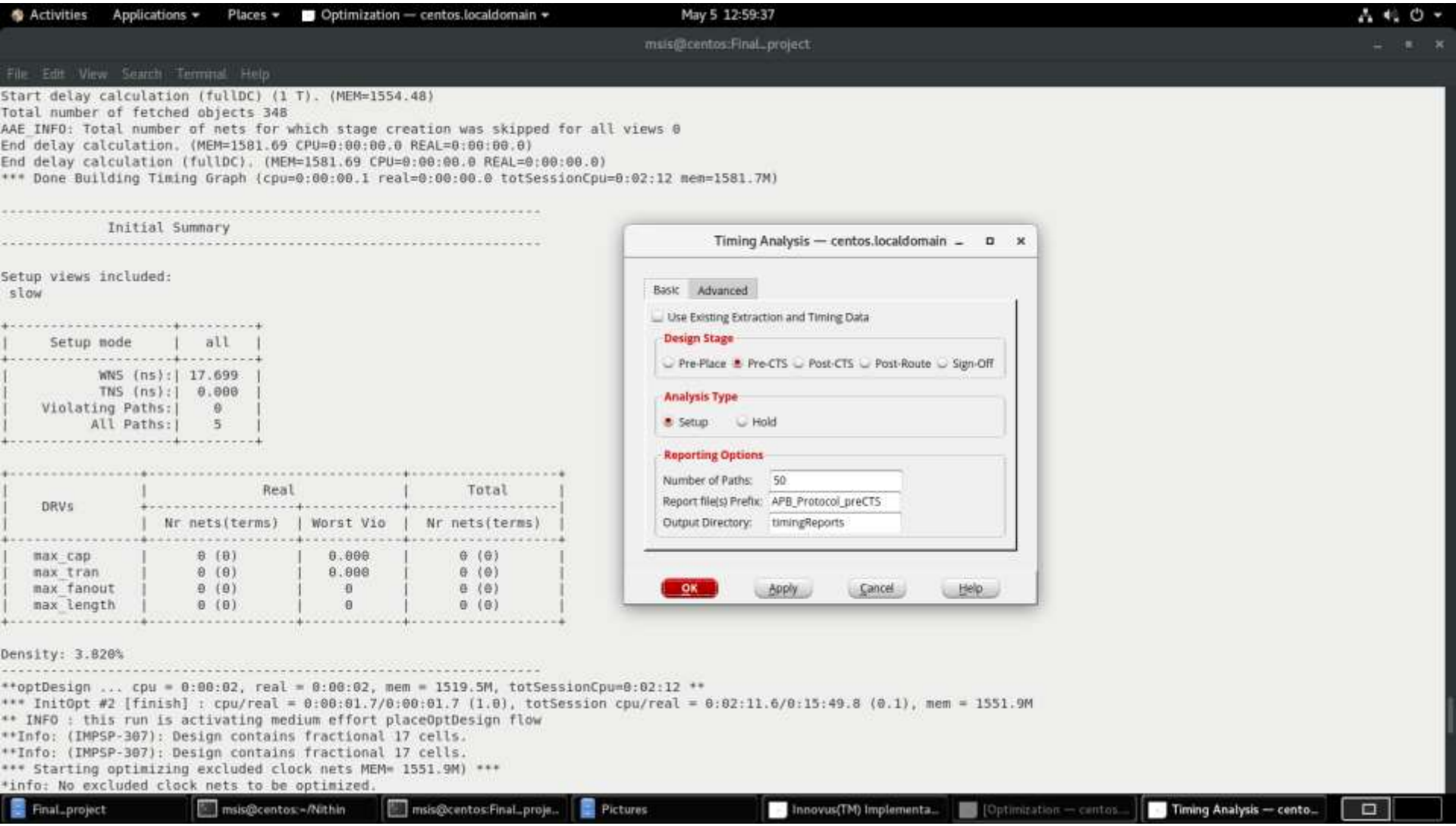

Fig 14: Pre-CTS setup timing report

5. Work done/Results

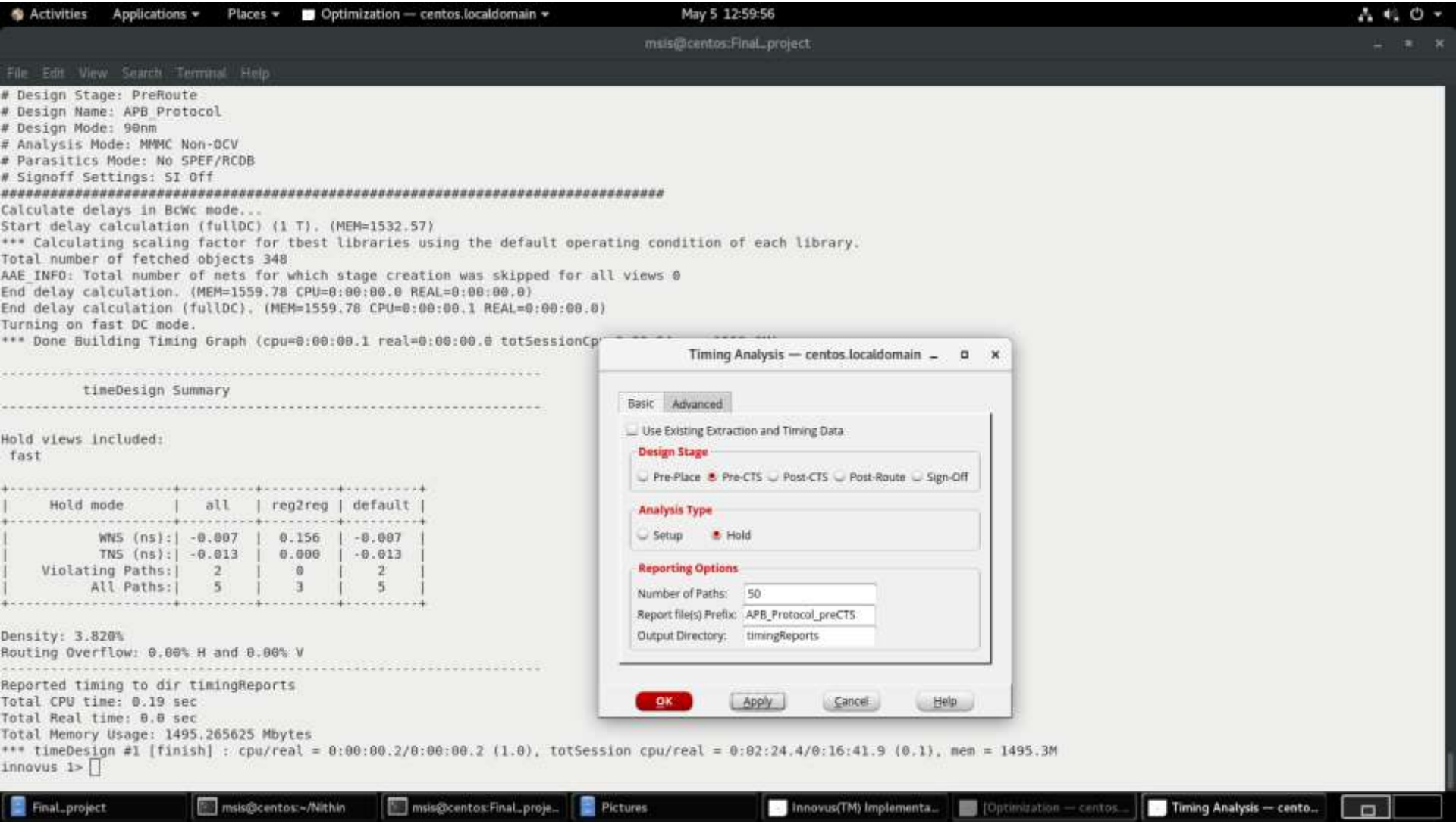

Fig 15: Pre-CTS hold timing report

5. Work done/Results

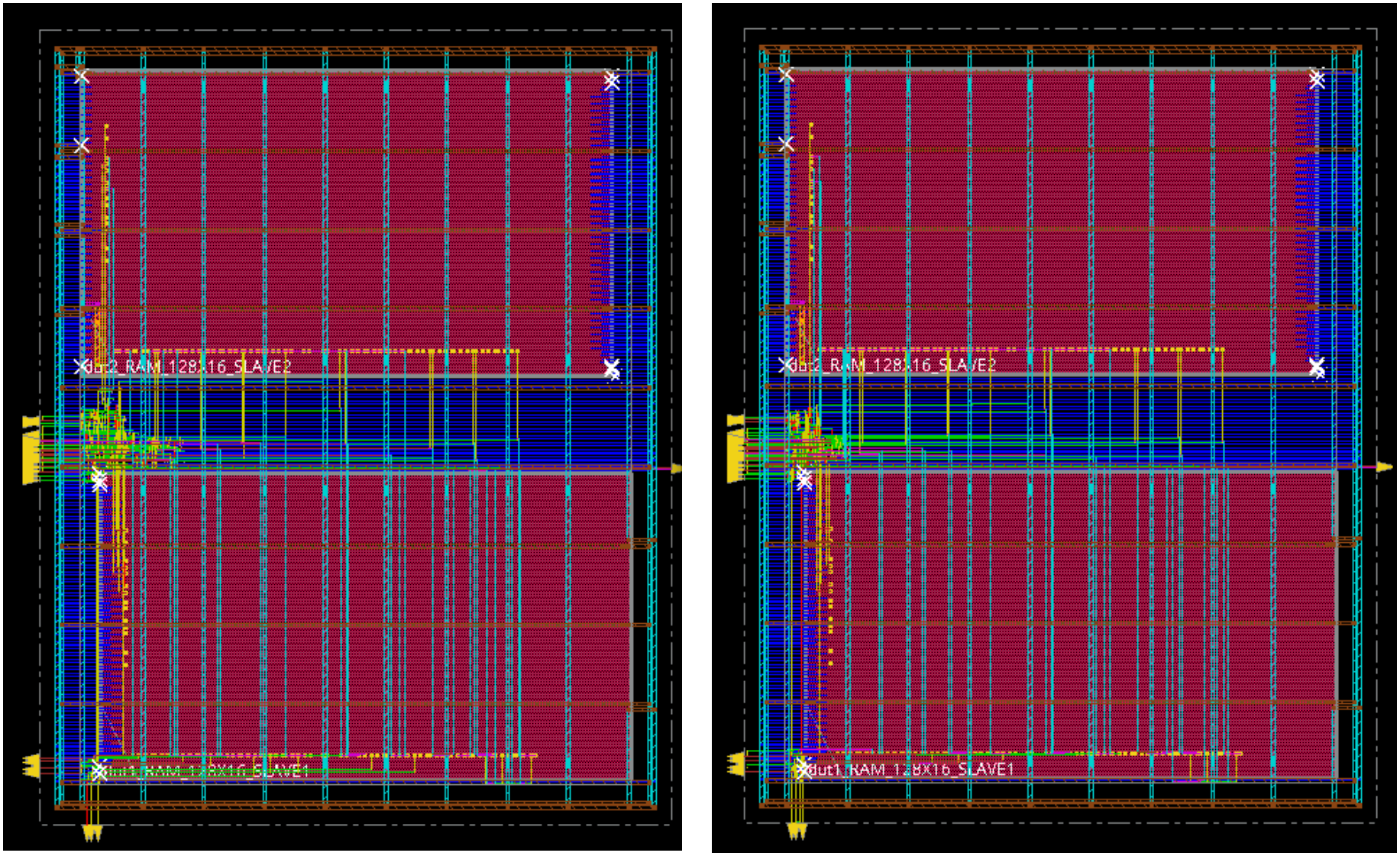

Fig 16: Pre & Post CTS design Optimization changes

5. Work done/Results

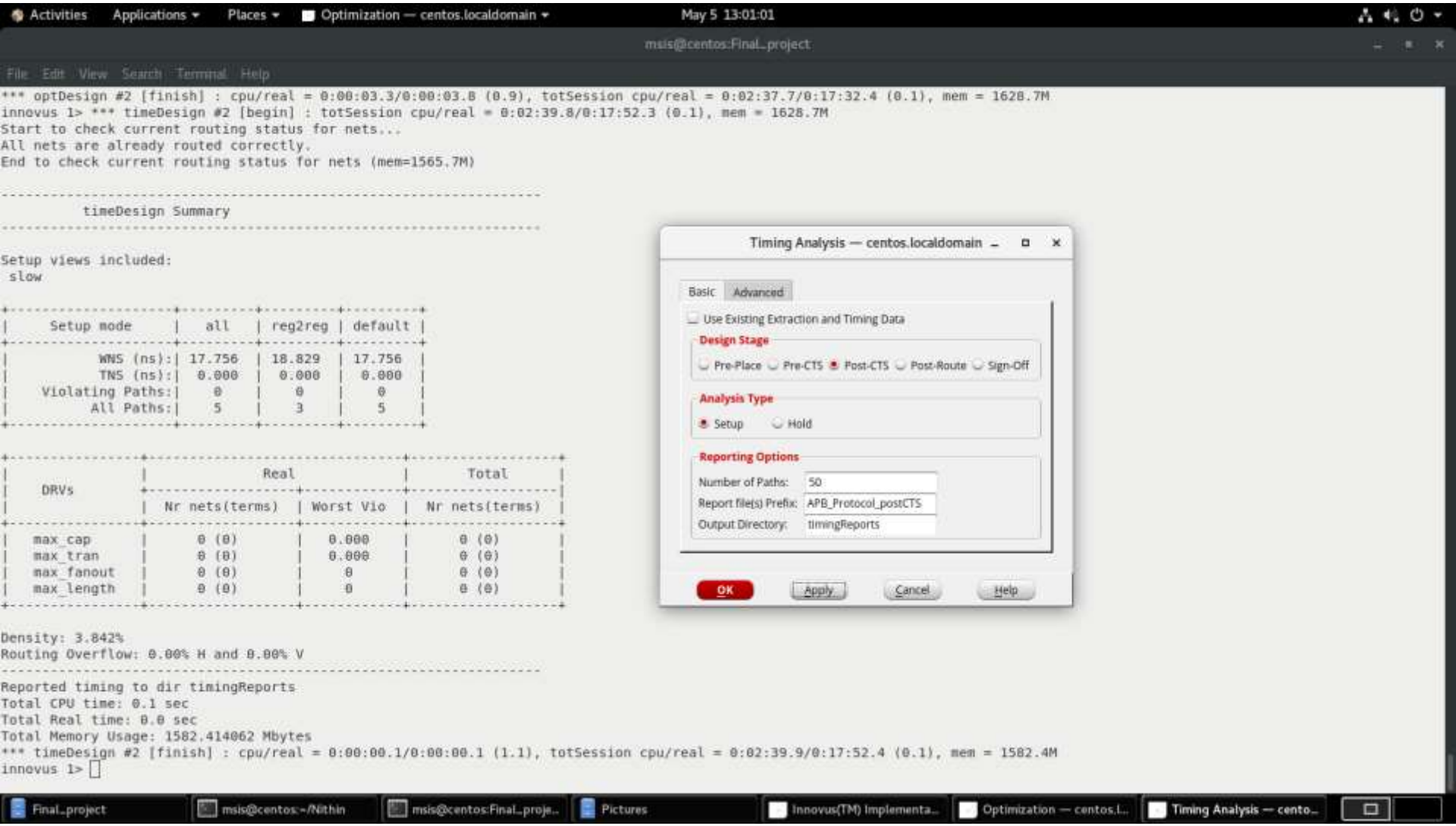

Fig 17: Post-CTS setup timing report

5. Work done/Results

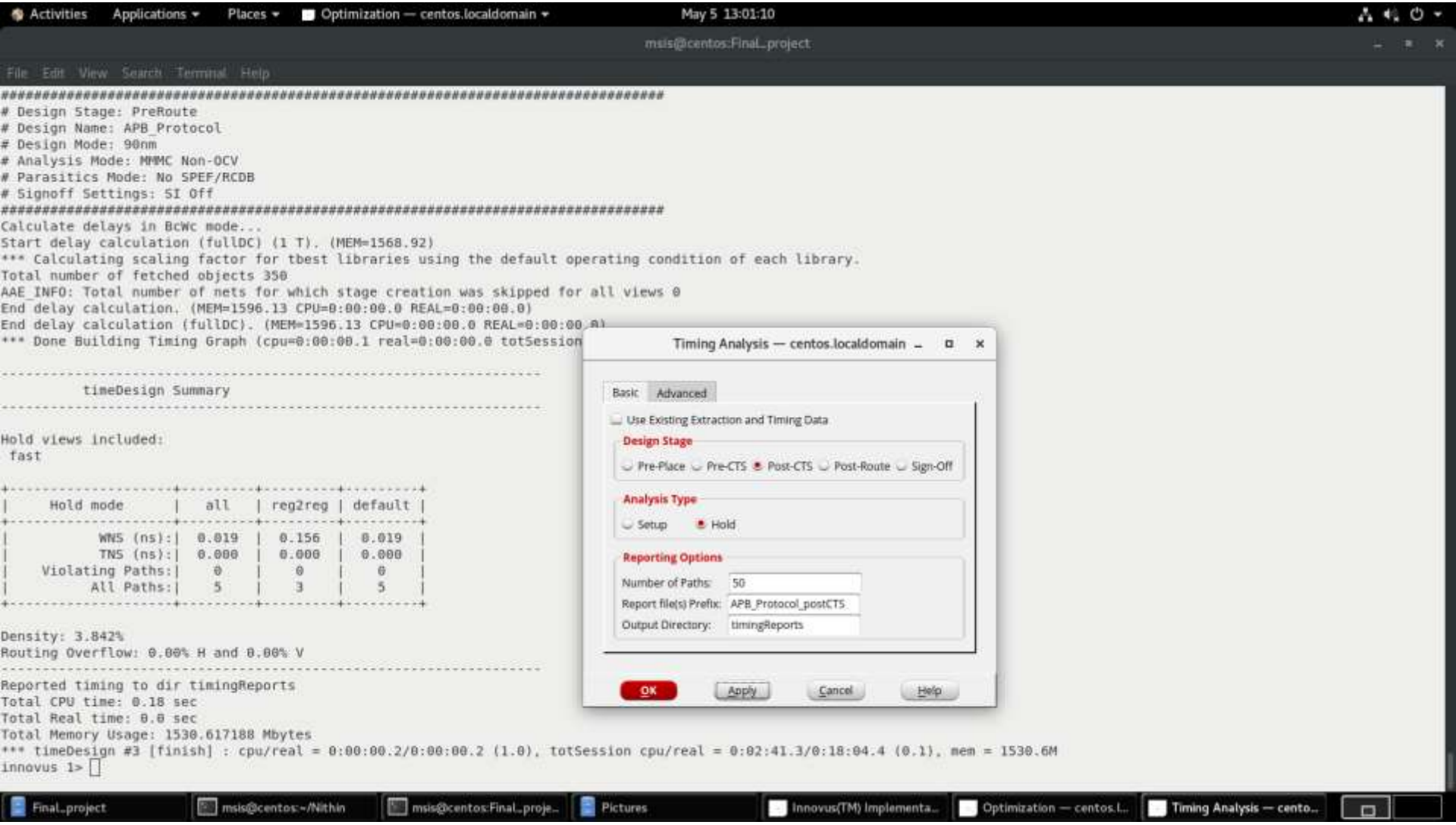

Fig 18: Post-CTS hold timing report

5. Work done/Results

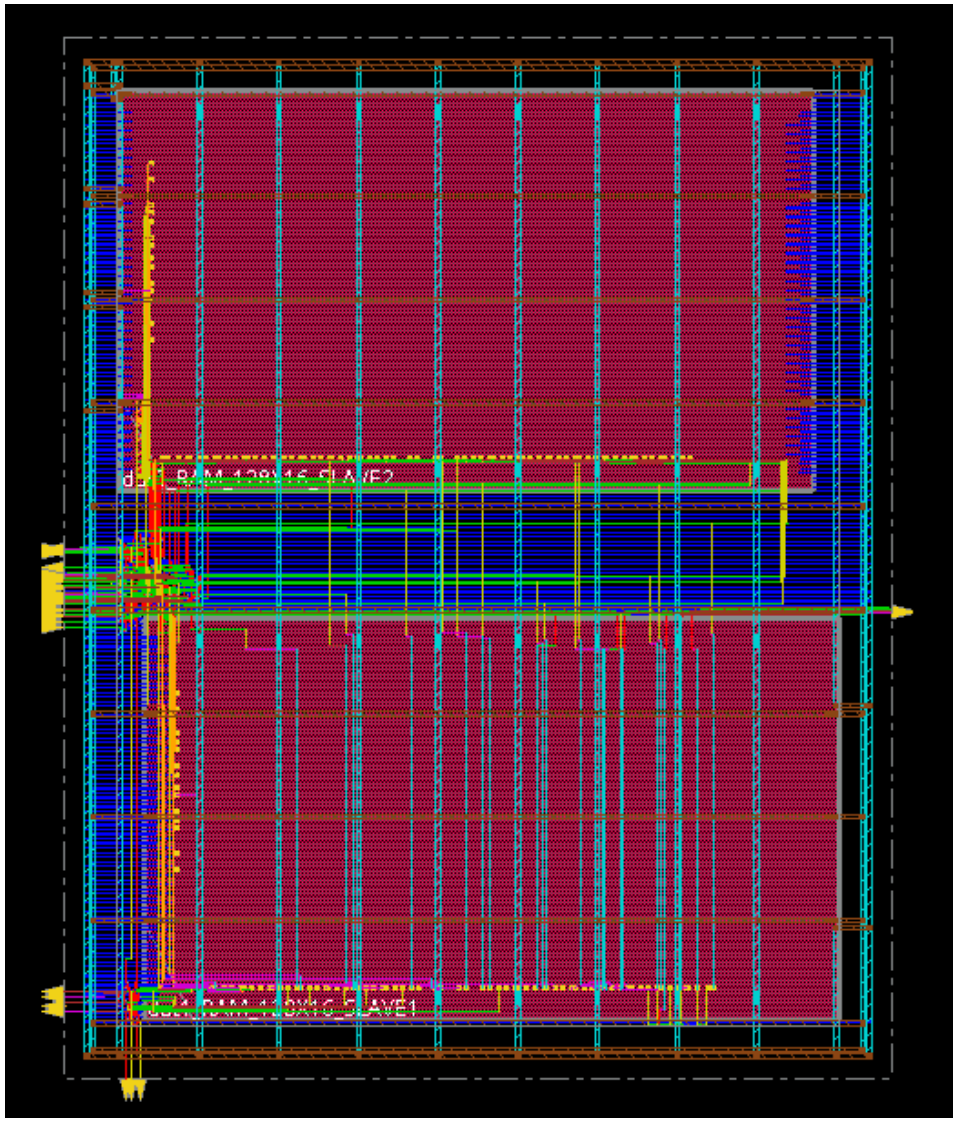

Fig 19: Post Routing

5. Work done/Results

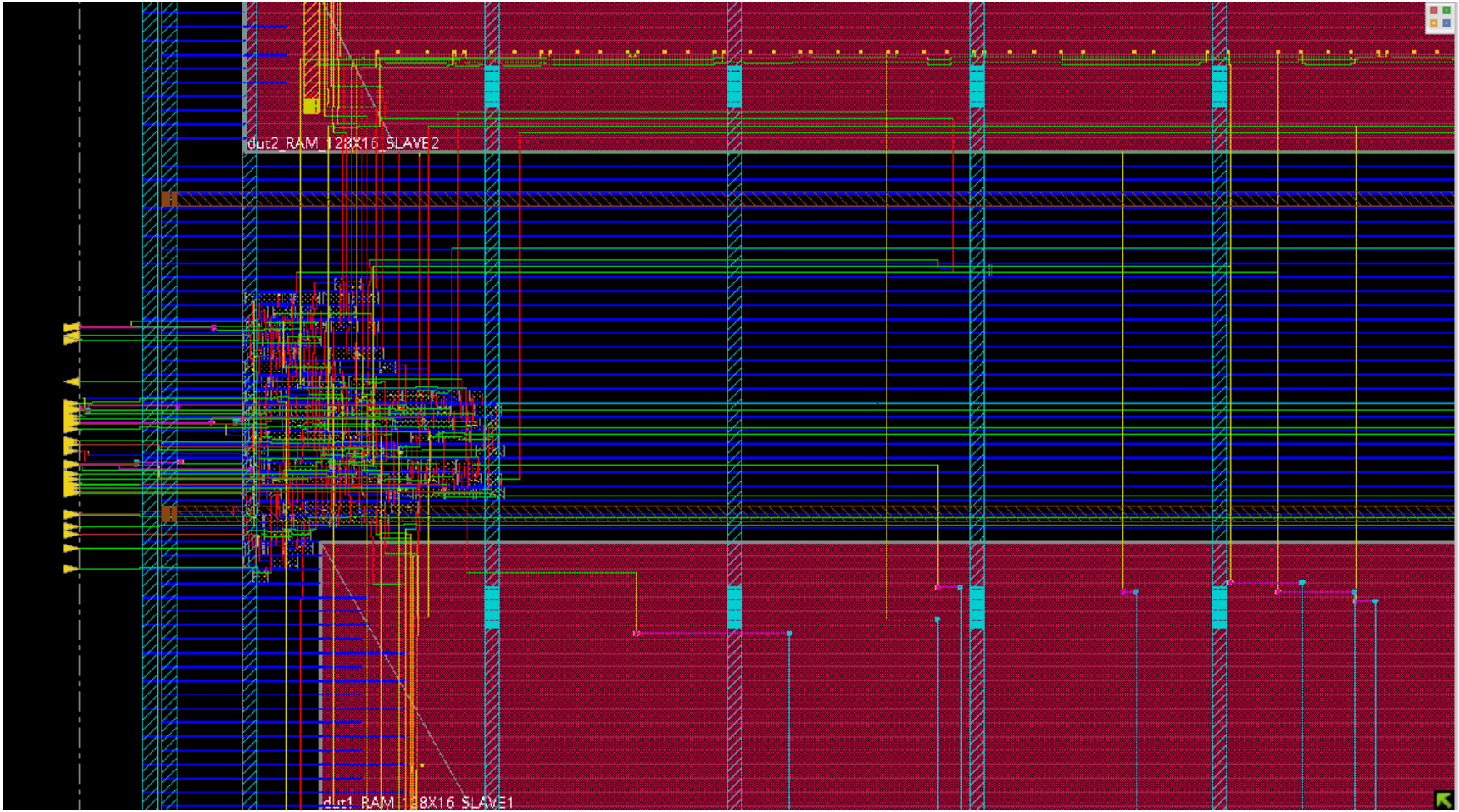

Fig 20: Post Routing standard cell connection close up

5. Work done/Results

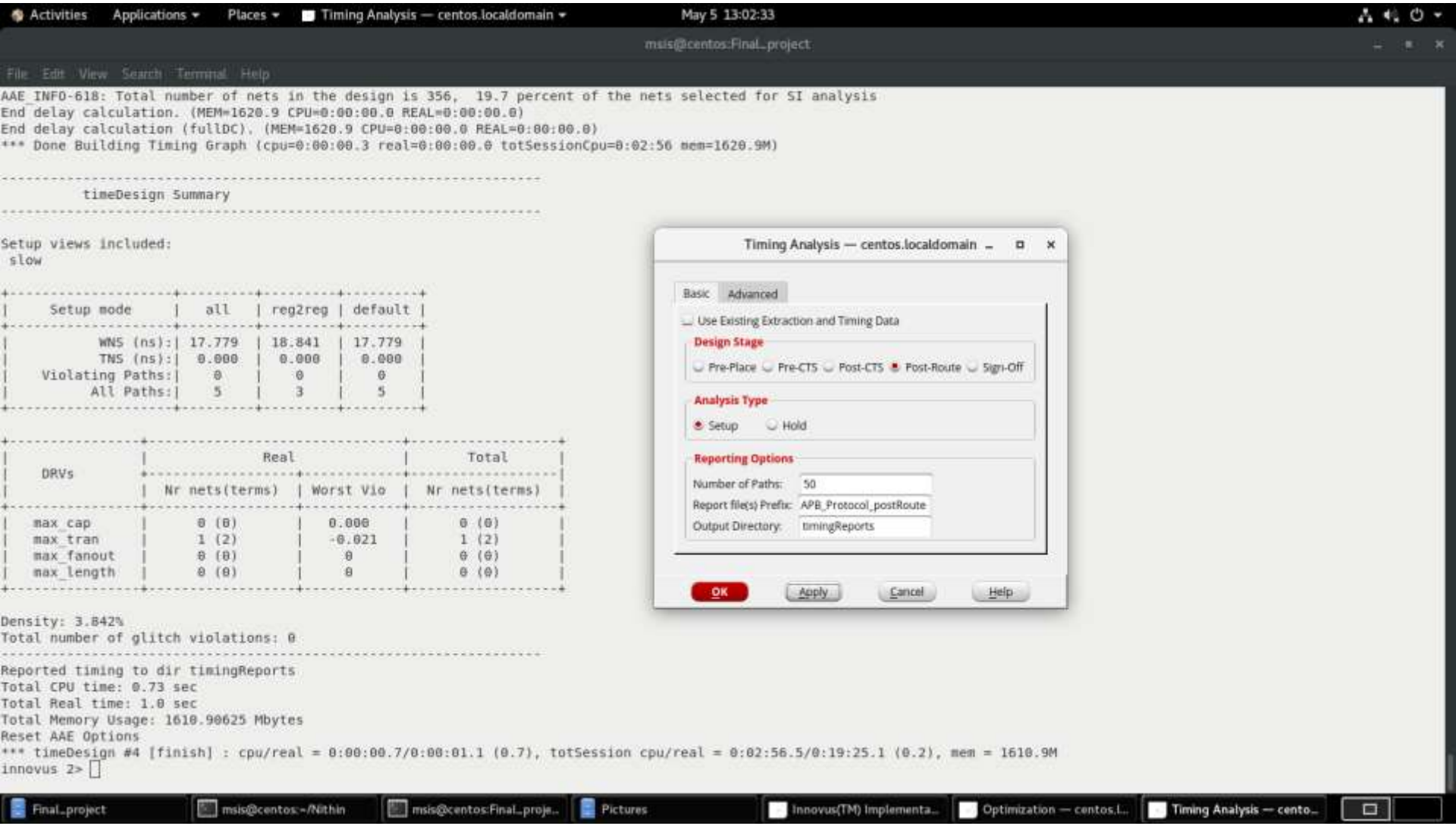

Fig 21: Post Routing setup timing report

5. Work done/Results

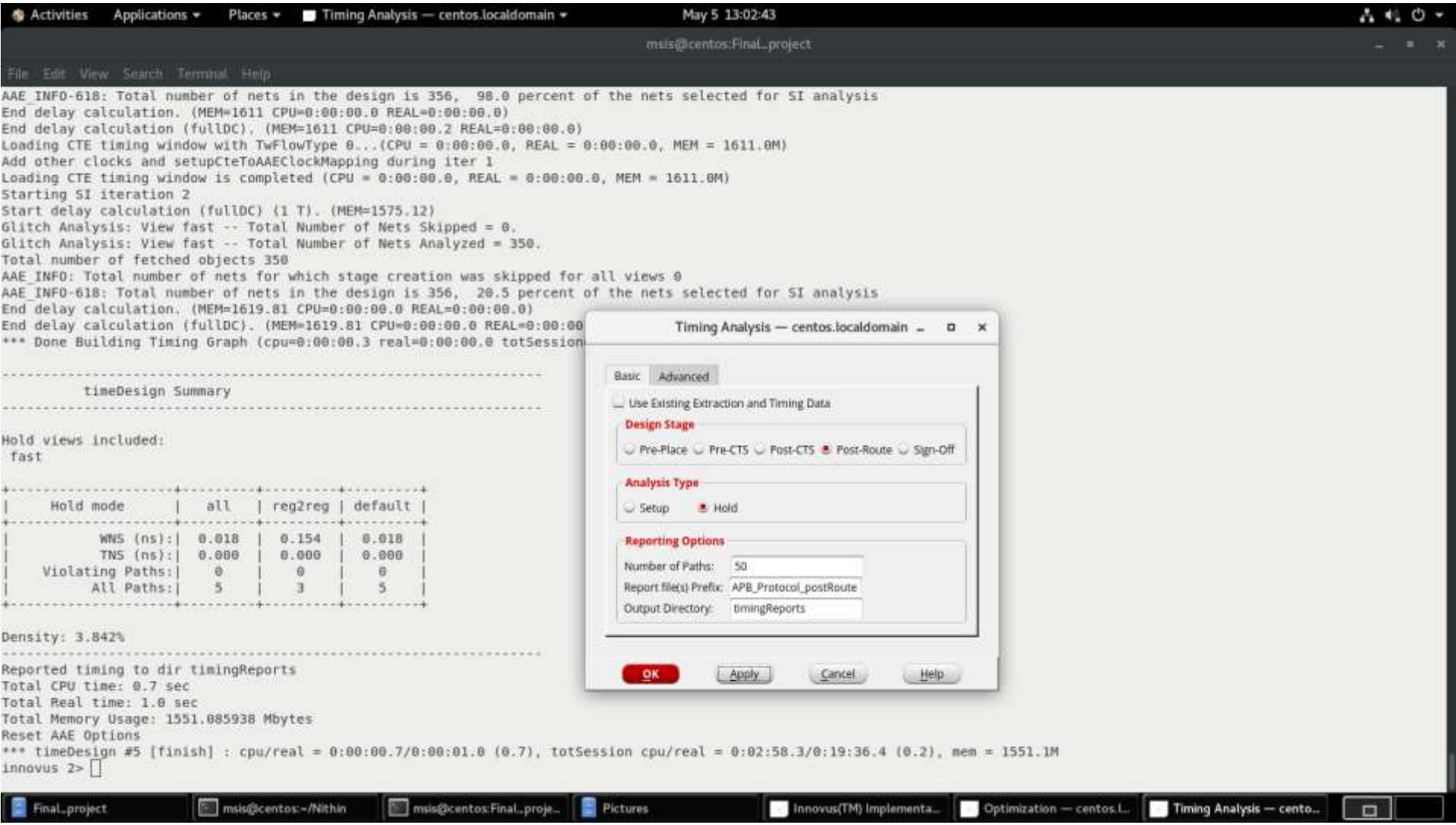

Fig 22: Post Routing hold timing report

5. Work done/Results

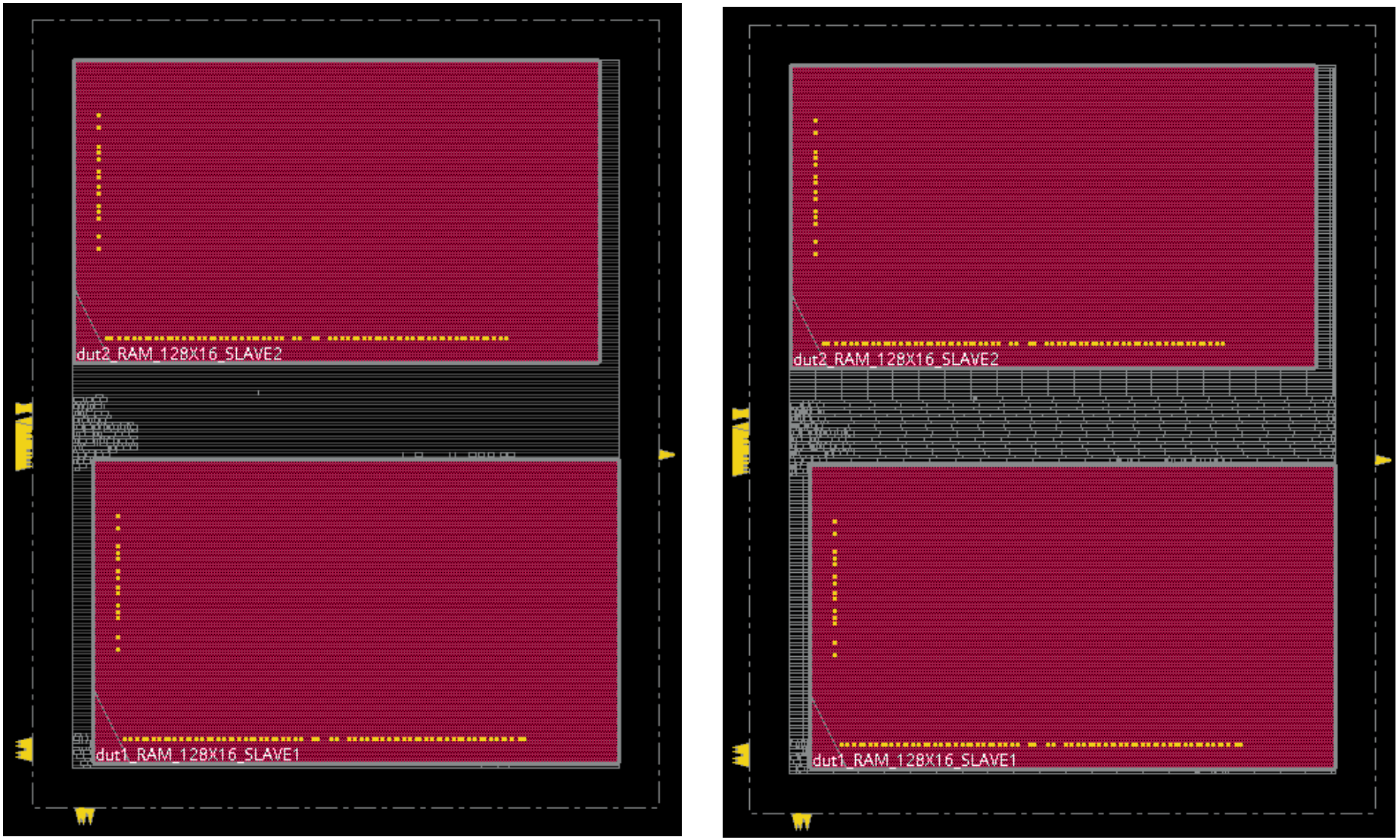

Fig 23: Adding fillers

5. Work done/Results

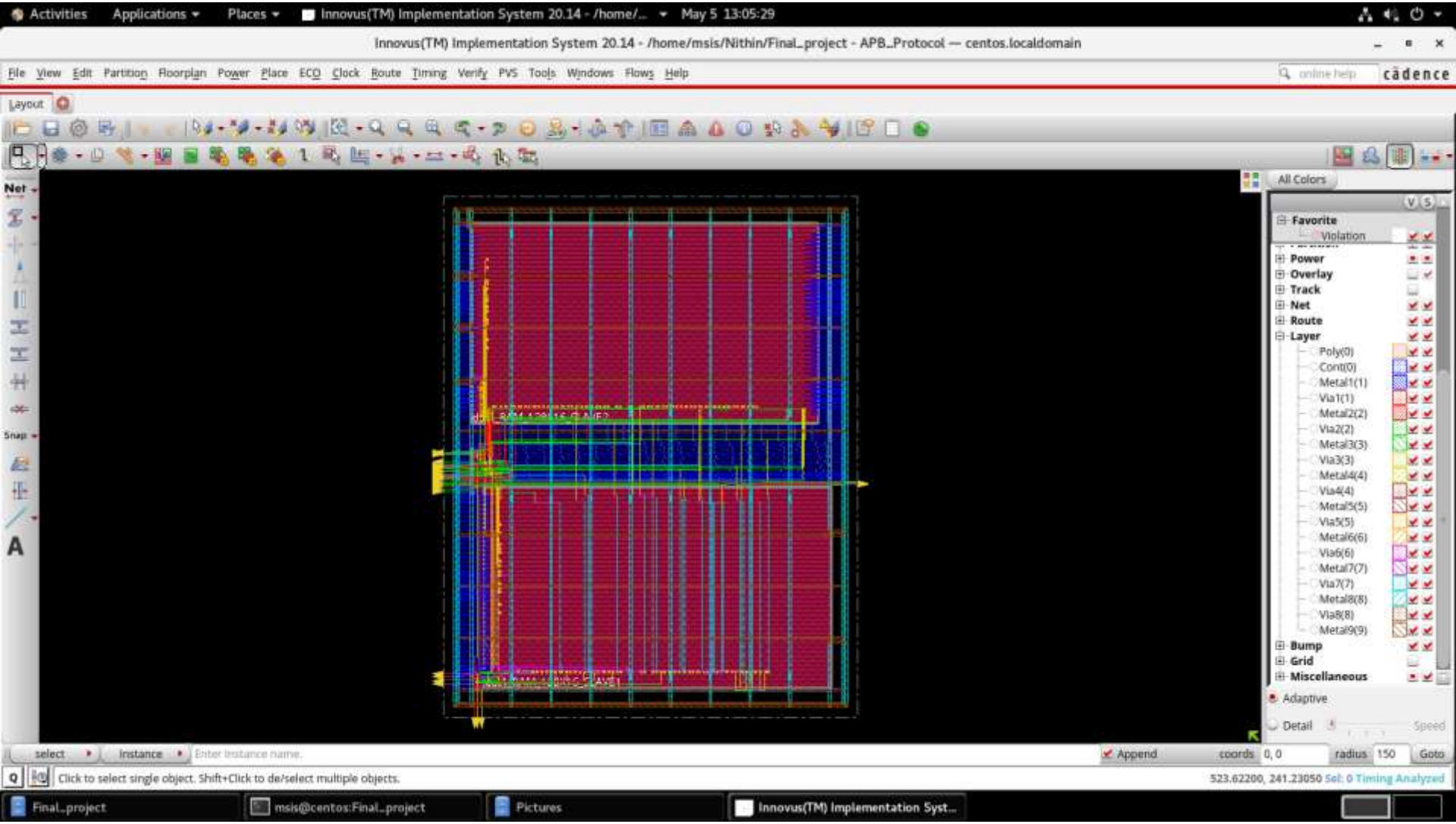

Fig 24: Final Design

Timing Report Summary

Sl. No	Stage	Setup timing (in ns)	Hold timing (in ns)
1	Pre CTS	17.699	-0.07
2	Post CTS	17.756	0.019
3	Post Routing	17.779	0.018

5. Work done/Results

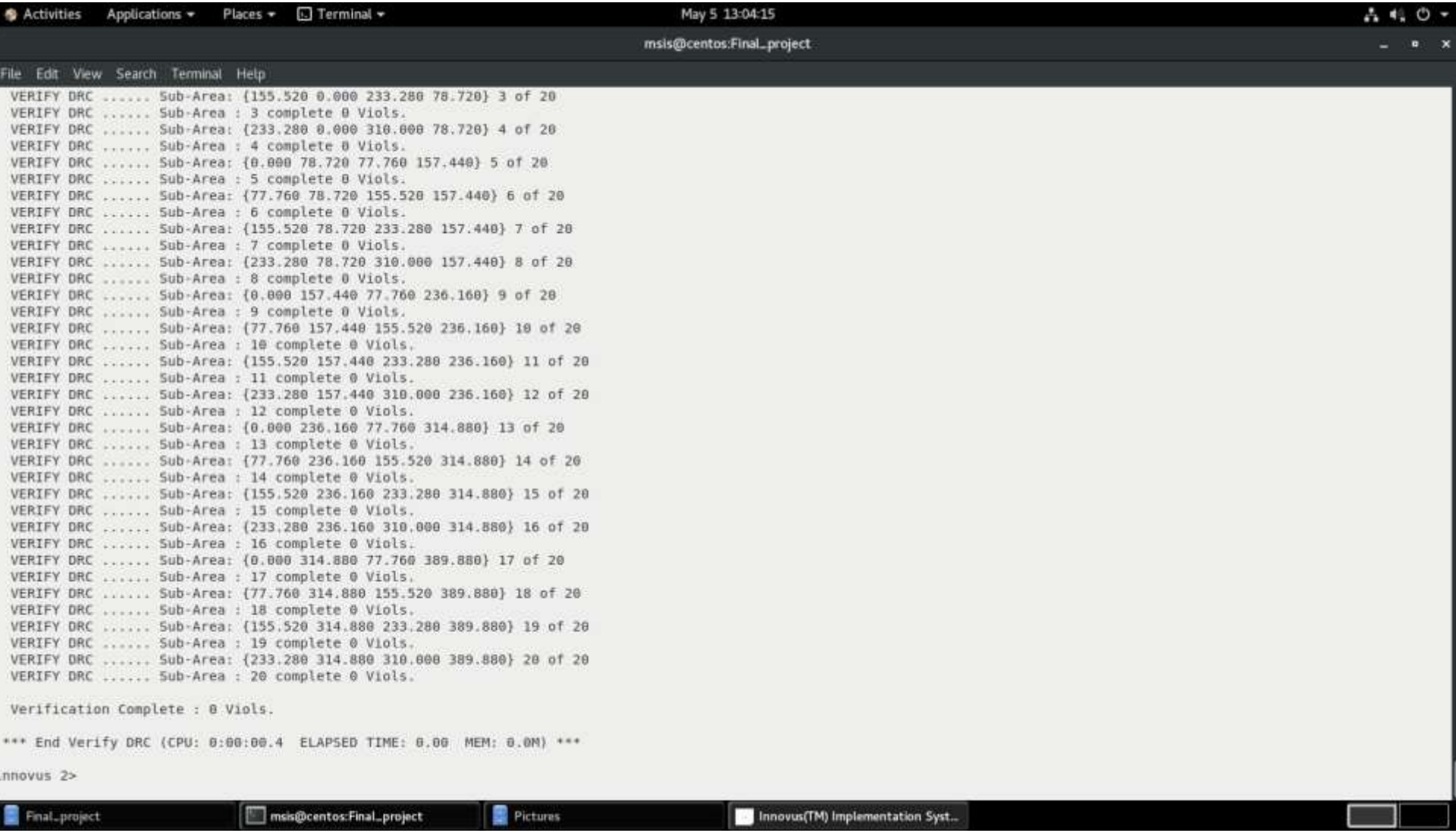

Fig 25: DRC check

UVM

Sl.no	Operation type	Test case
1	Normal Operation Testing	Write on to the slave -1 (8x i.e contiguous memory)
2		Write on to the slave -2 (8x)
3		Write using generated random data
4		Read from Slave 1
5		Read from Slave 2
6	Error injection	Write transfer without write address
7		Read transfer without read address
8		Write transfer without valid write data

Table 1: Test cases for verification

5. Work done/Results

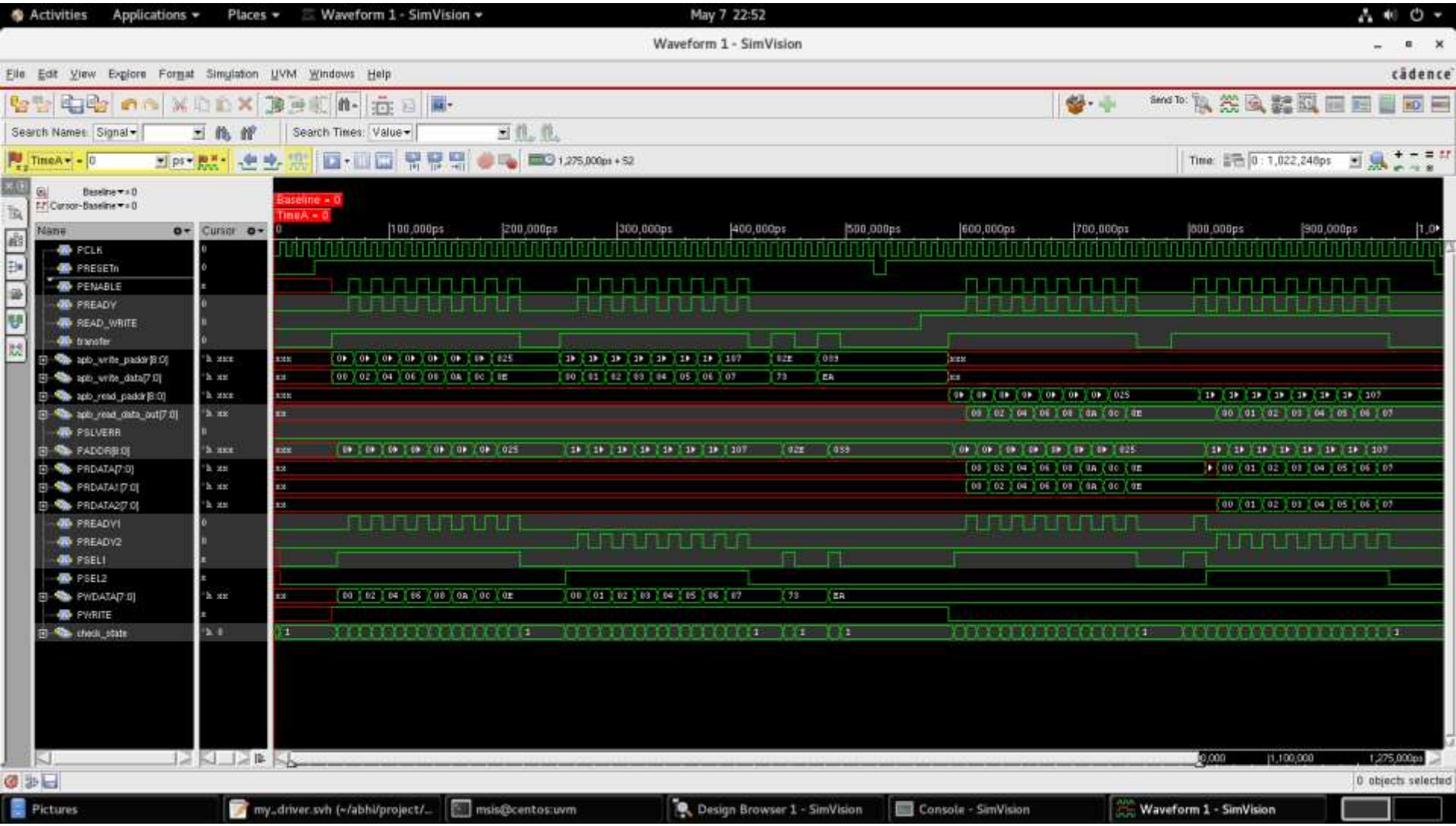

Fig 26: Simulation Results

5. Work done/Results

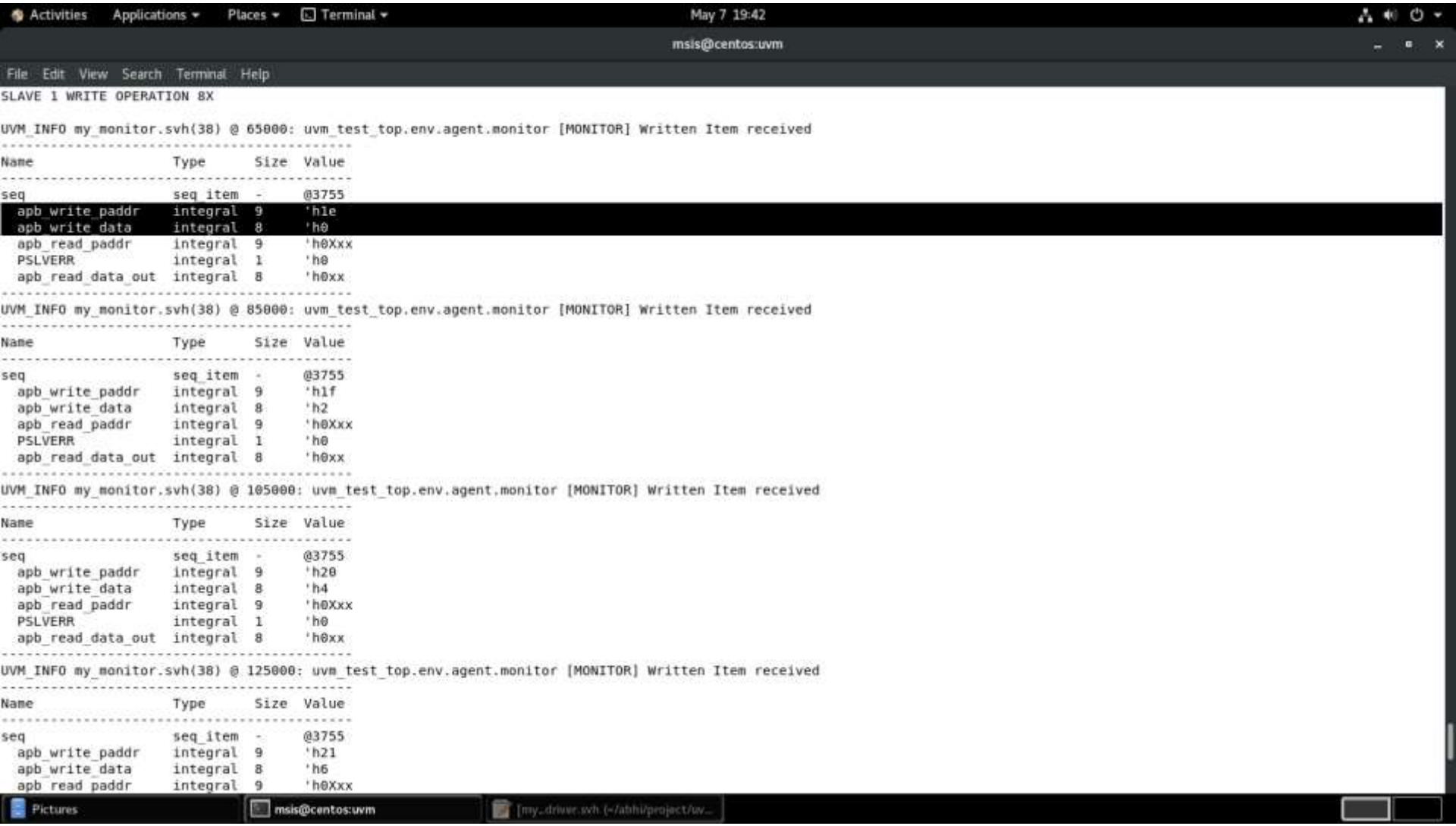

Fig 27: Write to Slave 1

5. Work done/Results

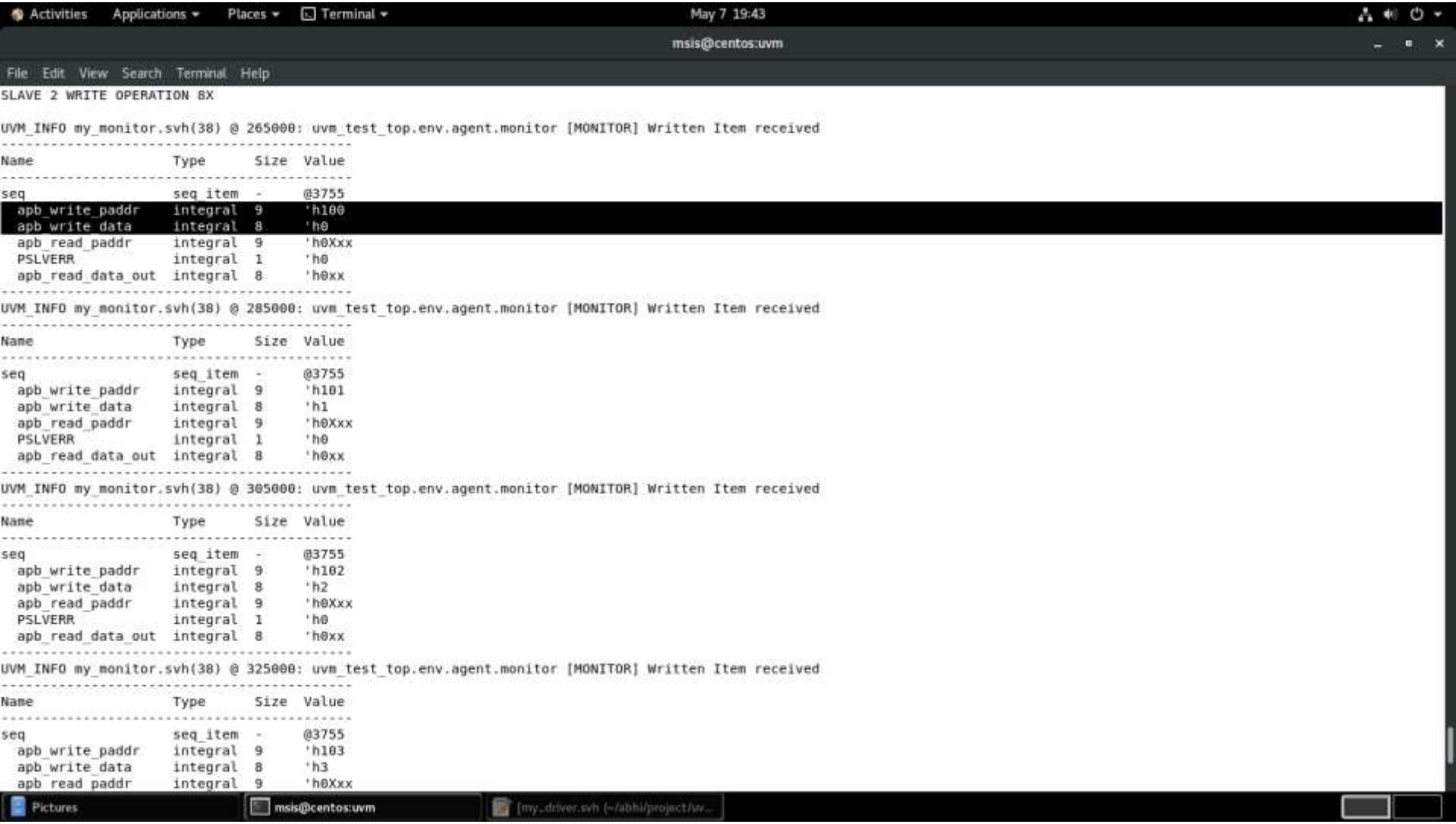

Fig 28: Write to Slave 2

5. Work done/Results

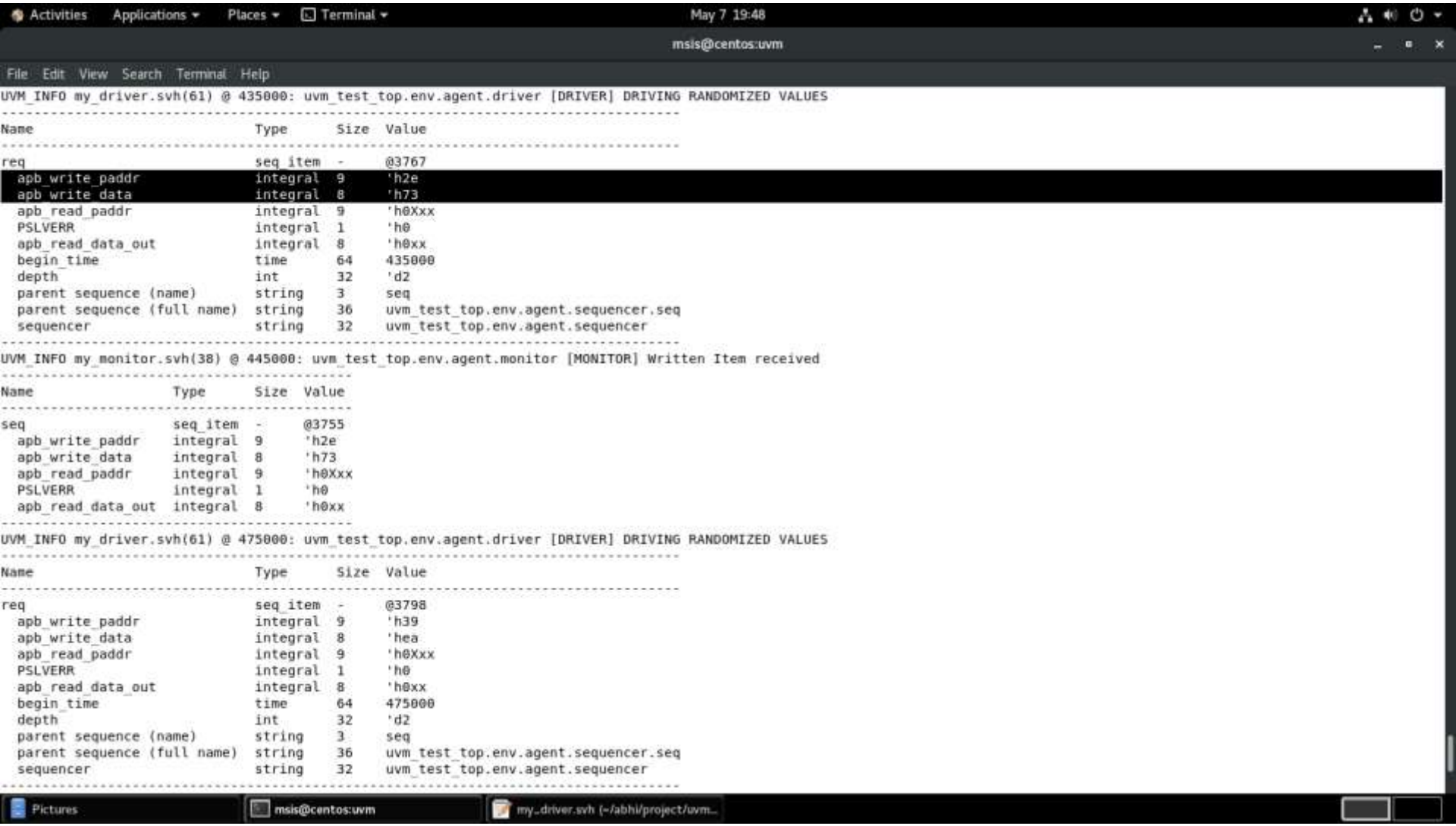

Fig 29: Driving Randomized Values

5. Work done/Results

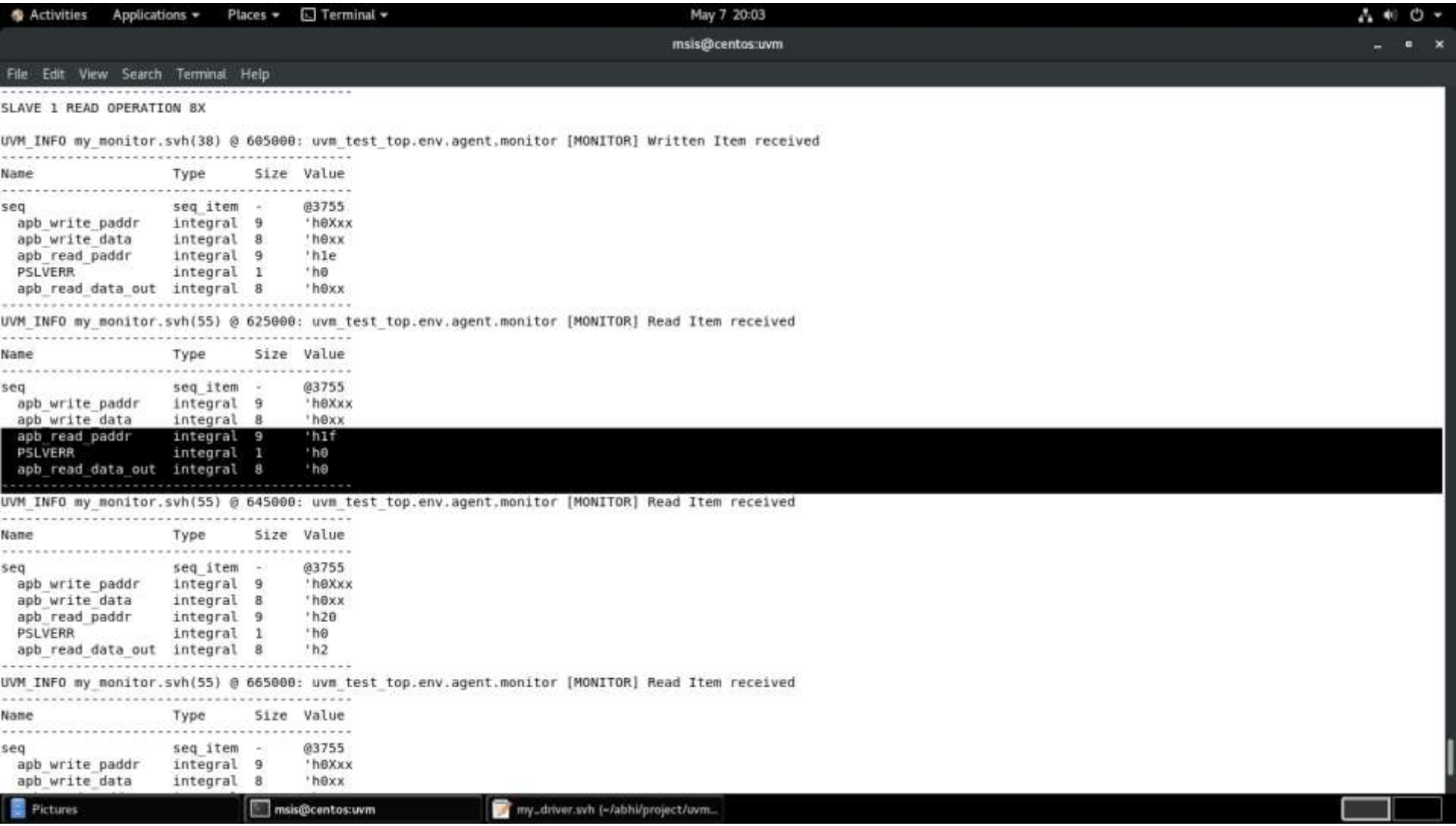

Fig 30: Read from Slave 1

5. Work done/Results

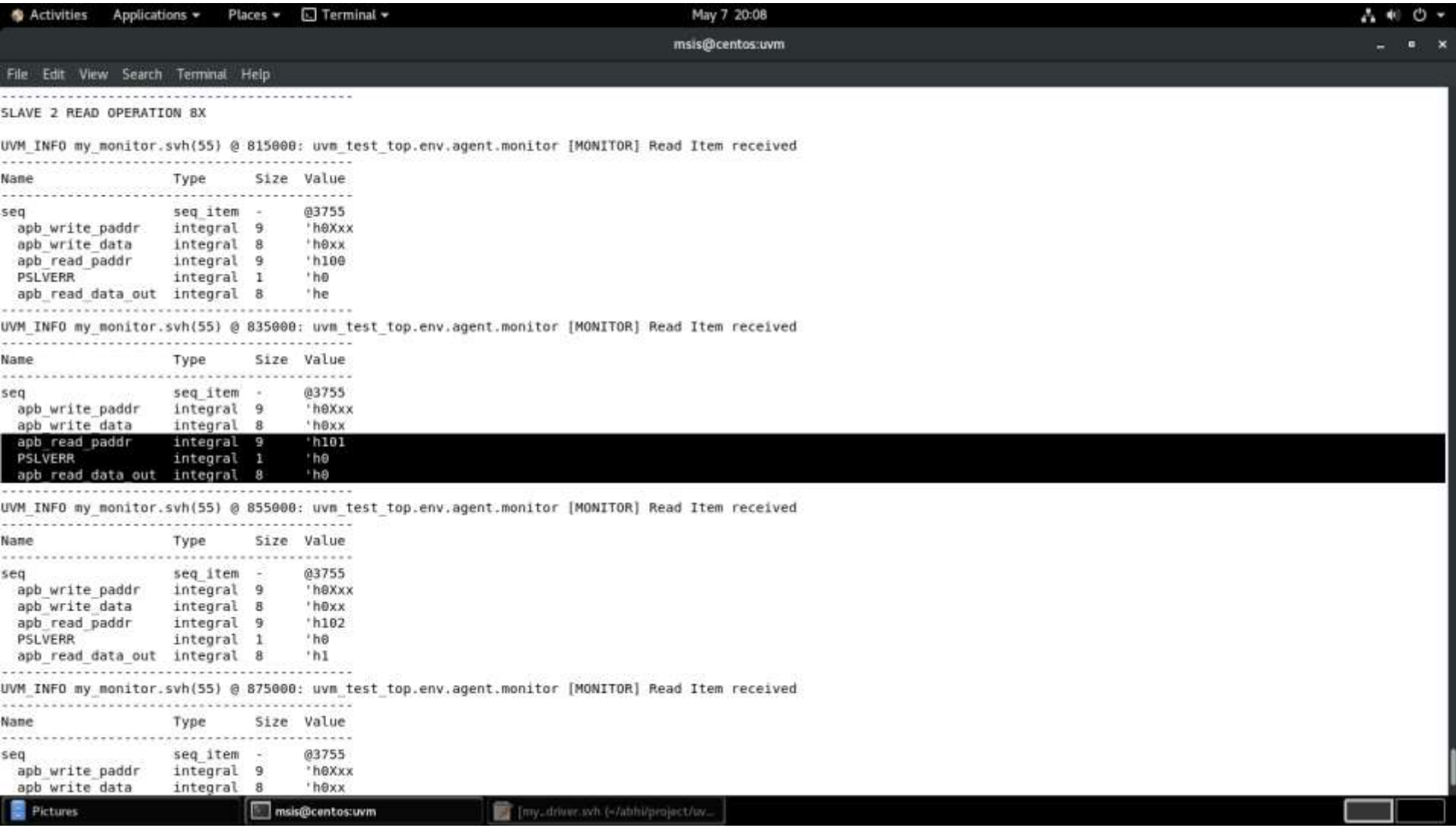

Fig 31: Read from Slave 2

5. Work done/Results

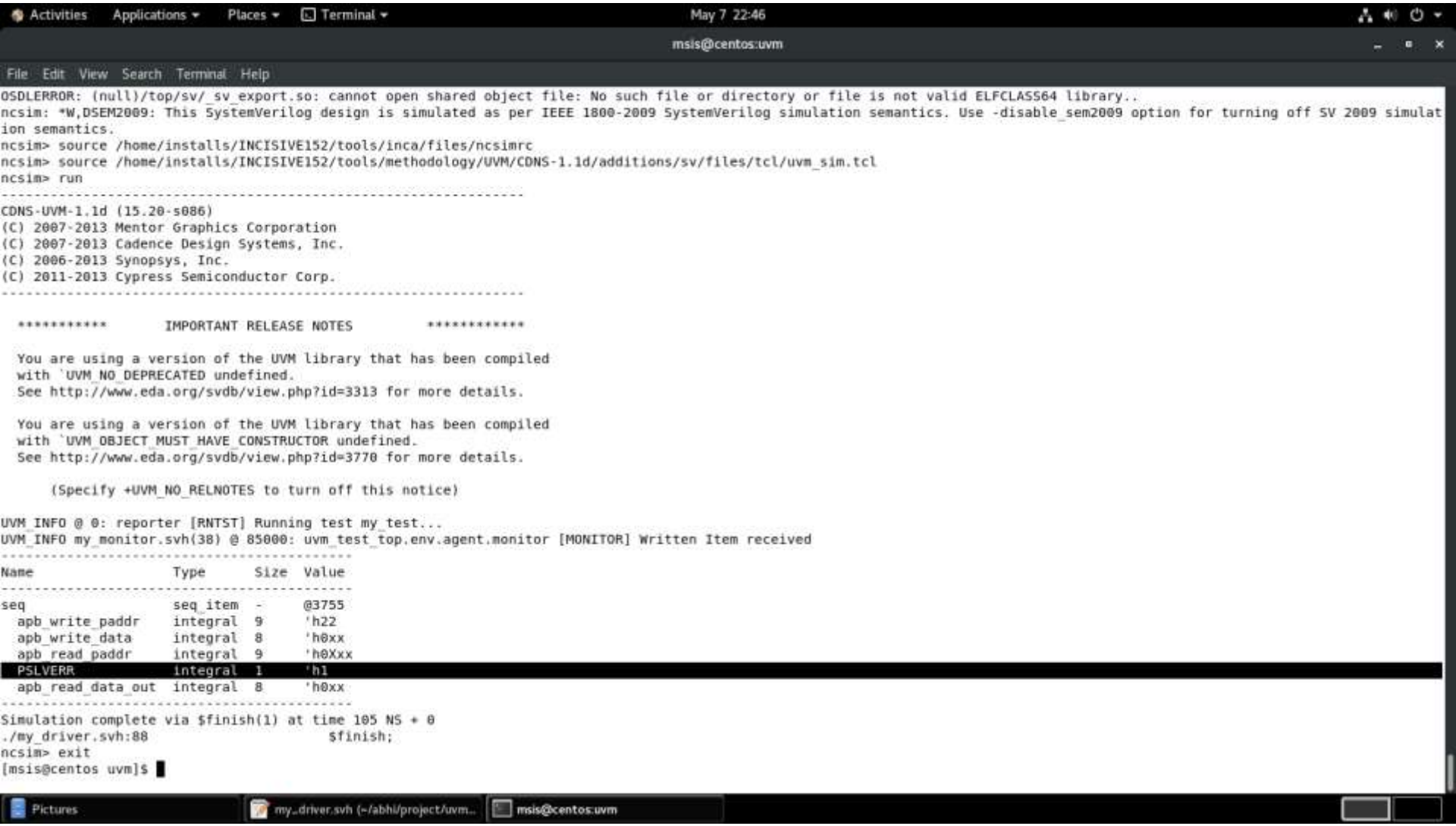

Fig 32: Invalid write data

5. Work done/Results

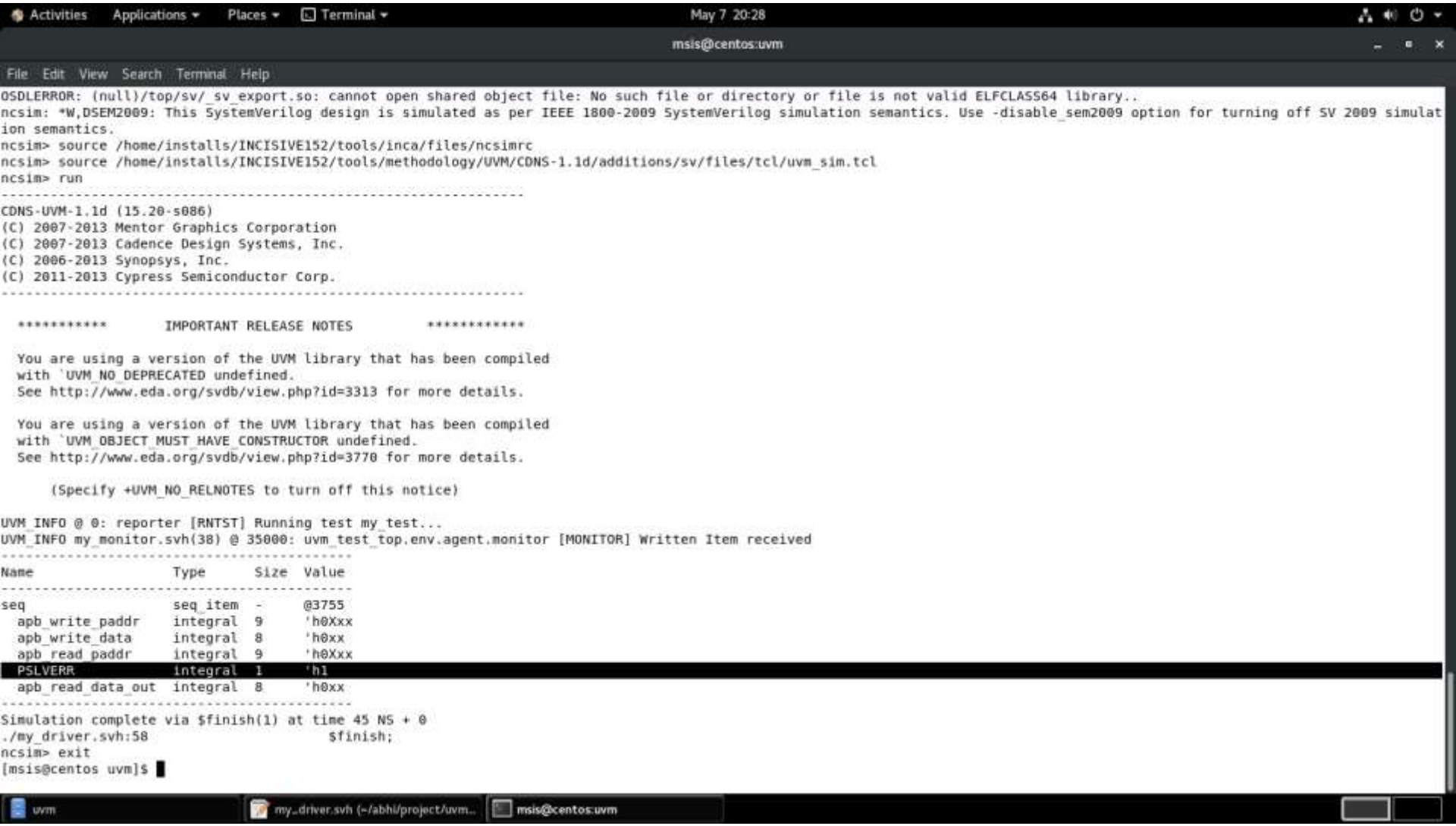

Fig 33: Invalid Write address

5. Work done/Results

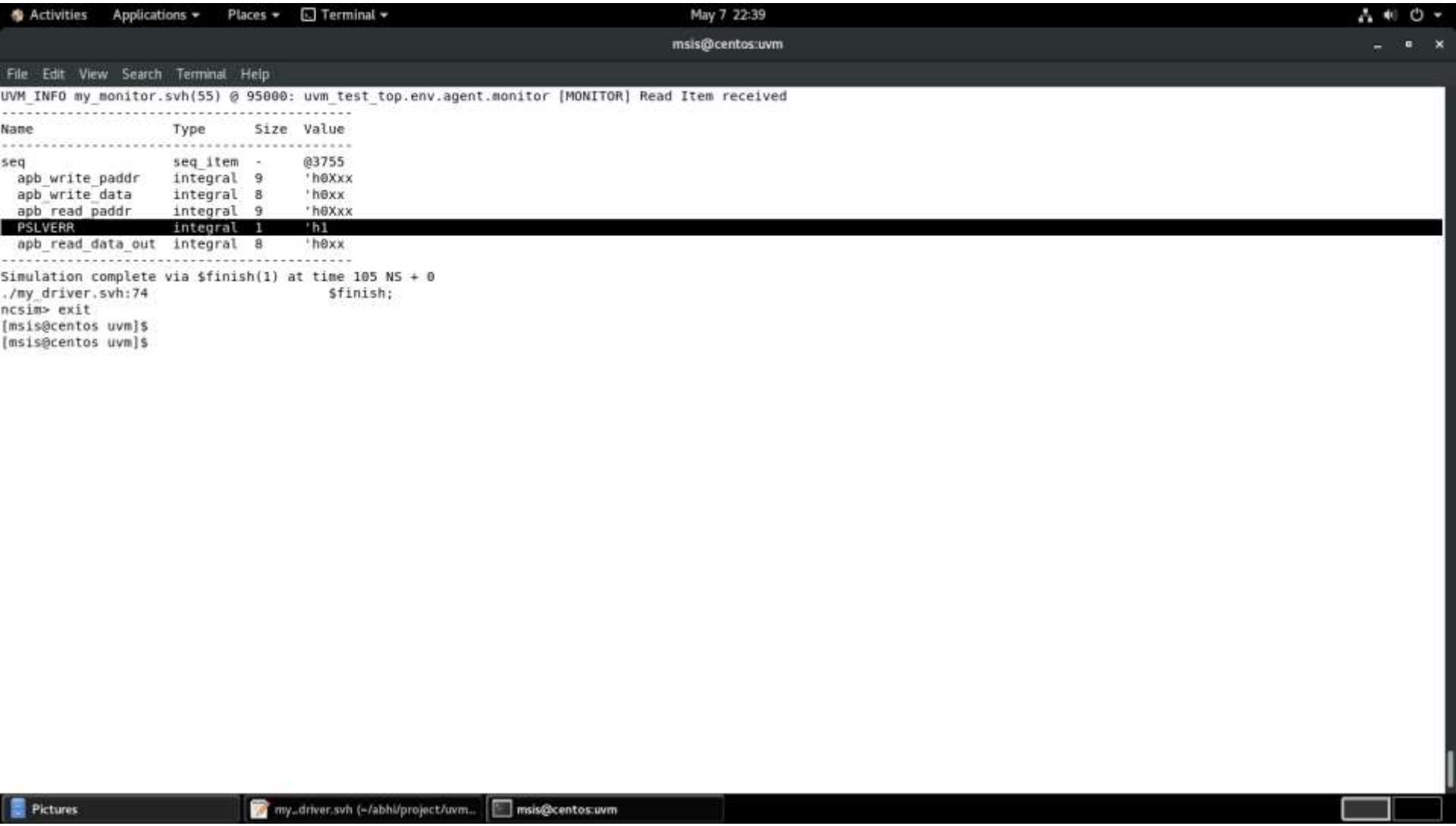

Fig 34: Invalid Read address

5. Work done/Results

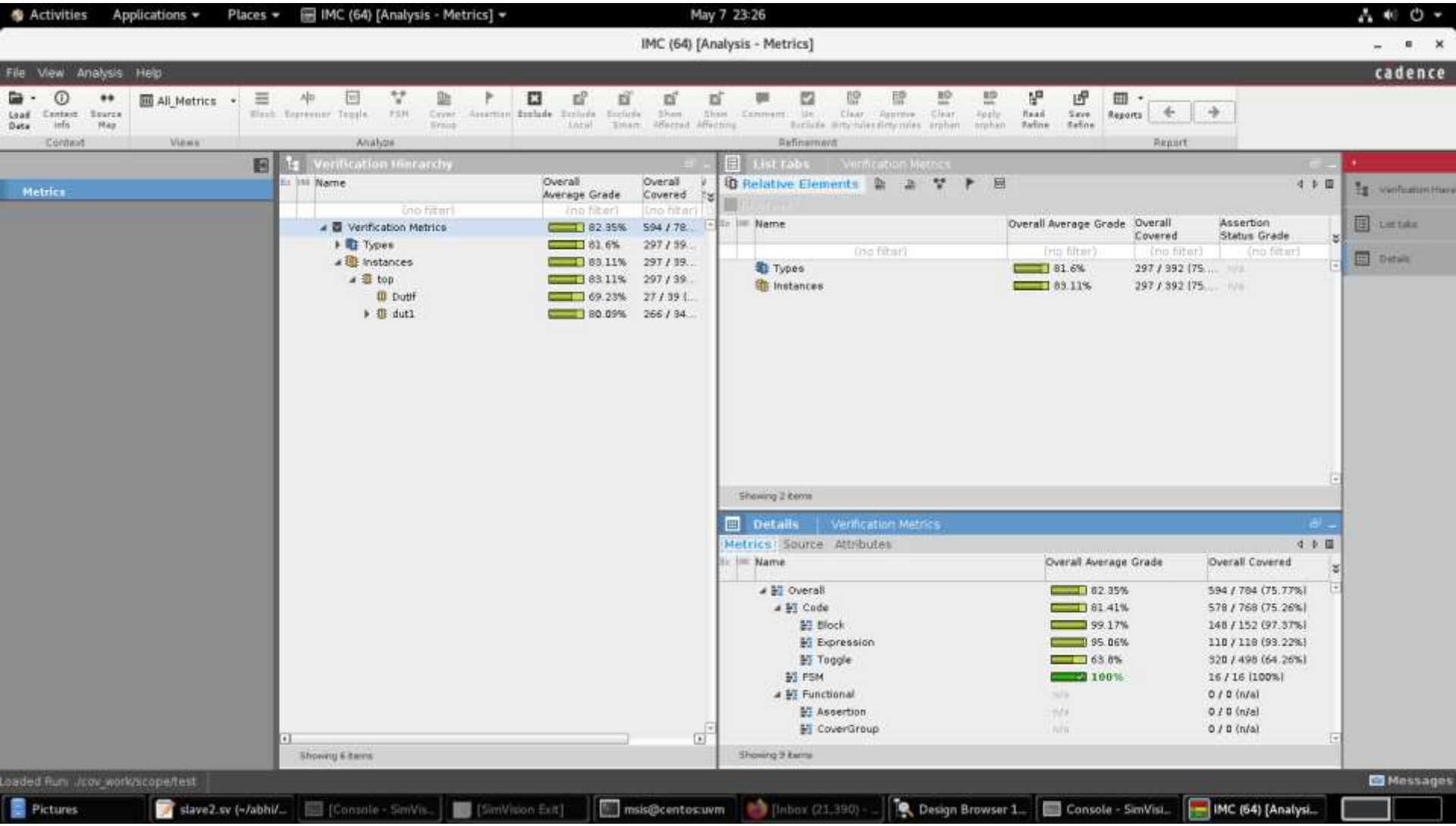

Fig 35: Verification Metrics

5. Work done/Results

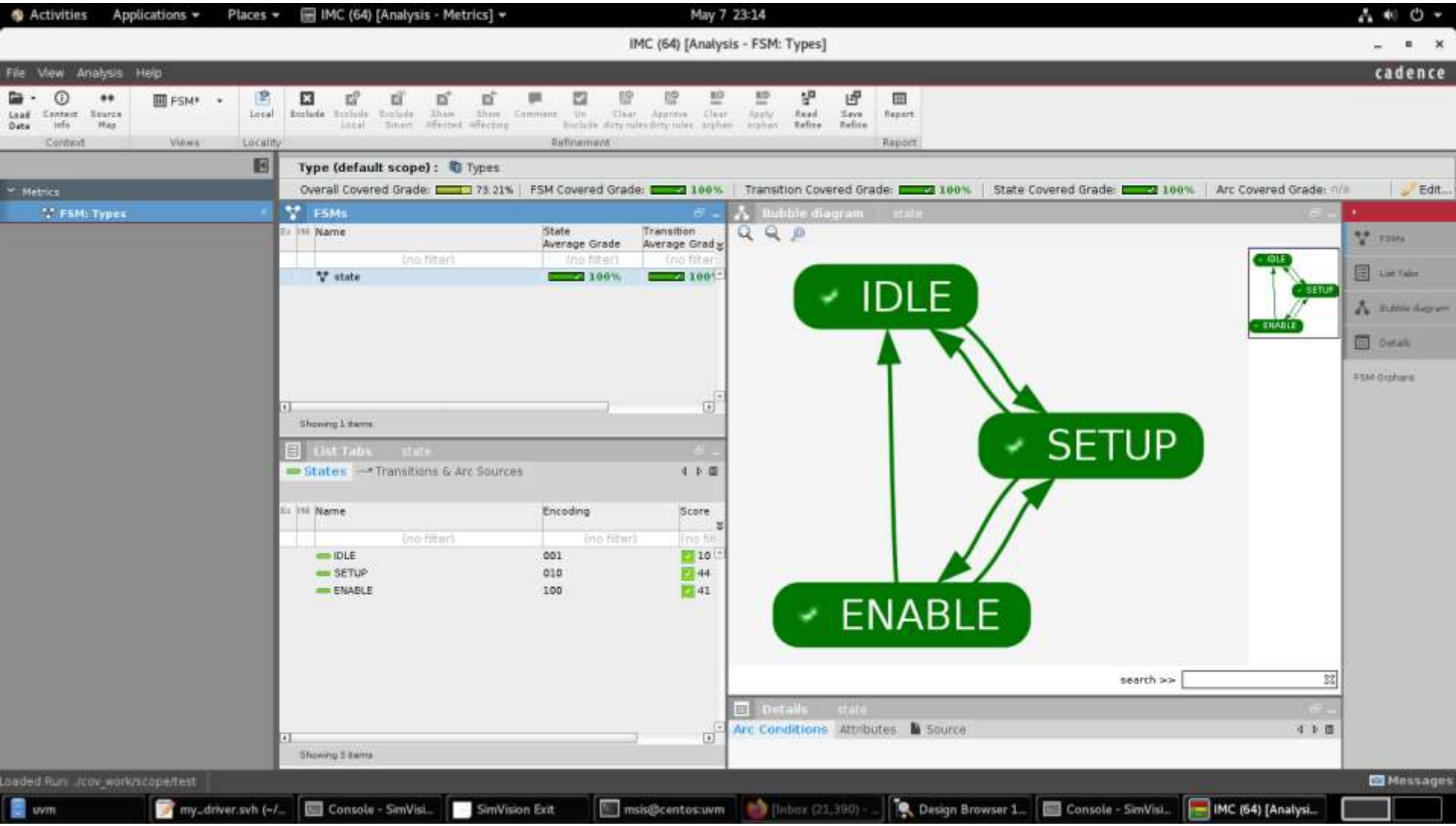

Fig 36: FSM Coverage

6. Conclusion

- Physical Design implemented for the design by creating macros for both the slaves and optimizing the design complexity.
- Verified using Universal Verification Methodology (UVM) and verification metrics generated.

7. References

- AMBA APB Protocol Specification – ARM
- Verification of Advanced Peripheral Bus Protocol (APB V2.0) - Meghana Jain H K1, Dr. Punith Kumar M B, Student, Professor, Dept of Electronics and Communication Engineering, P.E.S College of Engineering, Karnataka, India

THANK YOU…