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Design of DDR4 using System Verilog

Mini-Project Final Report

submitted to

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ABBREVIATIONS

DDR4 – Double Data Rate Version 4

DDR3 – Double Data Rate Version 3

DDR2 – Double Data Rate Version 2

SDRAM - Synchronous Dynamic Random Access Memory

DRAM – Dynamic Random Access Memory

DDR – Double Data Rate

I/O – Input/Output

MT – Mega Transfer

PC – Personal Computer

V – Volt

Gb – Giga Byte

CS – Chip Select

CKE – Clock Enable

DQ – Data Strobe

DQS – Differential Data Strobe

RAS – Row Address Strobe

CAS – Command Address Store

WE – Write Enable

BG – Bank Group

ACT – Activate

PRE – Pre-charge

PREA – Pre-charge All

RD – Read

WR - Write

1. Introduction

DDR4 SDRAM, is an abbreviation for Double Data Rate type 4 Synchronous Dynamic Random Access Memory.

Released into the market in 2014, it is a variant of Dynamic Random Access Memory (DRAM). DRAM has been used in the industry since the early 1970's. DDR4 is a successor to DDR3 and DDR2 technologies, released in 2007 & 2003 respectively.

Currently there is an increase in demand of memories because of its higher speed, lower cost and lower power consumption. DDR4 provides high reliability, availability and serviceability than other DDR4 memories. The cost of DDR memory is low, hence it is most used in PC's, storage and buffers.

The DDR controller can operate data in both edges of the clock cycles i.e., both rising and falling edge of the clock cycles, thereby double the transfer of data rate in the memory device.

Some of the significant improvements of DDR4 over the preceding generations is that, it consumes less power, faster speed and better data transfer rate, has no maximum memory size capability, clock speed varies from 1066MHz to 2133Mhz. Also, DDR4 has computing capabilities on different platforms like smartphones, tablets, PC, laptops which was limited in the previous generations.

Feature	DDR3	DDR4	DDR4 Advantage
Voltage (core and I/O)	1.5 V	1.2V	Reduces memory power demand
Prefetch	8n	8n	DDR4 also have 8n prefetch but parallel bank group
Densities	512Mb – 8Gb	2Gb – 16Gb	Better enhancement for large-capacity memory subsystems
Data rate (MT/s)	800, 1066, 1333, 1600, 1866, 2133	1600, 1866, 2133, 2400, 2667, 3200	Migration to higher data bandwidth
Internal banks	8	16	More banks
Bank groups	0	4	Faster burst accesses

Table 1.1: Comparison of DDR4 SDRAM with DDR3 generation

2. Literature Survey

1. "Design of DDR4 SDRAM controller" – Md. Ashraful Islam, Md. Yeasin Arafath, Md. Jahid Hasan, 8th International conference on Electrical and Computer Engineering, 2014

   The paper proposes the overall architecture of the DDR4 SDRAM controller. The detailed design of operations of its individual sub blocks is also described, along with the advantage of DDR4 SDRAM over previous generation DDR3.

2. "Modelling of DDR4 Memory and Advanced Verifications of DDR4 Memory Subsystems" – Pavan G, V Siddeswara Prasad, International Research Journal of Engineering and Technology (IRJET), 2022.

   The paper discusses on how the authors have designed a DDR4 Memory Model using system Verilog to improve the efficiency in terms of data rate when compared to its previous generation. The main objective being the DDR4 improvement with reference to DDR3 according to the JEDEC Spec of DDR4.

3. Objectives

The main aim of the project is to Design a DDR4 RAM using system Verilog with improved efficiency of the system in terms of: Data rate, increased read/write operations speed, faster burst access and reduce memory power demand.

4. Specifications

Specification sheets is available by different manufacturers such as Micron Technology Inc., Samsung, etc which provide all details of DDR4 SDRAM. The one being referred for this project is that of Micron Technology Inc and JEDEC Standard(JESD79-4).

5. Block Diagram

5.1 Top Level Block Diagram

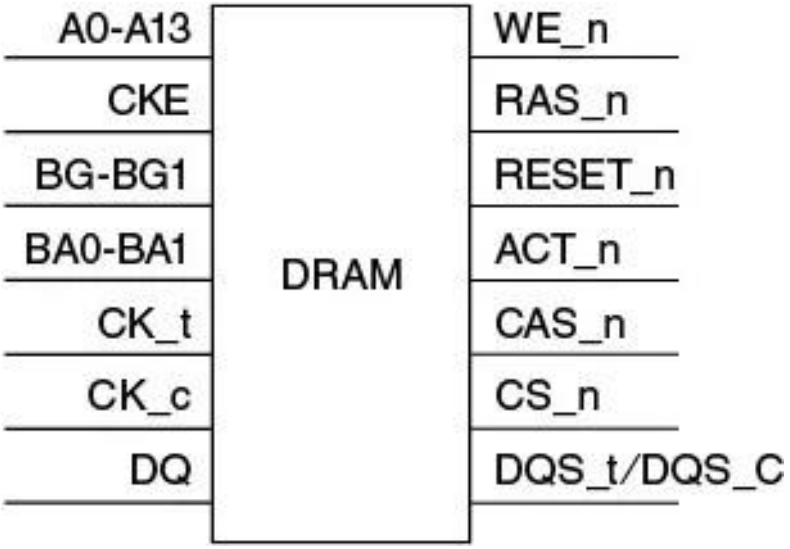

Fig 5.1: Top Level Block Diagram

Symbol	Type	Function
RESET_n	Input	DRAM is active only when this signal is HIGH
CS_n	Input	The memory looks at all the other inputs only if this is LOW.
CKE	Input	Clock Enable. HIGH activates internal clock signals and device input buffers and output drivers.
CK_t/CK_c	Input	Differential clock inputs. All adders and control signals are sampled at the crossing of posedge of the CK_t & negedge of CK_n.
DQ/DQS	Input	Data Bus & Data Strobe. This is how data is returned in and read out. The strobe is essentially a data valid flag
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	These are dual function inputs. When ACT_n & CS_n are LOW, these are interpreted as Row Address Bits. When ACT_n is HIGH, these are interpreted as command pins to indicate READ, WRITE or other commands
ACT_n	Input	Activate command input
BG0-1 BA0-1	Input	Bank Group, Bank Address
A0-13	Input	Address inputs

Table 5.1: Pin description of DRAM

The Top level block diagram of a DRAM provides an overview of the available pins and the pin description provides a brief understanding of the abbreviations and the basic functionalities that each pin performs.

5.2 Functional Block Diagram

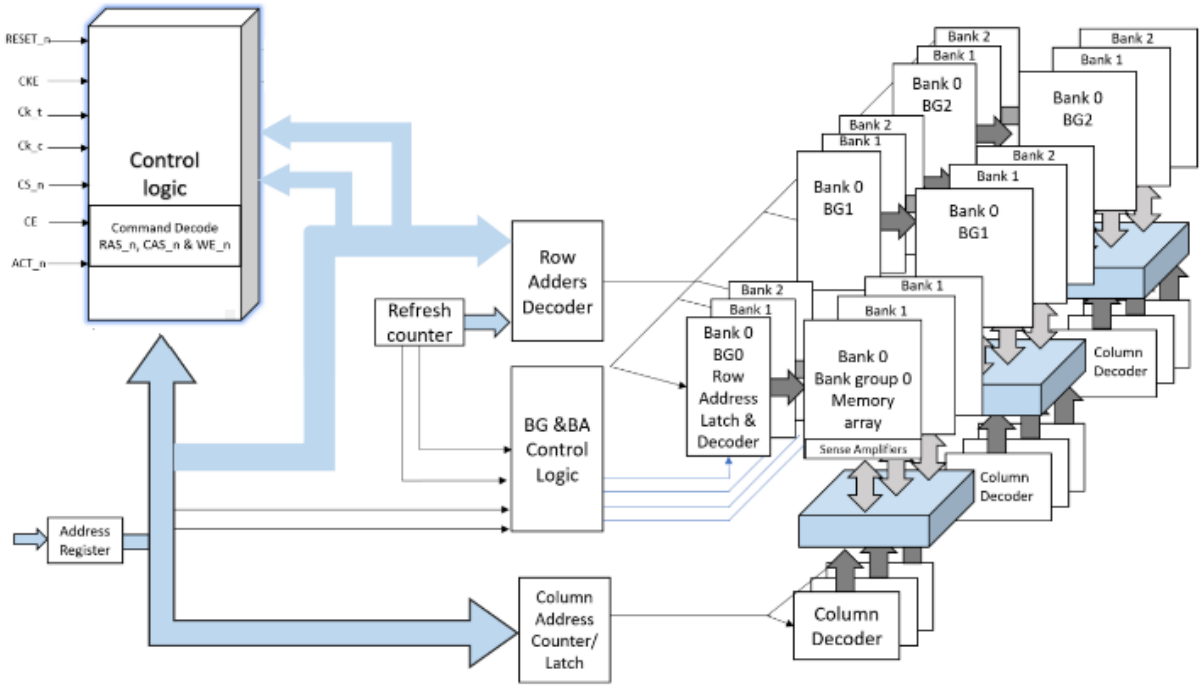

Fig 5.2: Functional Block Diagram

Activation Command Input:

ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14

CKE (Clock Enable):

CKE high activates internal clock signals.

CLK_t(Clock True):

It is true clock signal, where read and write operation is performed at positive edge of the clock cycle.

CLK_c(Clock complement):

It is compliment of the clock signal. Read and write operation is performed at negative edge of the clock cycle.

Address register:

Holds the information on the bank group and bank to be selected. Also contains row and column address based on RAS and CAS inputs.

Command Inputs:

RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi-function. For example, for activation with ACT_n Low, those are Addressing like A16, A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command.

BG(Bank Group) and BA(Bank Array) control Logic:

Selects the bank group and bank based on the address passed.

Row address Decoder:

Selects the row in bank in which data has to be written/read. The entire row data of a particular bank selected is sent to the sense amplifiers.

Column address Decoder:

Selects the column in the row which is sent to the sense amplifier.

Refresh counter:

The capacitor storing data will discharge over time. Periodic refresh is required to keep the data from being lost.

RST(Reset):

When Reset mode is activated, the device will go to Initialization state where thedata in sense amplifier is cleared.

5.3 Signals and Commands

In order to perform any operation on the DRAM a set of signals and commands need to be executed. To read or write data to or from the DRAM, first the DRAM row must be precharged. Then, an activation command must be issued. After successful activation, the data in the required row will be transferred to the sense amplifiers. The required data is then read from the sense amplifiers by using the column addresses.

The following are the main signals to be considered for DDR4 operation

Symbol	Type	Description
A [16:0]	Input	Address Inputs: Provides the row address for ACTIVATE commands and the column address for READ/WRITE commands to select one location out of the memory array in the respective bank.
A10/AP	Input	Auto precharge: A10 is sampled during READ and WRITE commands to determine whether auto precharge should be performed to the accessed bank after a READ or WRITE operation
A12/BC_n	Input	Burst chop: A12/BC_n is sampled during READ and WRITEcommands to determine if burst chop (on-the-fly) will be performed.
ACT_n	Input	Command input: ACT_n indicates an ACTIVATE command.
BA [1:0]	Input	Bank address inputs: Define the bank (within a bank group) towhich an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied.
BG	Input	Bank group address inputs: Define the bank group to which anACTIVATE, READ, WRITE, or PRECHARGE command is being applied.
CLK_t, CLK_c	Input	Clock: Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.

CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations
CS_n	Input	Chip select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection onsystems with multiple ranks. CS_n is considered part of the command code.
DM_n, UDM_n LDM_n	Input	Input data mask: DM_n is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a write access. DM is sampled on both edges of DQS. UDM_n is associated with DQ [15:8]; LDM_n is associated with DQ [7:0].
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14(along with CS_n and ACT_n) define the command and/or address being entered.
RESET_n	Input	Active LOW asynchronous reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH.RESET_n must be HIGH during normal operation.
DQ	I/O	Data input/output: Bidirectional data bus. Represents the DQ [15:0] for the x16 configuration.
DBI_n, UDBI_n, LDBI_n	I/O	DBI input/output: Data bus inversion. UDBI_n and LDBI_n isthe input/output signal used for data bus inversion in the x16 configuration. UDBI_n is associated with DQ [15:8], and LDBI_n is associated with DQ [7:0].
DQS_t, DQS_c, UDQS_t, UDQS_c, LDQS_t, LDQS_c	I/O	Data strobe: Output with READ data, input with WRITE data. Edge-aligned with READ data, centered-aligned with WRITEdata. For the x16, LDQS corresponds to the data on DQ [7:0];UDQS corresponds to the data on DQ [15:8].

Table 5.2: DDR4 signals and description

5.4 Finite State Diagram

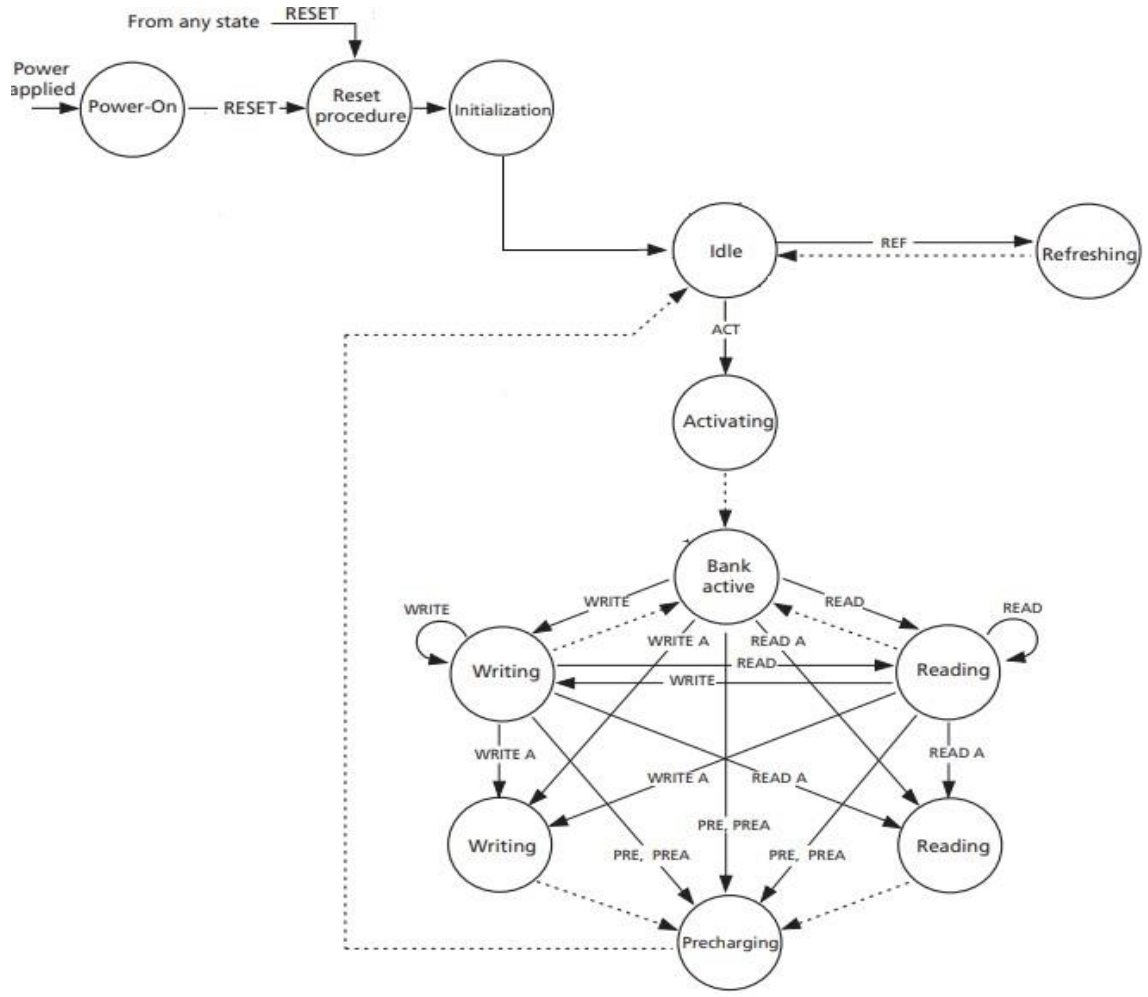

Fig 5.3: State diagram of DDR4 SDRAM

Command	Description
ACT	Activate
PRE	Pre-charge
PREA	Pre-charge All
READ	RD, Read Data
READA	Read and Pre-charge
WRITE	WR, Write data
WRITEA	Write and Pre-charge
RESET	Start reset procedure

Table 5.3: FSM Commands with respective descriptions

The implementation of DDR4 is done in accordance with the FSM model shown above.

There are 9 major states of operation that can be implemented using System Verilog.

a. Open Page Policy: Here after the address is received, if the new location to be accessed is a different row then, after the completion of current operation the state is changed to PRECHARGE where the data from the sense amplifiers is written back into the row before the activation of the new row as mentioned in the address.
b. Closed Page Policy: In this, as shown in the FSM represented by the dotted lines after READ and WRITE operation, the state automatically moves to the PRECHARGE state before the next command is received regardless of the address
    - The ACTIVATE command is used to activate a row in a particular bank for subsequent access.
    - The PRE-CHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. Once pre-charge is done, the bank is in idle state and must be activated prior to read/write commands being issued to the bank. Pre-charge commandis allowed if already pre-charging or even if a bank is not open.
      AUTO PRE-CHARGE is activated when read/write is performed with A10 high.
    - REFRESH command is used in periodic intervals each time a refresh is required in the device. Refresh generally happens every 32ms if temperature is above 85℃ and 64msif temperature is below 85℃.
    - IDLE state is defined as all banks are closed and no data bursts are in progress.
    - During INITIALIZATION, default values of Mode registers are set. These default modes aredefined in the Micron Specification sheet.
    - When the RESET command is preformed, the device is forced to the initialization state.
    - WRITE/WRITE_A: These states are used to write the data into the sense amplifier and theninto the memory. The major difference in the two states is that Write command is used in an open page policy whereas WRITE_A is used in a closed page policy.
    - READ/READ_A: These states are used to read the data from the memory and then into the row buffer (sense amps). The major difference in the two states is that read command is used in an open page policy whereas READ_A is used in a closed page policy.

6. Work done/ Results

The Cadence NCSim tool was used for the simulation purposes and the following operations were performed.

- Data is written in a bank of a particular bank group following the necessary steps like PRECHARGE, delay etc.
- The below data is read and displayed back (read operation on memory)
- Stored multiple data in multiple banks of single/multiple bank groups.
- Read Multiple data from multiple banks of single/multiple bank group.
- Burst WRITE into or READ from a bank.

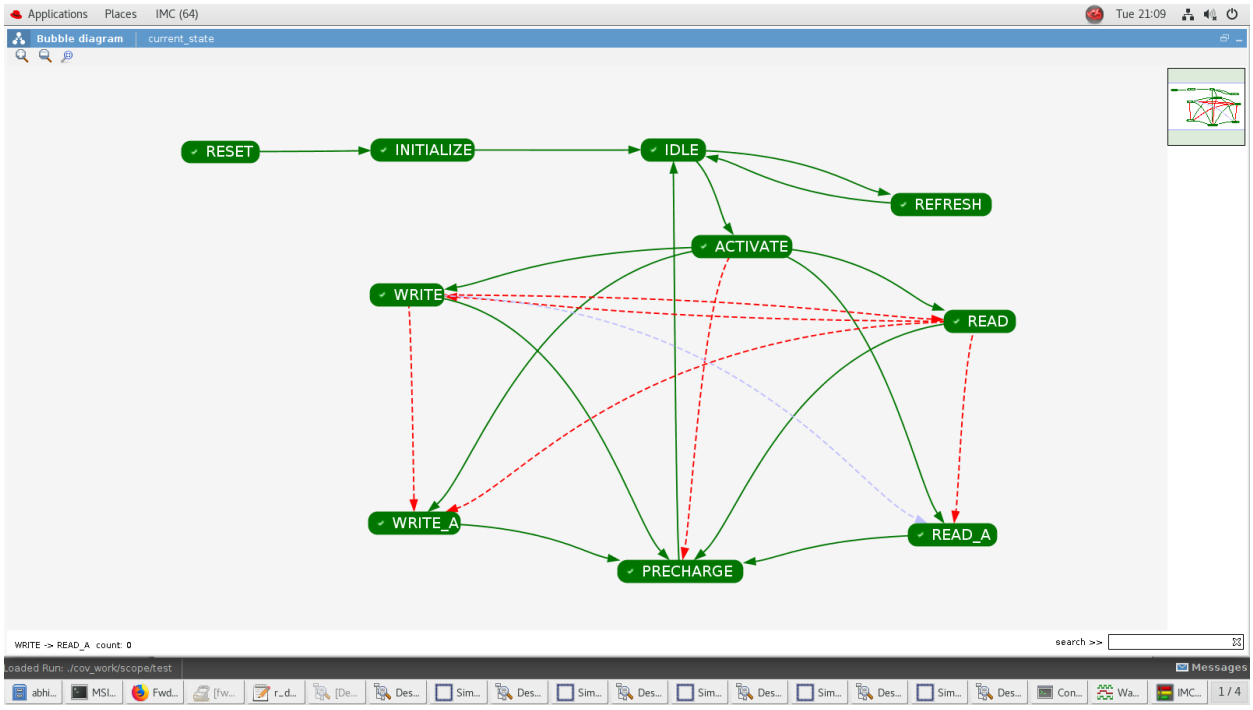

Fig 6.1: Verified FSM coverage of simulated DDR4 SDRAM

In general, READ/WRITE or READ_A/WRITE_A operation is performed when CKE is HIGH (which enables the clock) and also when RESET_n is HIGH.

When ACT_n is active LOW it selects the bank to perform READ/WRITE operation. If the AP is HIGH it performs READ_A/WRITE_A operation.

Only if CS_n is active LOW it is allowed to perform READ/WRITE & READ_A/WRITE_A operations.

Based on the above inputs, the BG with corresponding BGA and their respective ROW_ADDRESS, COLUMN_ADDRESS is accessed to perform either READ/WRITE operation.

The DATAIN is first written into the SENSE_AMPLIFIER which stores the data as buffer until AP state is active HIGH and then writes the data into the respective Bank Group/Bank to their corresponding Row/Column addresses.

If the BURST_MODE is active HIGH, the above data from SENSE_AMPLIFIER is written into or read from the corresponding Row/Column addresses of a given Bank Group/Bank successively.

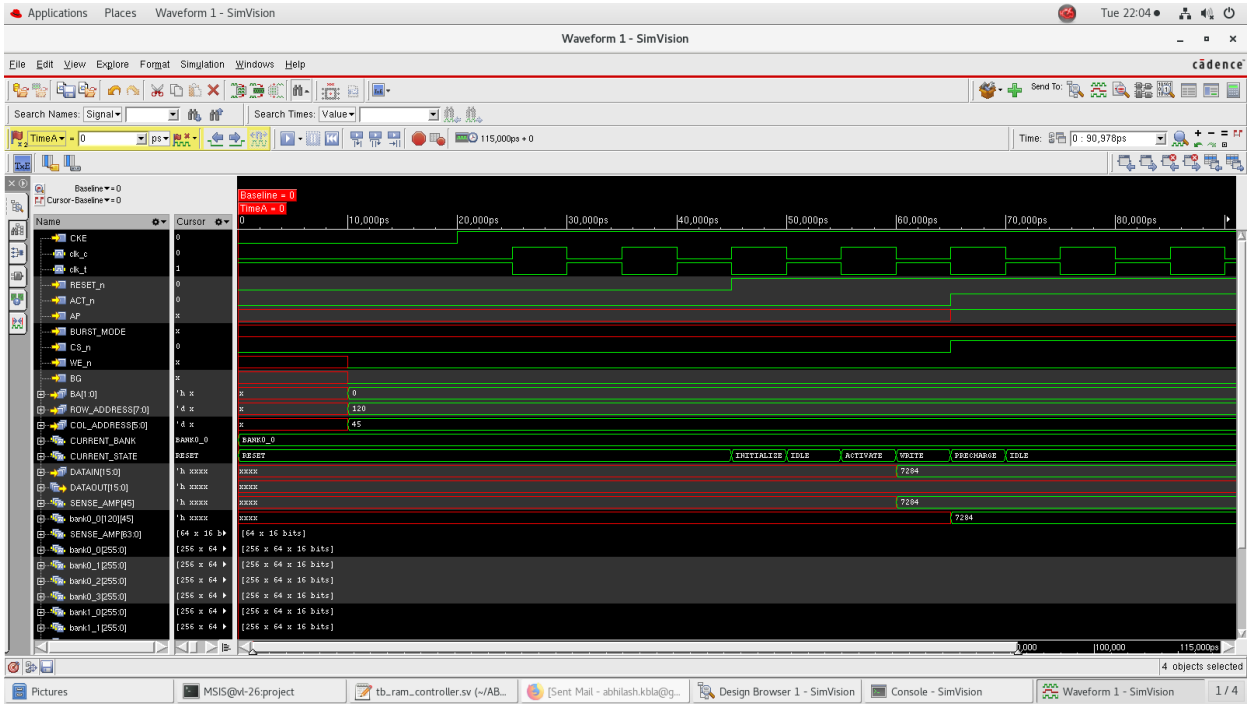

Fig 6.2: Displaying RESET & CKE(Clock Enable) activity when both become active

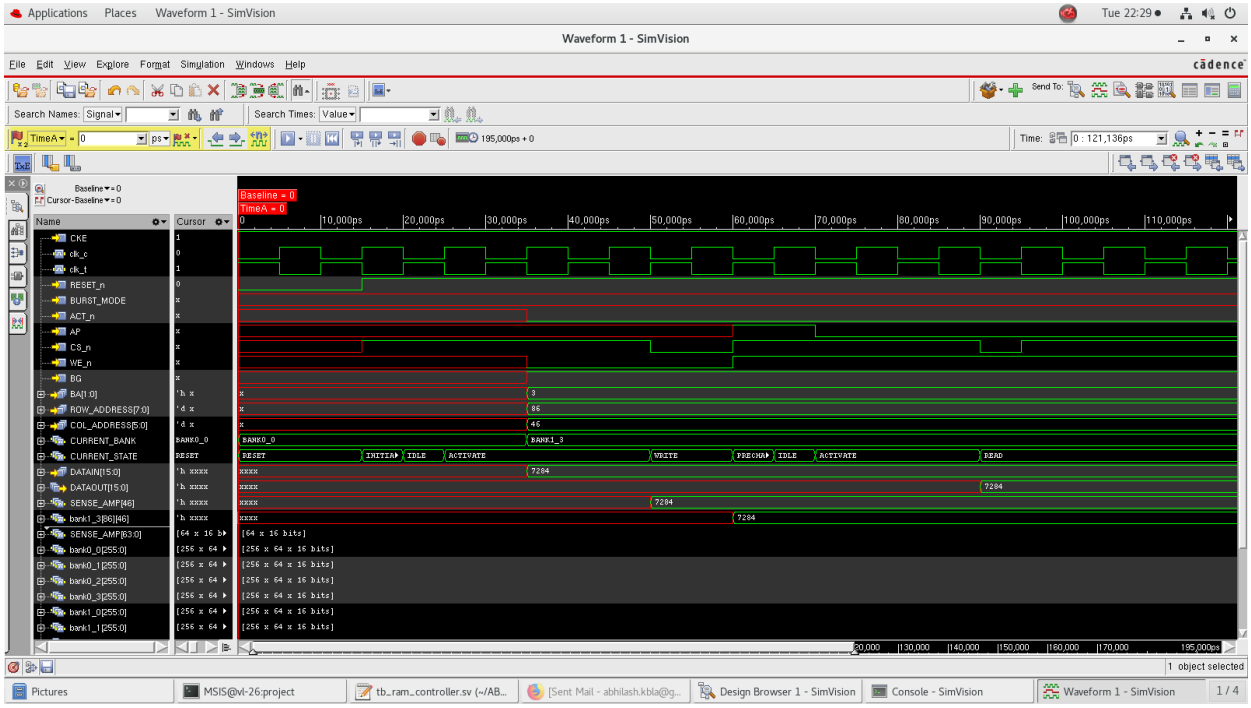

Fig 6.3: Functioning of READ/WRITE operation only when CS(Chip Select) is active

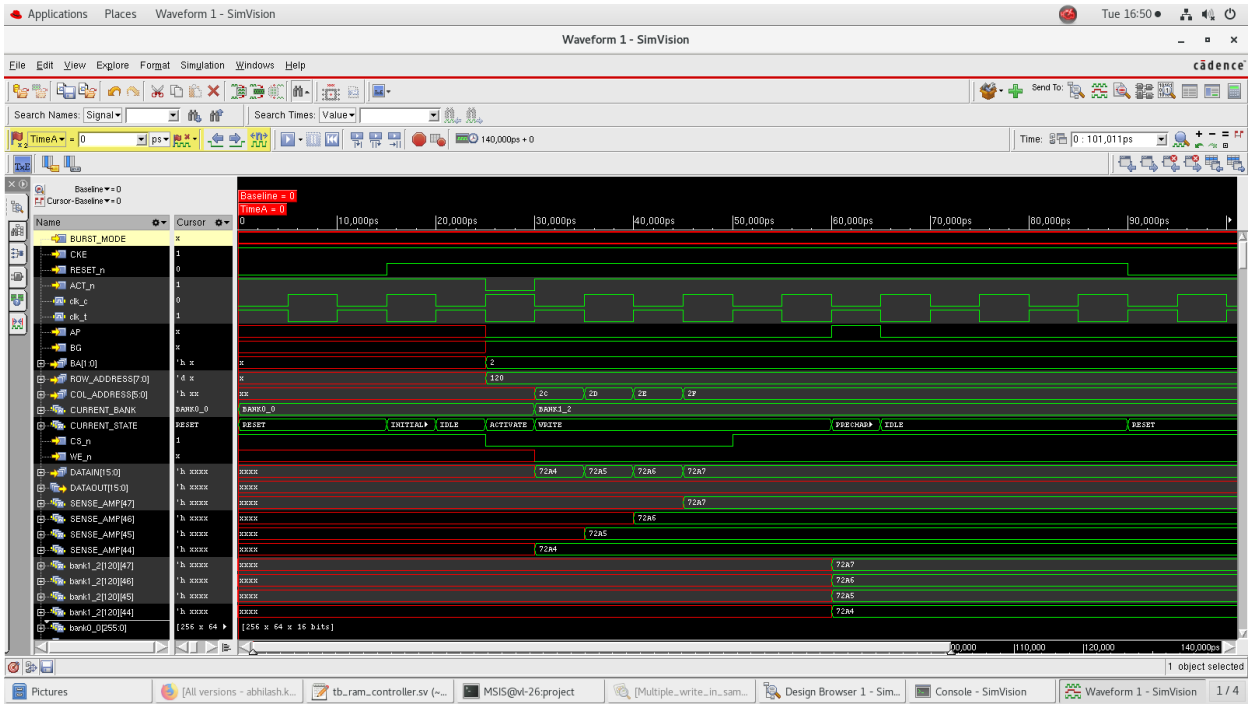

Fig 6.4: Multiple Write operations into a single bank row

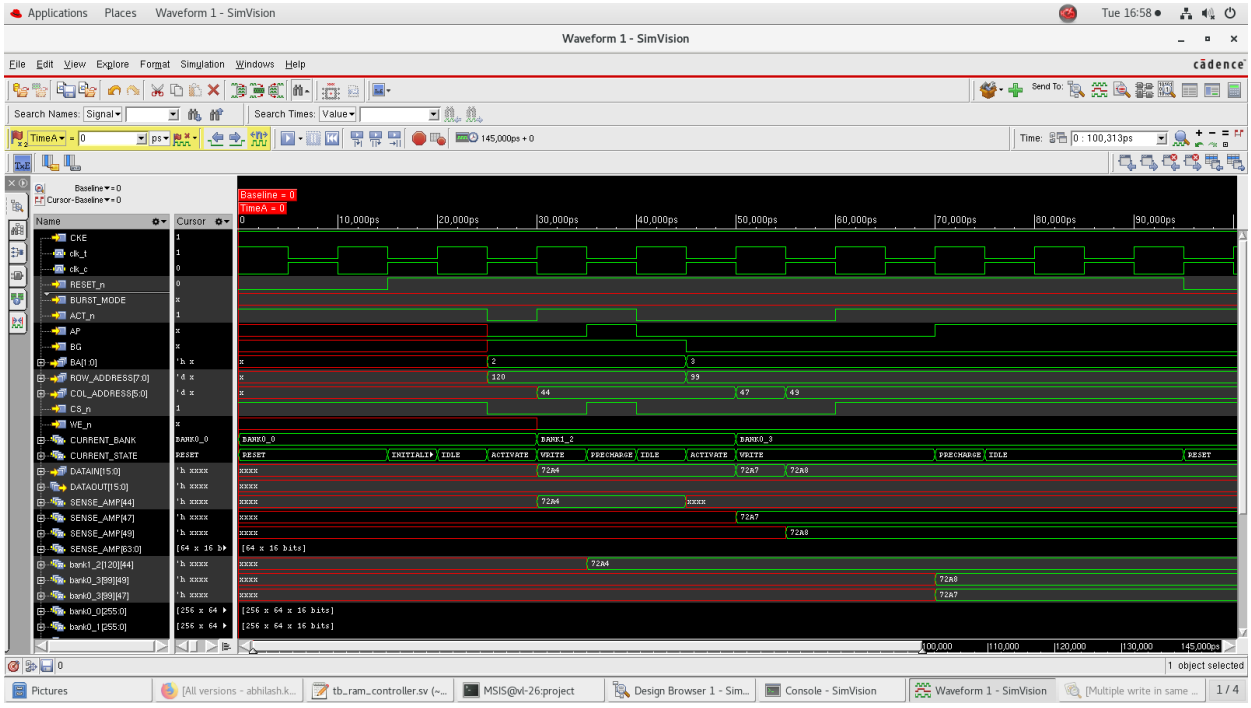

Fig 6.5 Multiple Write operations into a different banks and different rows

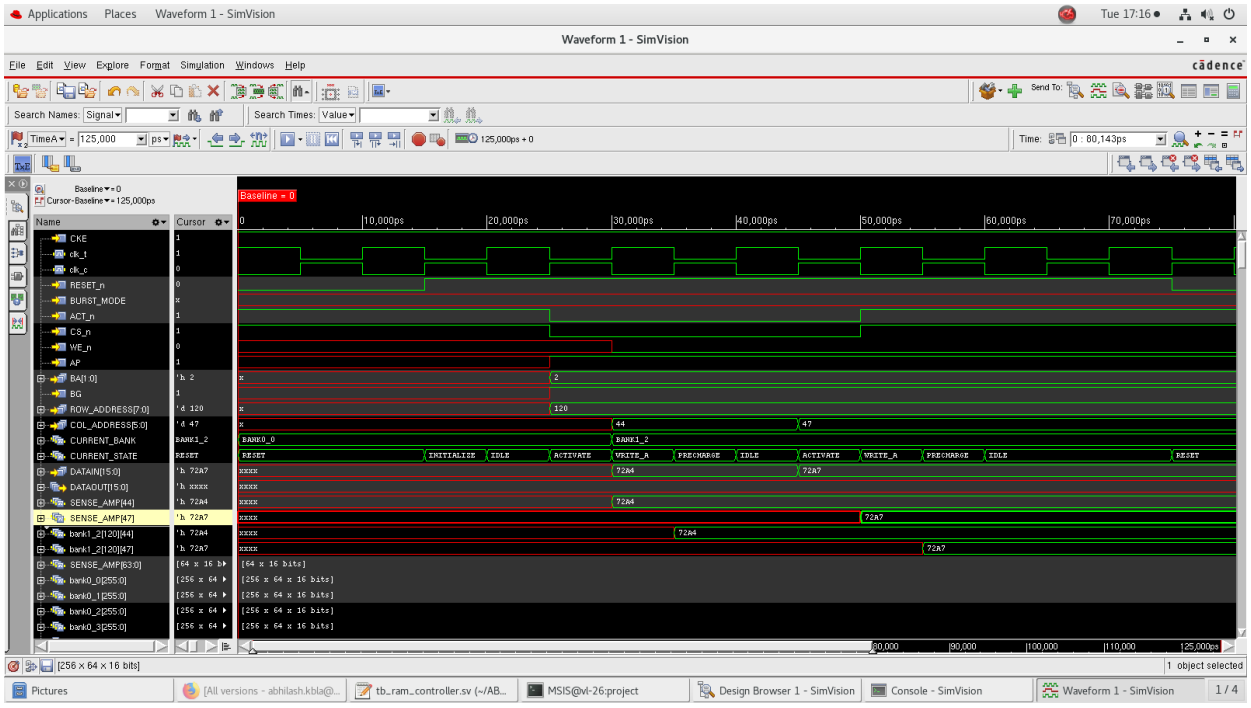

Fig 6.6: Multiple Write operations into a single bank with Auto-Precharge ON

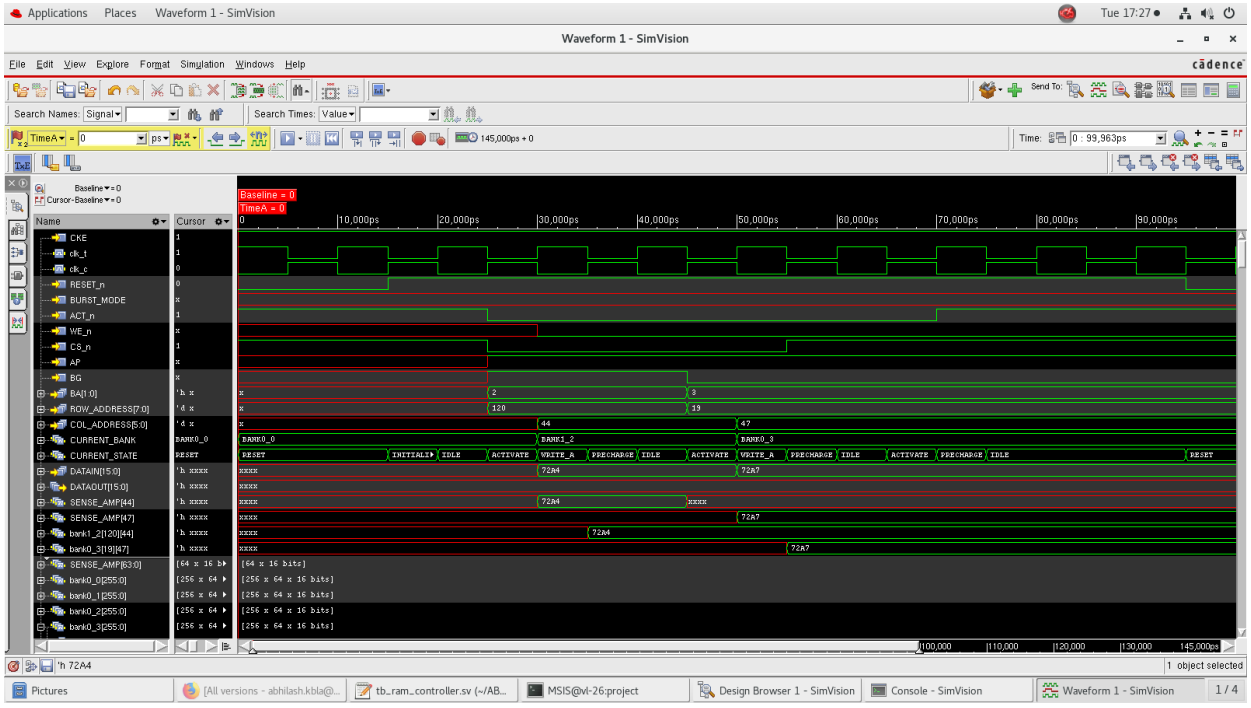

Fig 6.7: Multiple Write operations into different banks with Auto-Precharge ON

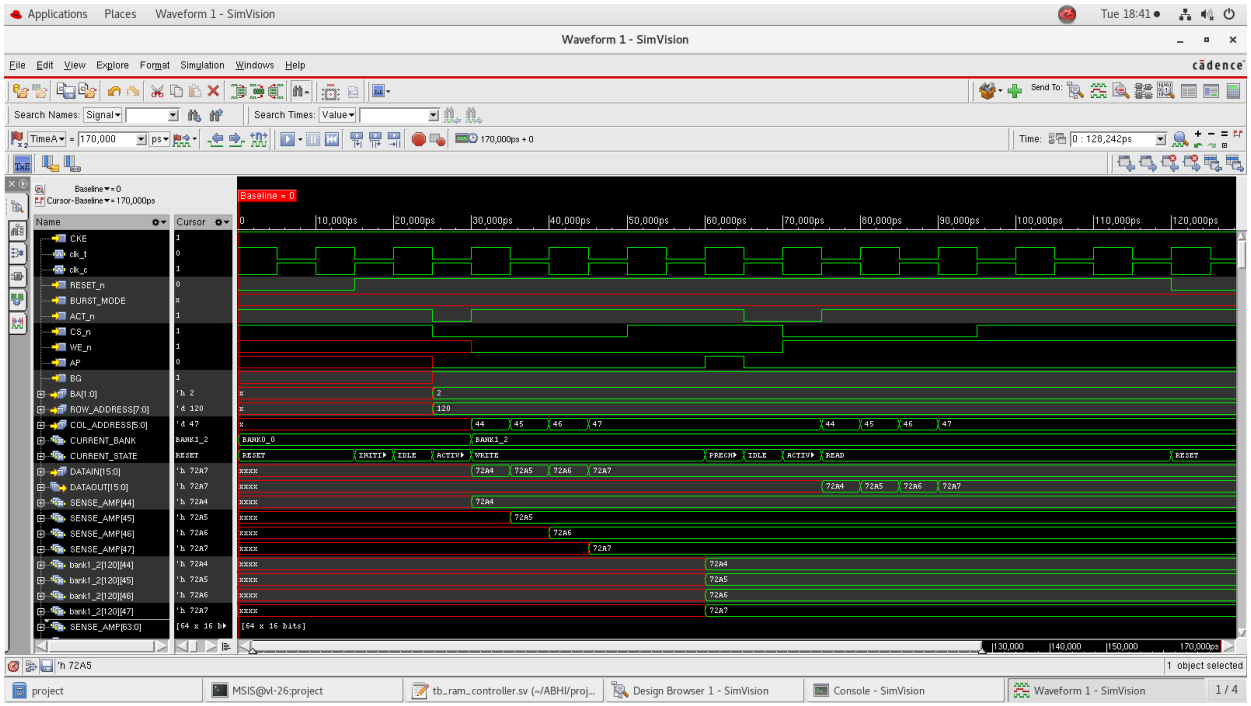

Fig 6.8: Multiple Read operations from a single bank row

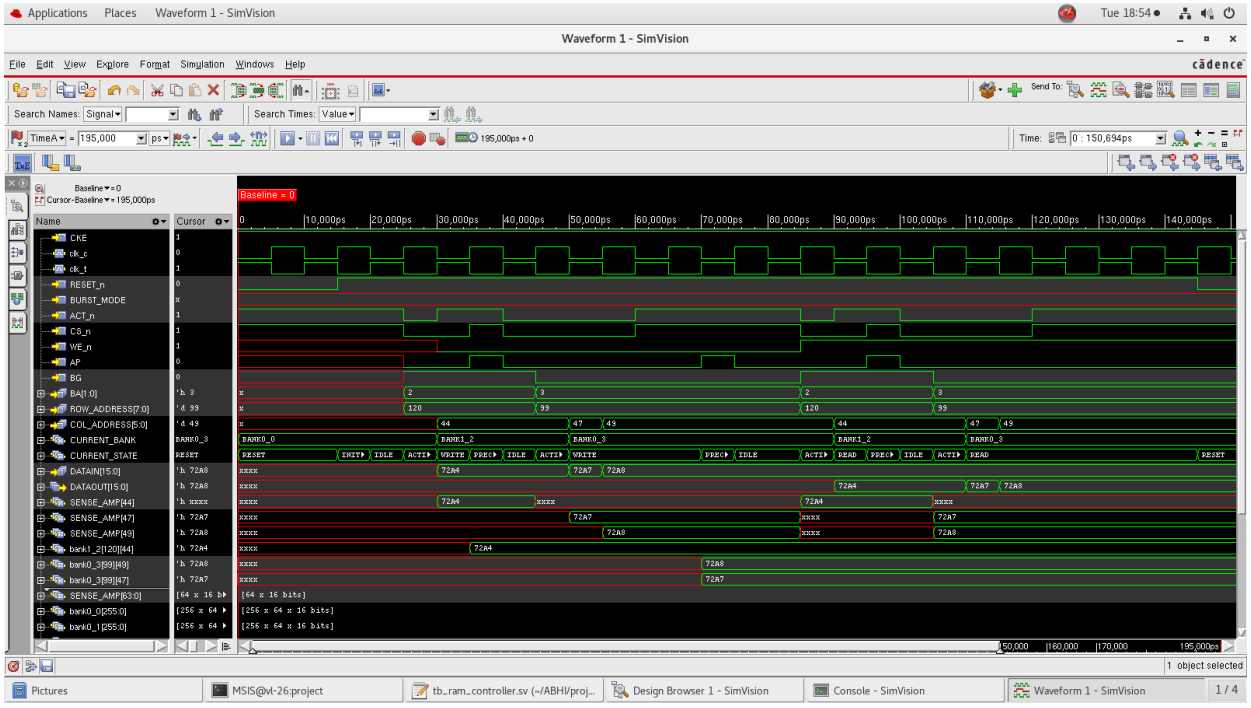

Fig 6.9: Multiple Read operations from different banks

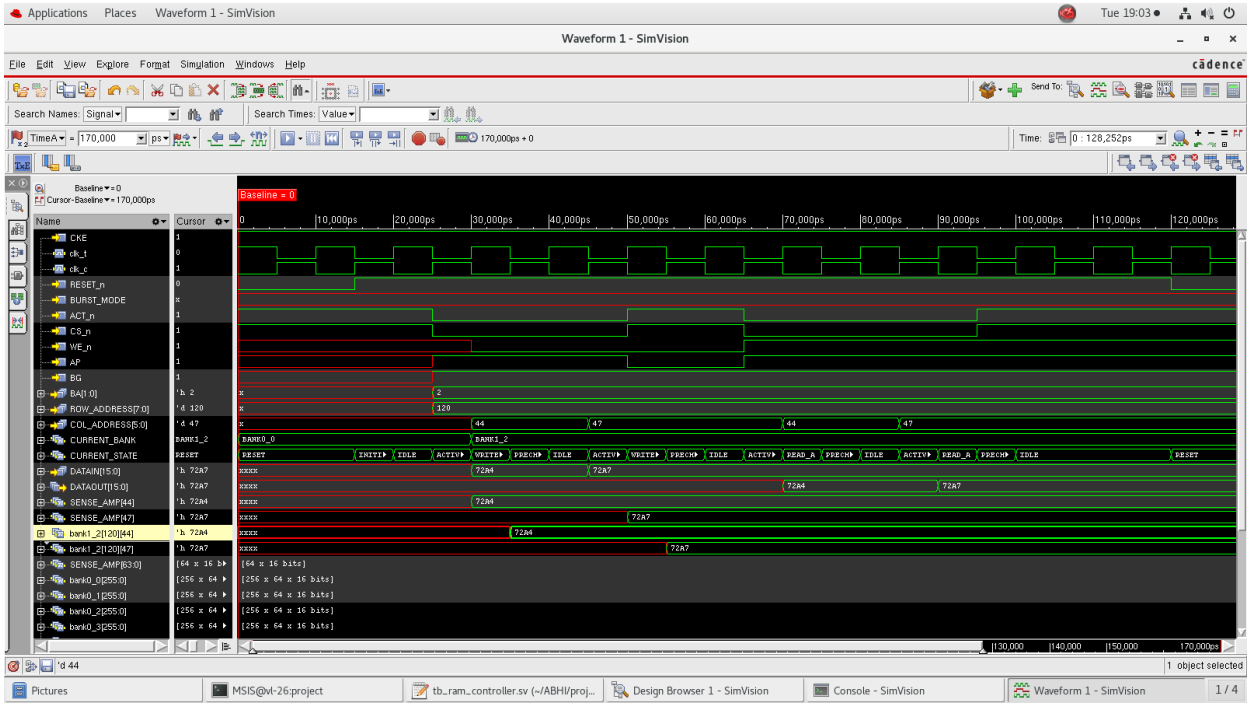

Fig 6.10: Multiple Read operations from a single bank with Auto-Precharge ON

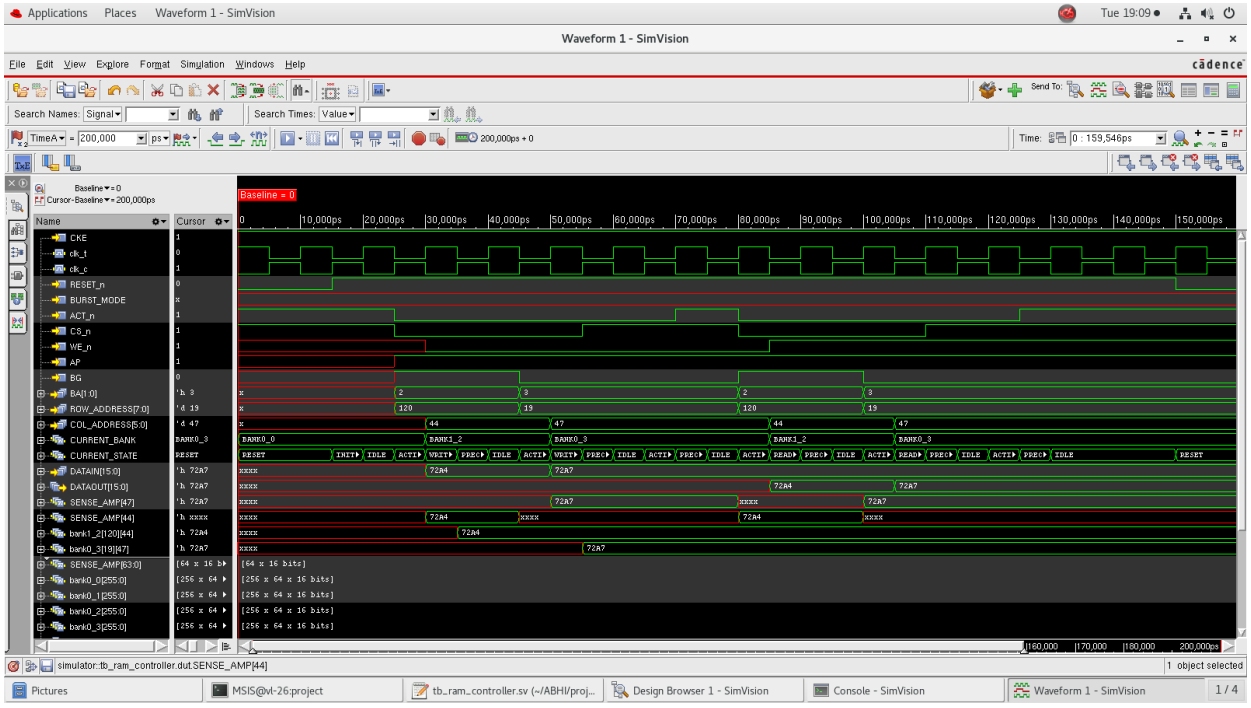

Fig 6.11: Multiple Read operations from different banks with Auto-Precharge ON

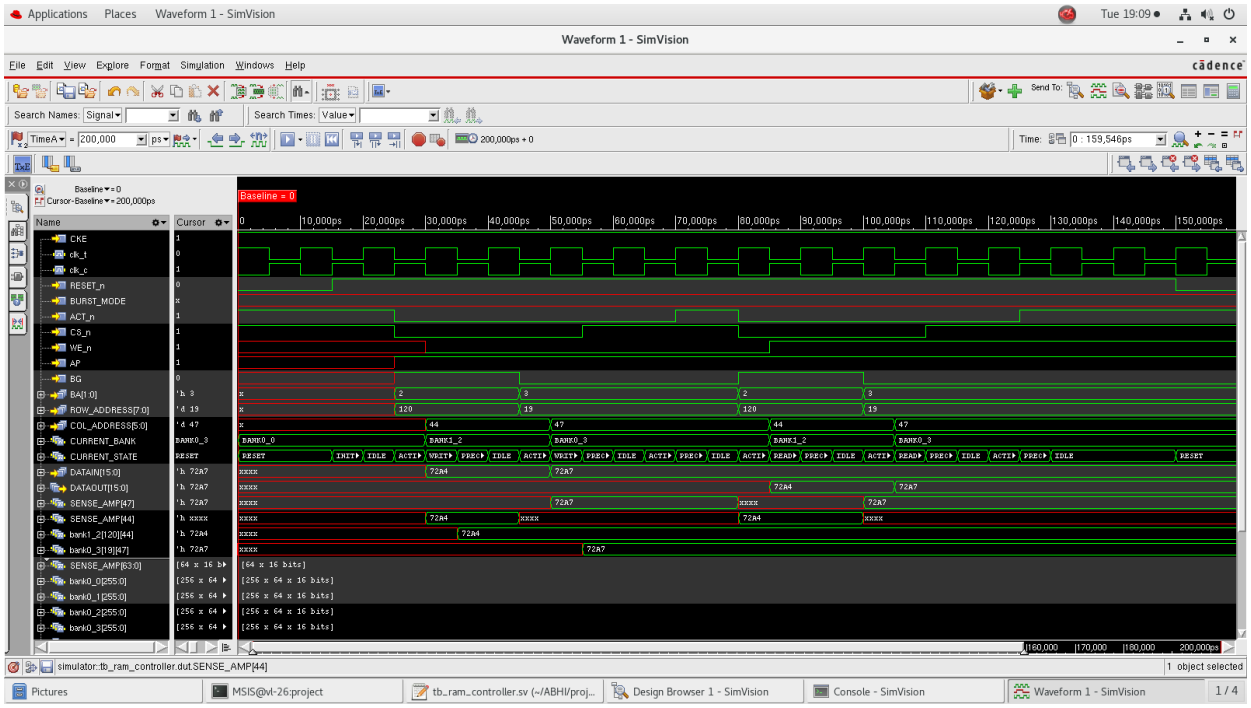

Fig 6.12: Burst Mode Write & Read Operation

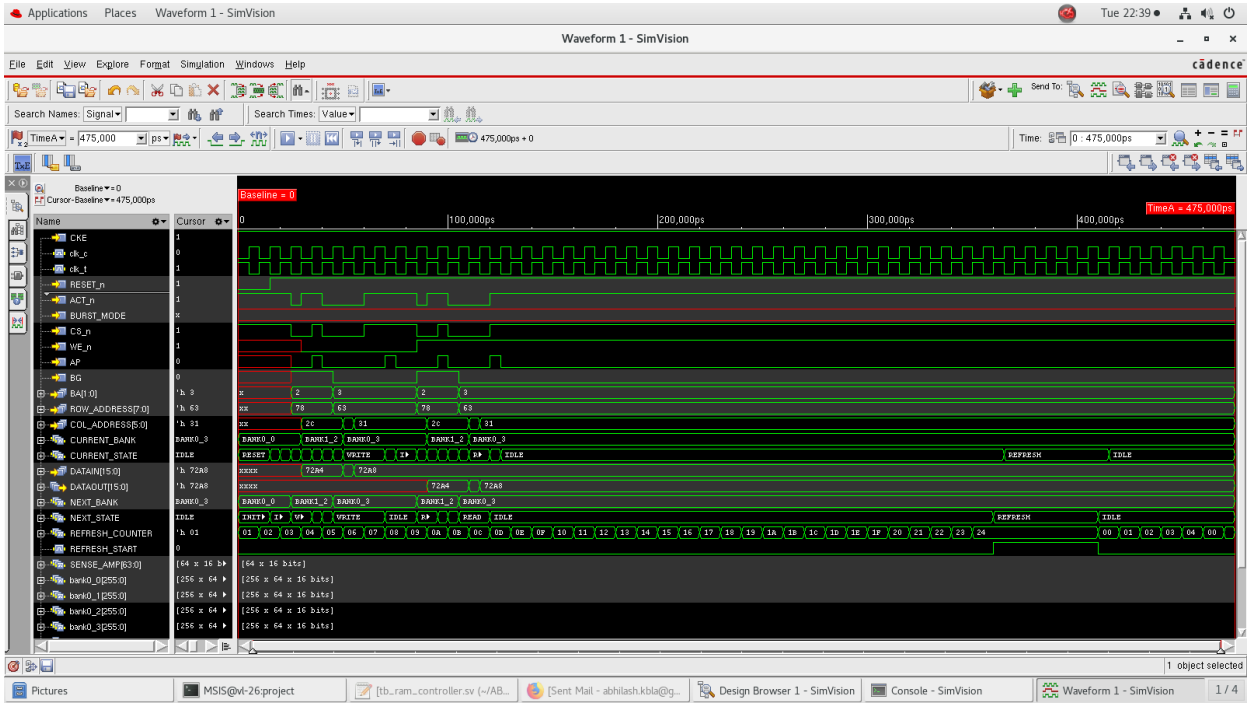

Fig 6.13: Achieving REFRESH state after 360ns

7. Conclusion

The proposed functional DRAM model of the to be designed DDR4 is being implemented and verified under different parameters using System Verilog. DDR4 RAM has achieved Double Data Rate (DDR) with successful read/write operation using both states of burst mode operations. DDR4 has reduced power consumption while also having better transfer rate than its predecessors i.e DDR3, DDR2, DDR.

8. Scope for further work

- The complex schematic uses large number of buffers.This increases the delay. Hence easier schematic reducing the delay can be worked on.
- Error handling feature is not available in DDR4. Error detection and handling can be one of the works that can be carried out for overall improvement of the system.
- Implementation of current DDR4 design is only being done on a simulation tool, which can be implemented on an FPGA to see best results.

9. References

[1] "Design of DDR4 SDRAM controller" – Md. Ashraful Islam, Md. Yeasin Arafath, Md. Jahid Hasan, 8th International conference on Electrical and Computer Engineering, 2014.

[2] "Modelling of DDR4 Memory and Advanced Verifications of DDR4 Memory Subsystems" – Pavan G, V Siddeswara Prasad, International Research Journal of Engineering and Technology (IRJET), 2022.

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