Design of DDR4 using System Verilog

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Presentation Outline

1. Introduction
2. Objectives
3. Block Diagram
4. State Diagram
5. Work done/Results
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1. Introduction

Understanding RAM…

- **Random Access Memory**
  - Short-term memory
  - Faster than hard disk, SSD or other storage devices.

Two types of RAM

- **SRAM** – Static RAM
  - Retains data bits in memory as long as power is being supplied.
- **DRAM** – Dynamic RAM
  - Retains data bits in memory as long as continuous external periodic refresh is supplied.

Types of DRAM

- SDRAM – Synchronous DRAM
- ECC DRAM – Error Correcting Code DRAM
- DDR SDRAM, DDR2, DDR3, DDR4 – Double Data Rate (DDR) Version 4

2. Objectives

Main objectives of designing DDR4 RAM:

- Memory operation with multiple bank groups/banks.
- Read/Write operations with Double Data Rate(DDR).
- Burst Read/Write operation.

3. Block Diagram

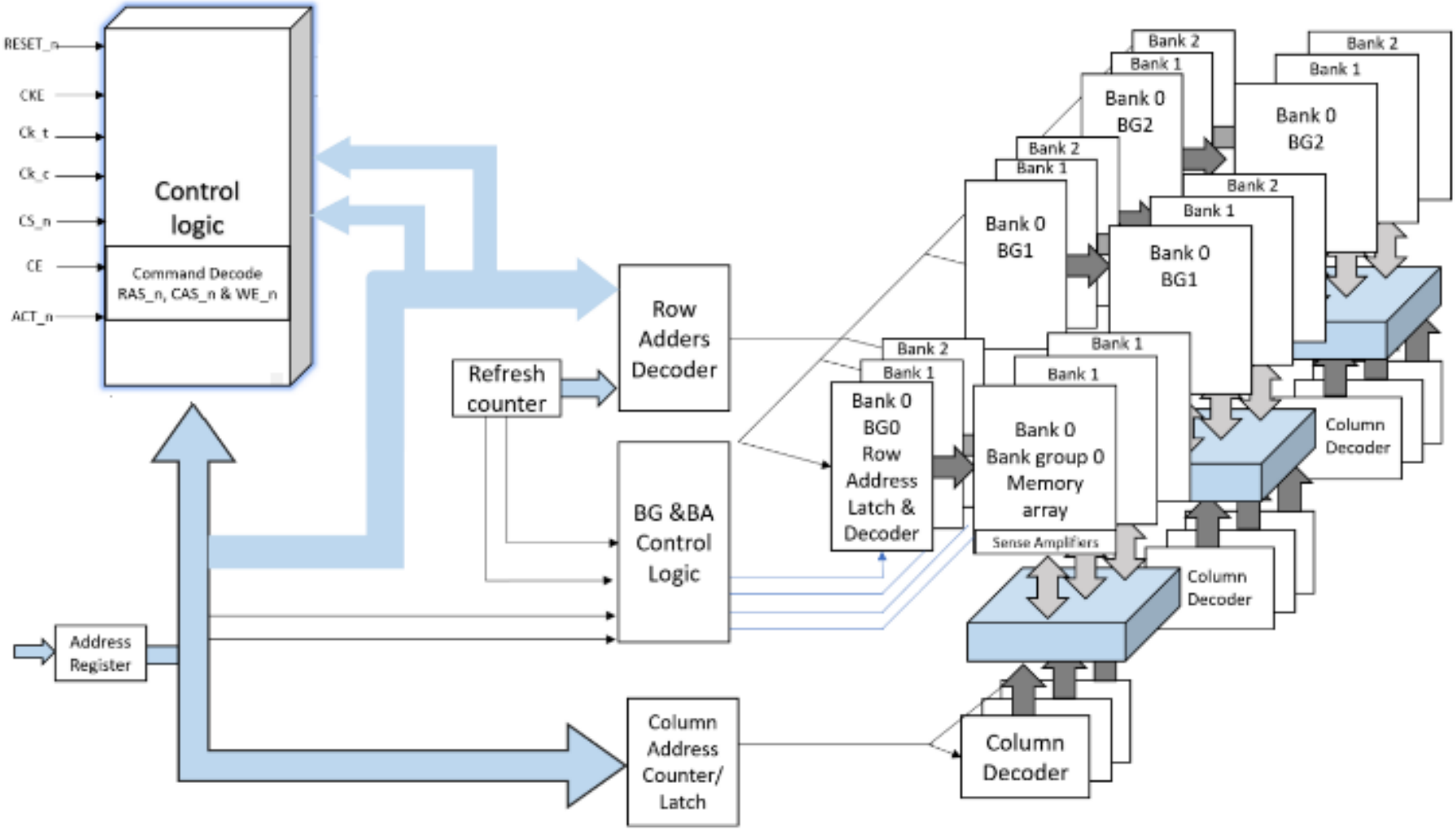

Figure 1: Functional Block Diagram of DDR4[2]

4. State Diagram

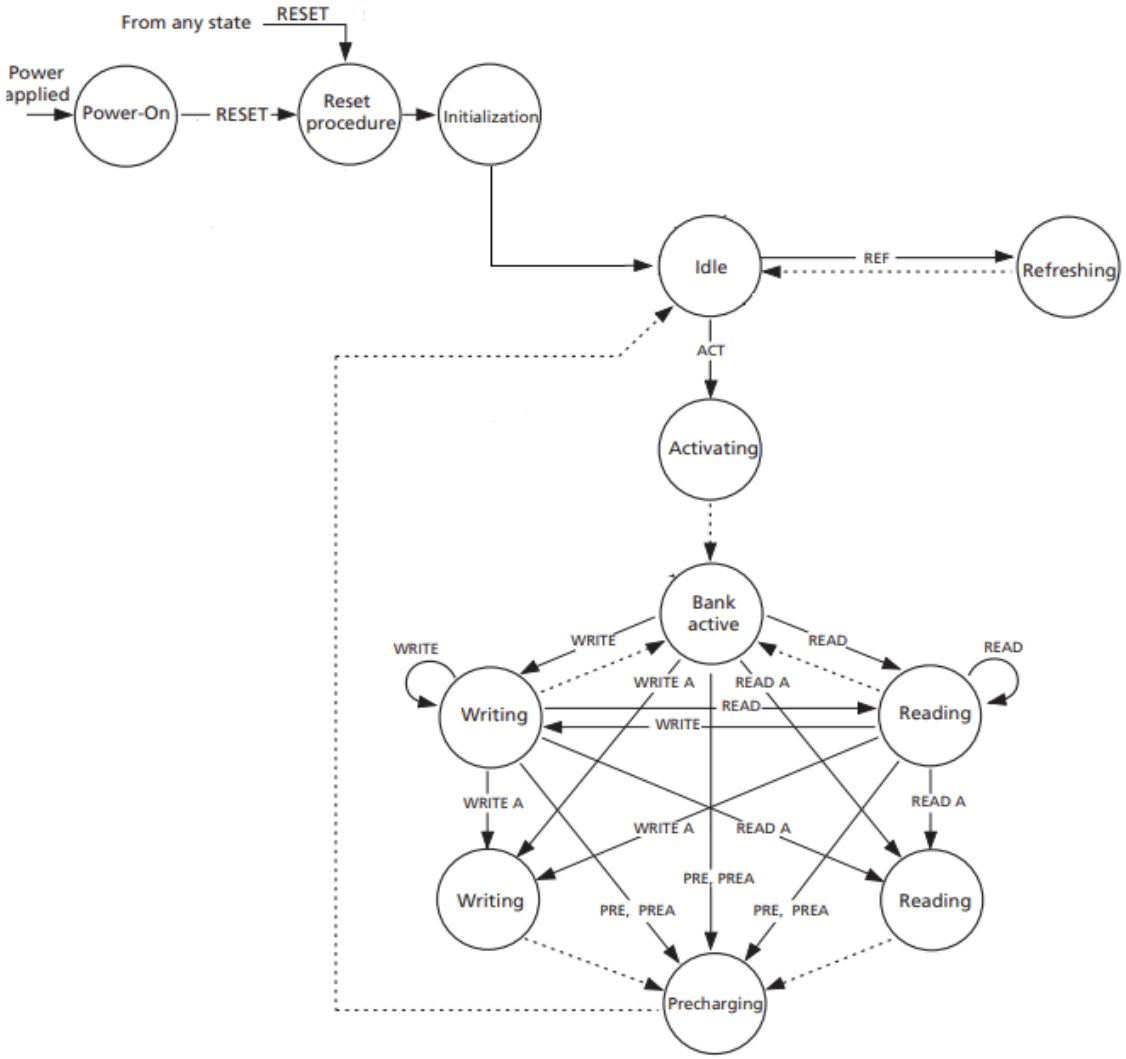

Figure 2: State diagram of DDR4 SDRAM[1]

5. Work done/Results

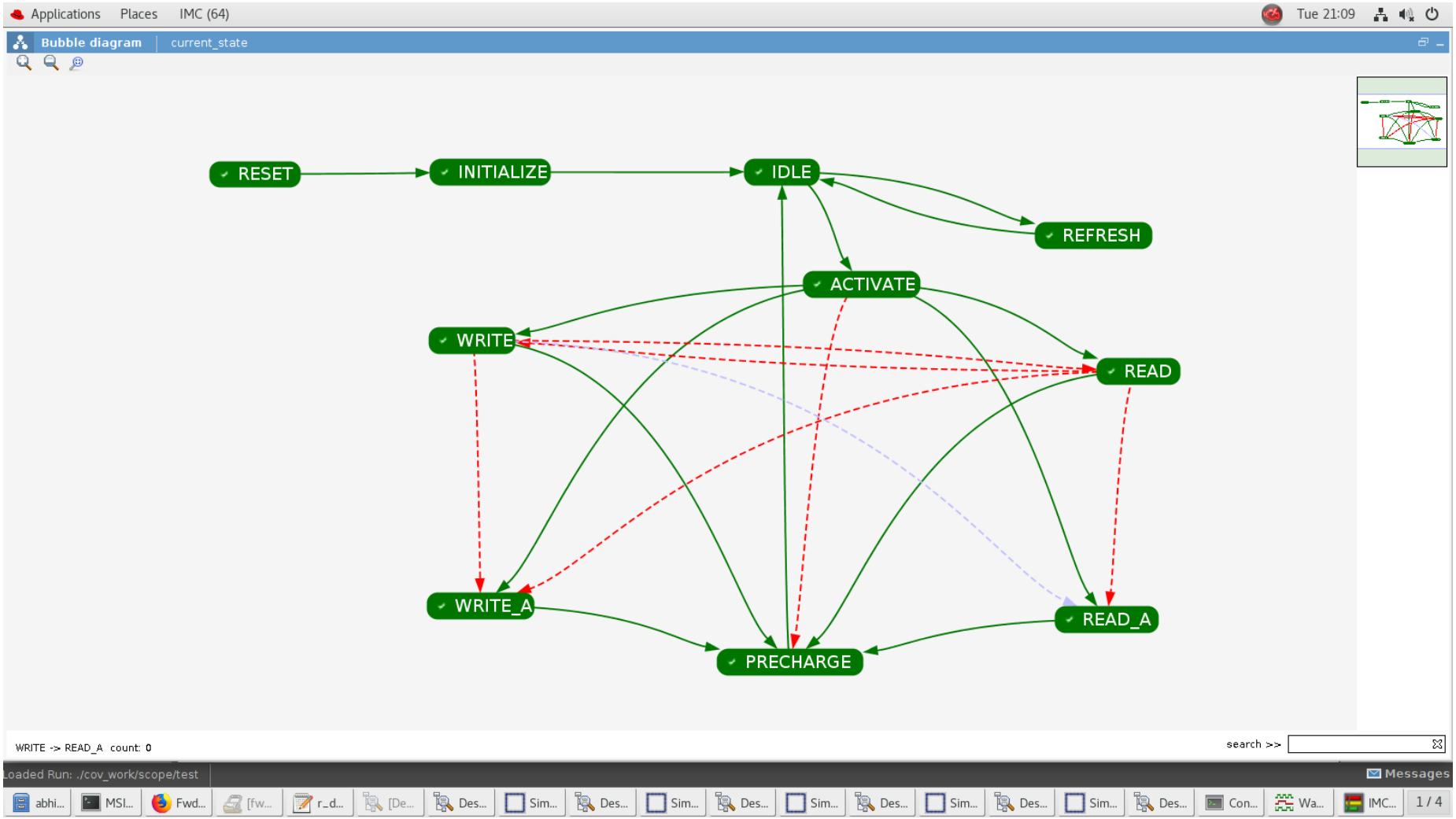

Fig 3: Verified FSM coverage of simulated DDR4 SDRAM

5. Work done/Results

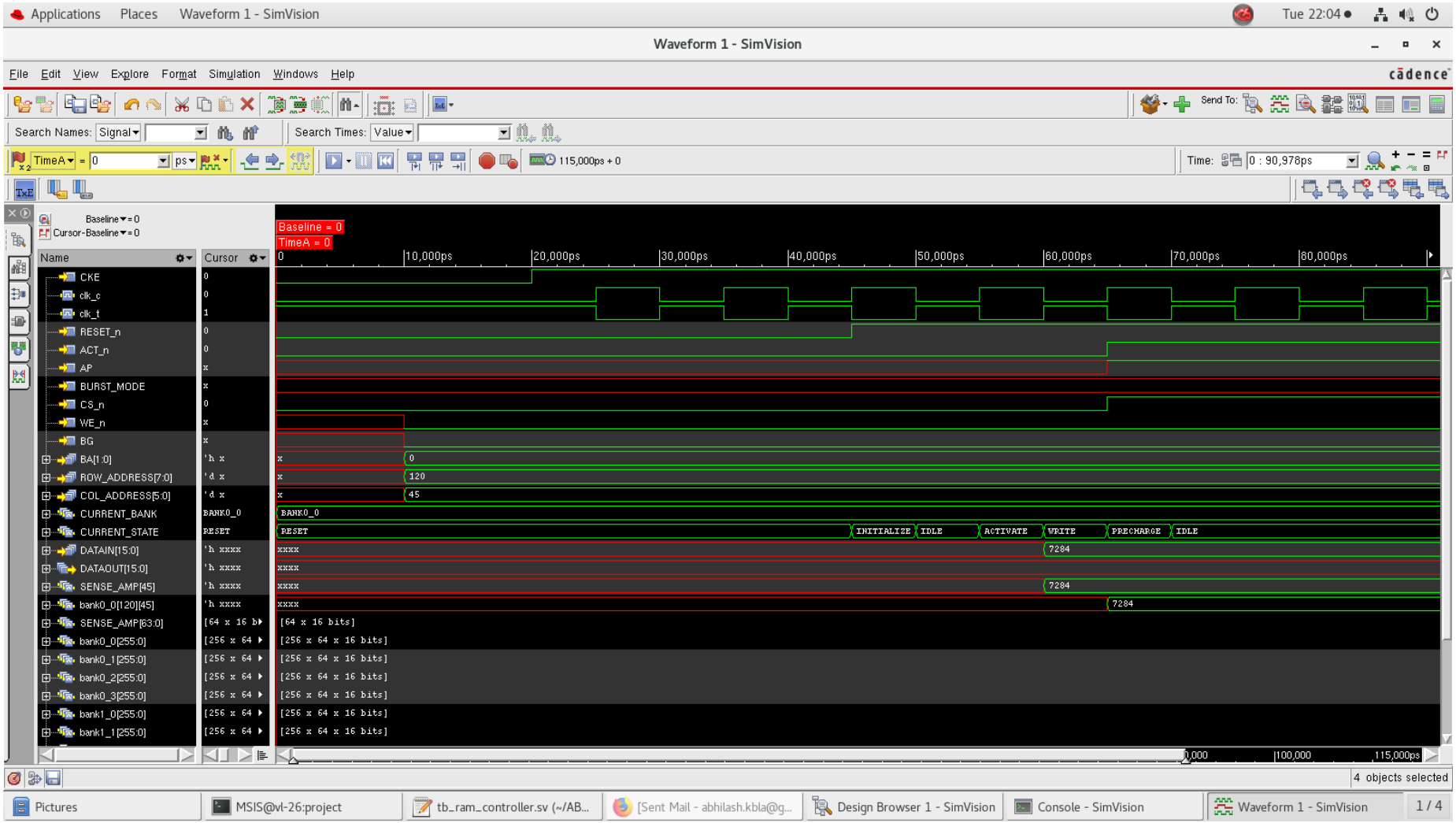

Fig 4: Displaying RESET & CKE(Clock Enable) activity when both become active

5. Work done/Results

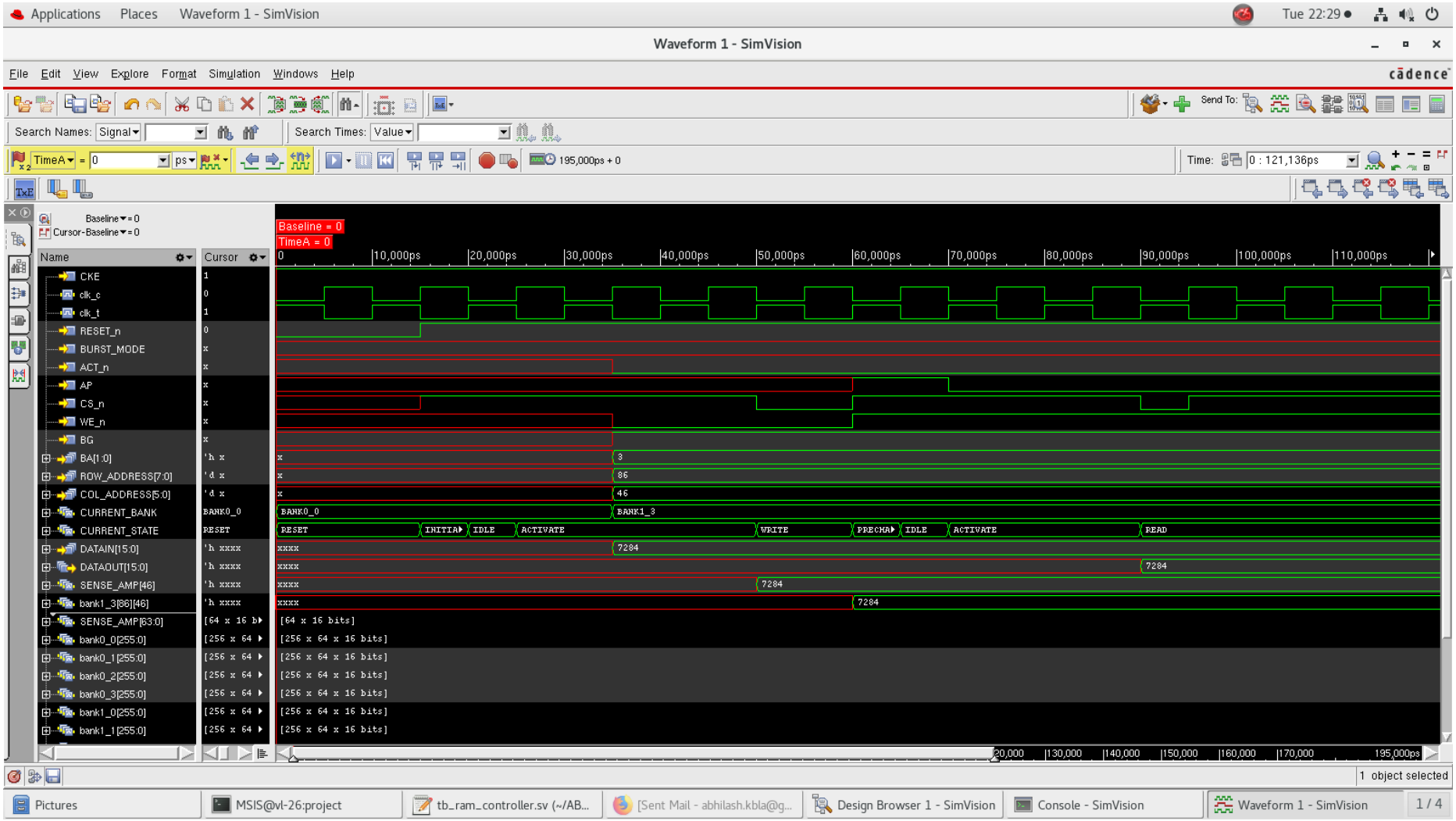

Fig 5: Functioning of READ/WRITE operation only when CS(Chip Select) is active

5. Work done/Results

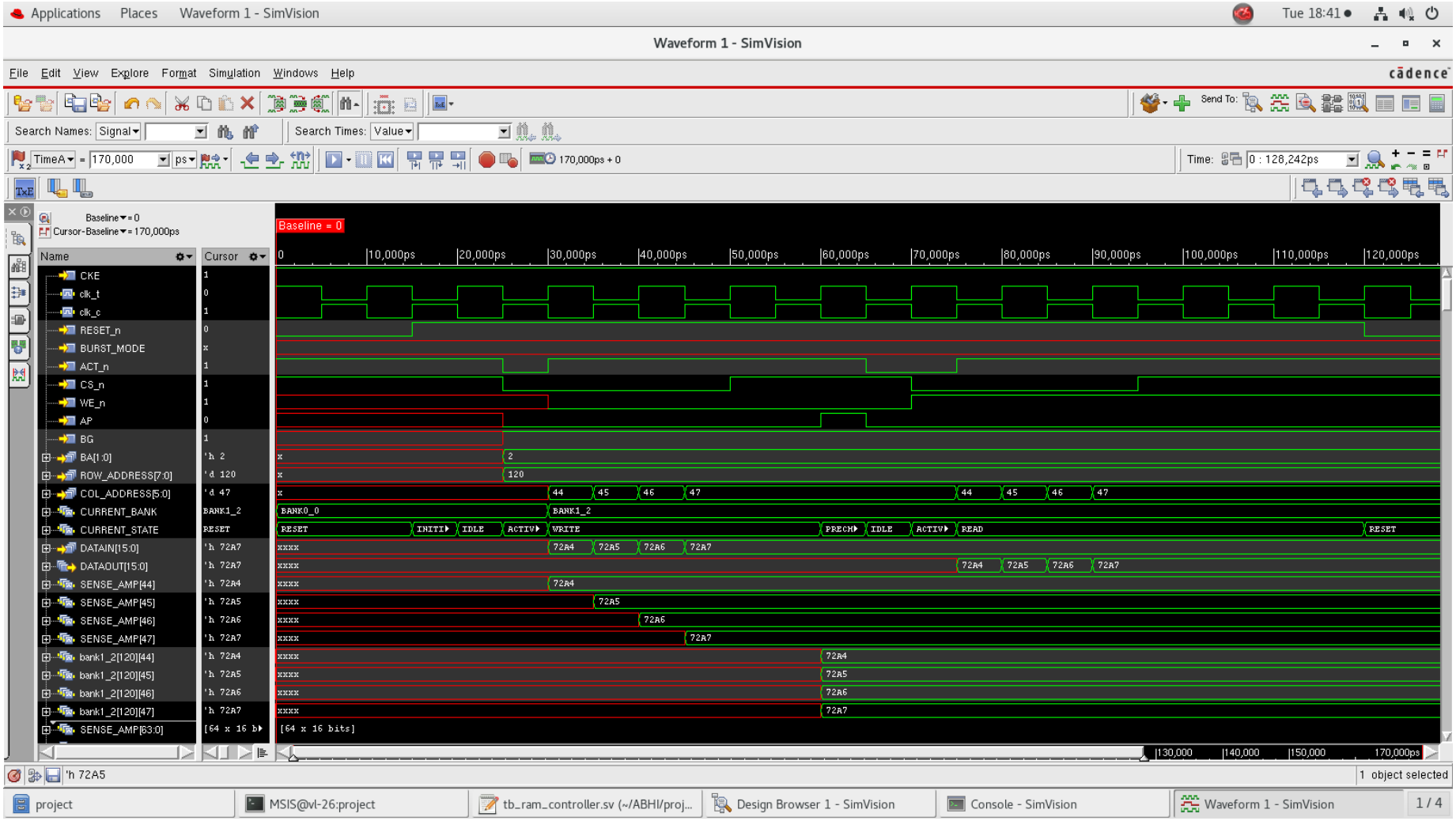

Fig 6: Multiple Write/Read operations from a single bank row

5. Work done/Results

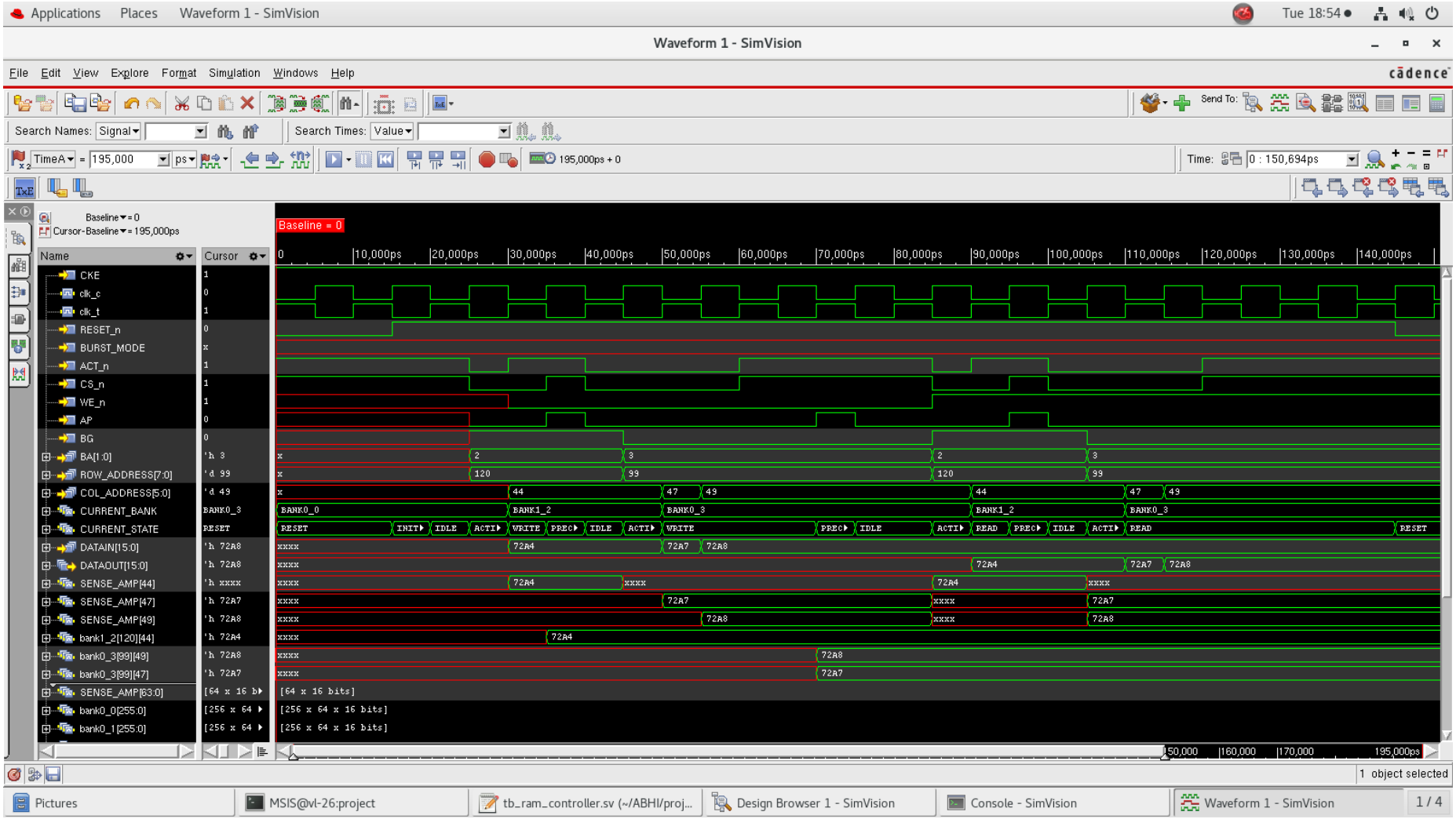

Fig 7: Multiple Write/Read operations from different banks

5. Work done/Results

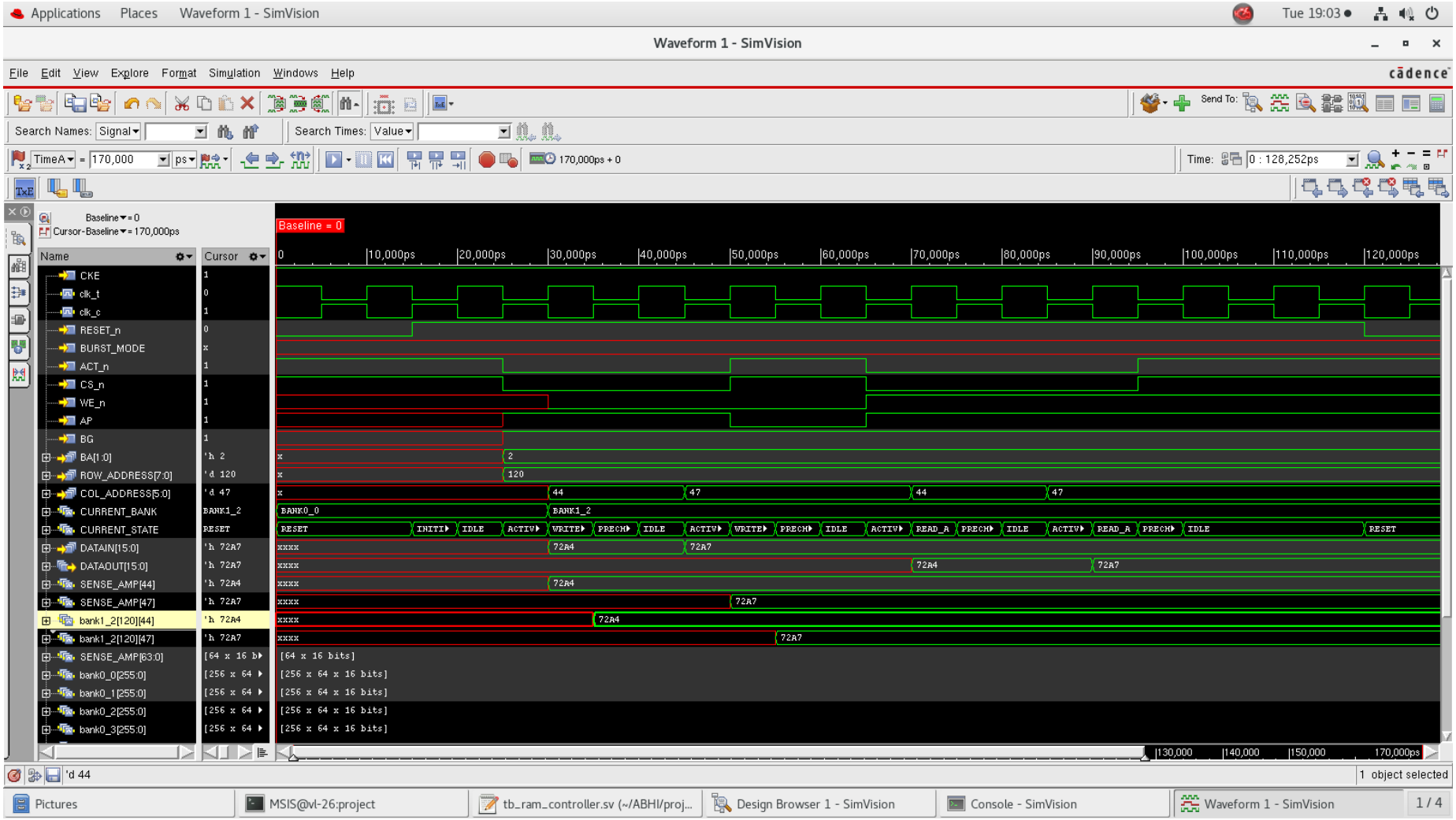

Fig 8: Multiple Write/Read operations from a single bank with Auto-Precharge ON

5. Work done/Results

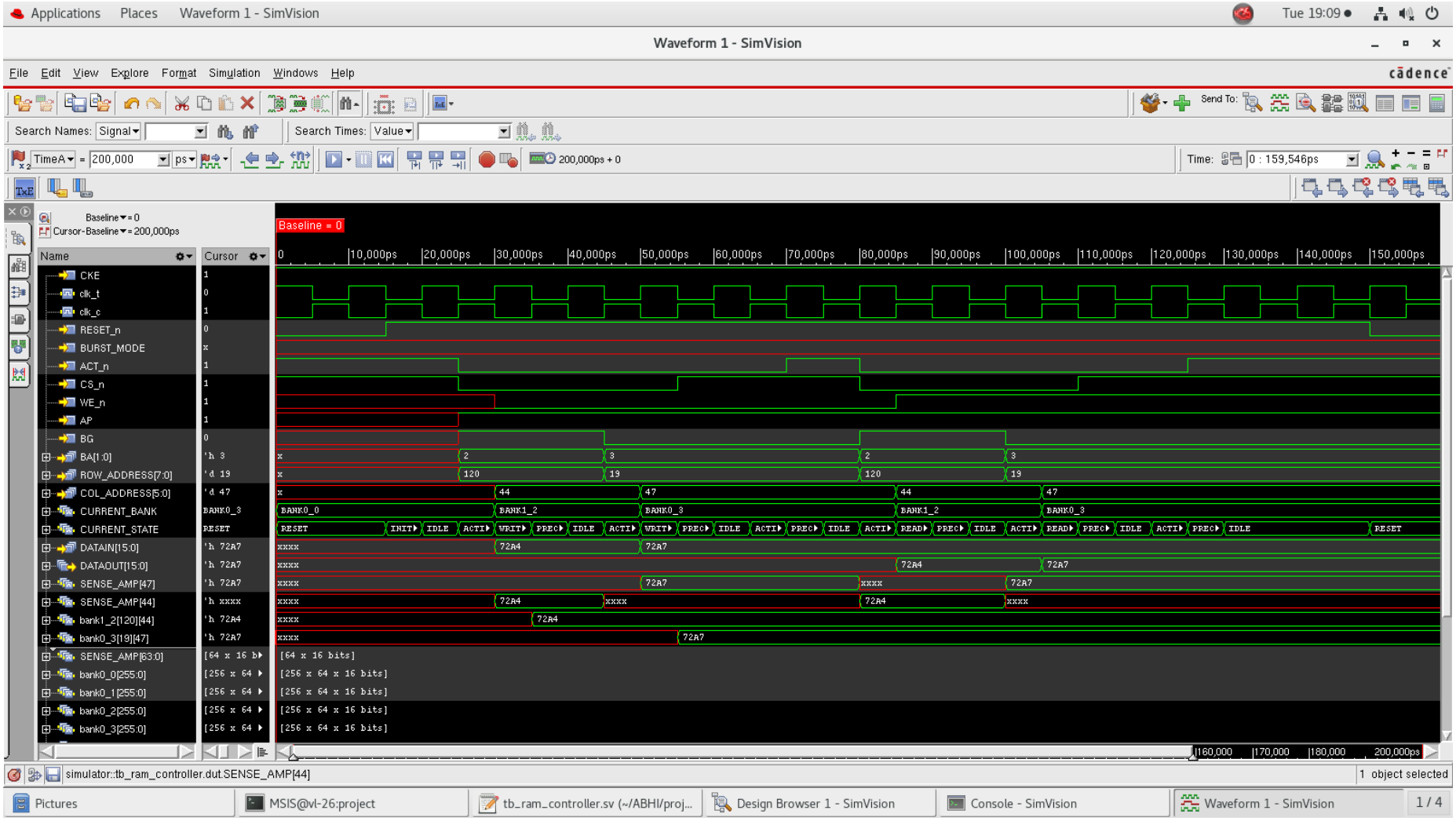

Fig 9: Multiple Write/Read operations from different banks with Auto-Precharge ON

5. Work done/Results

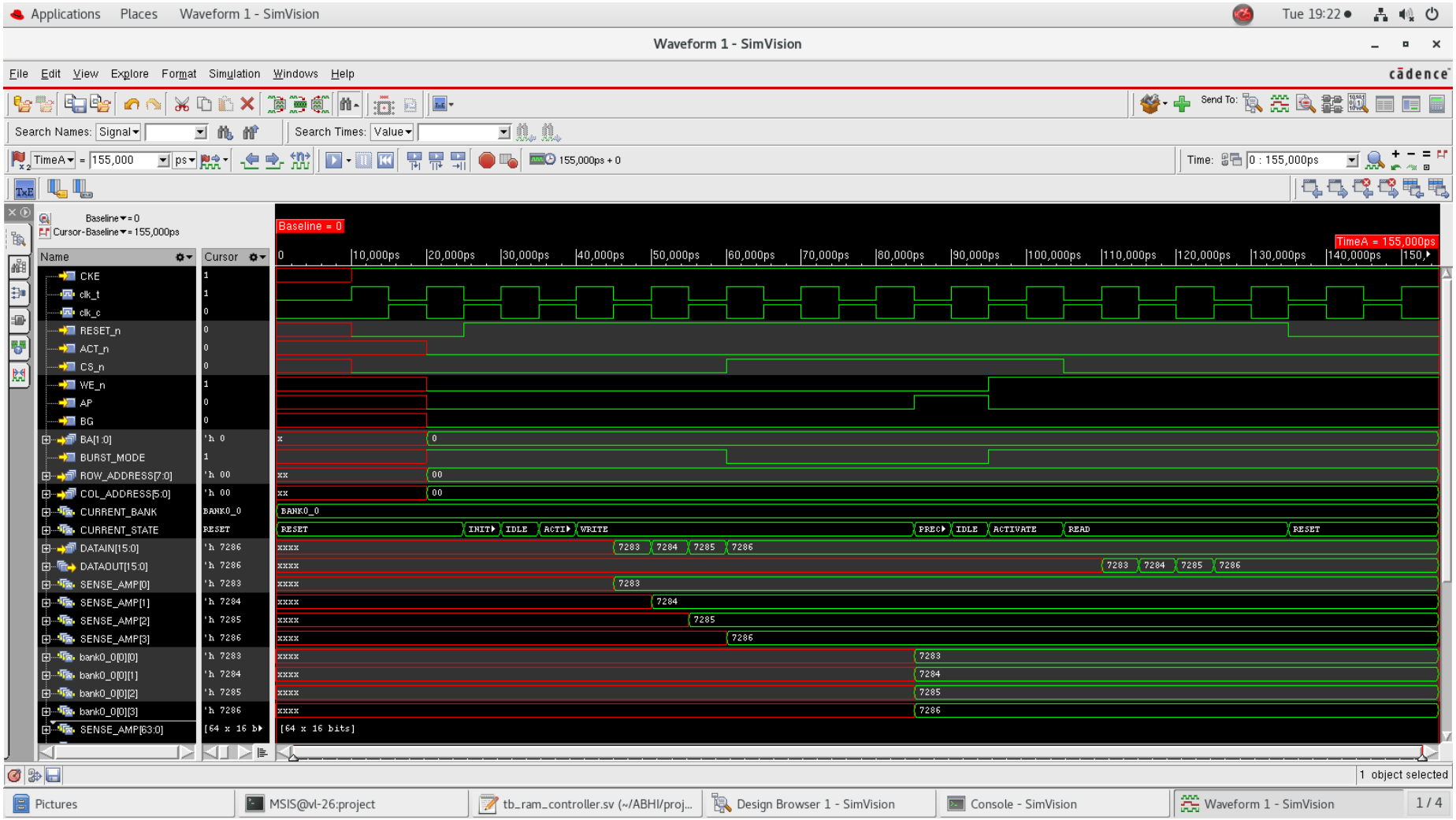

Fig 10: Burst Mode Write & Read Operation

5. Work done/Results

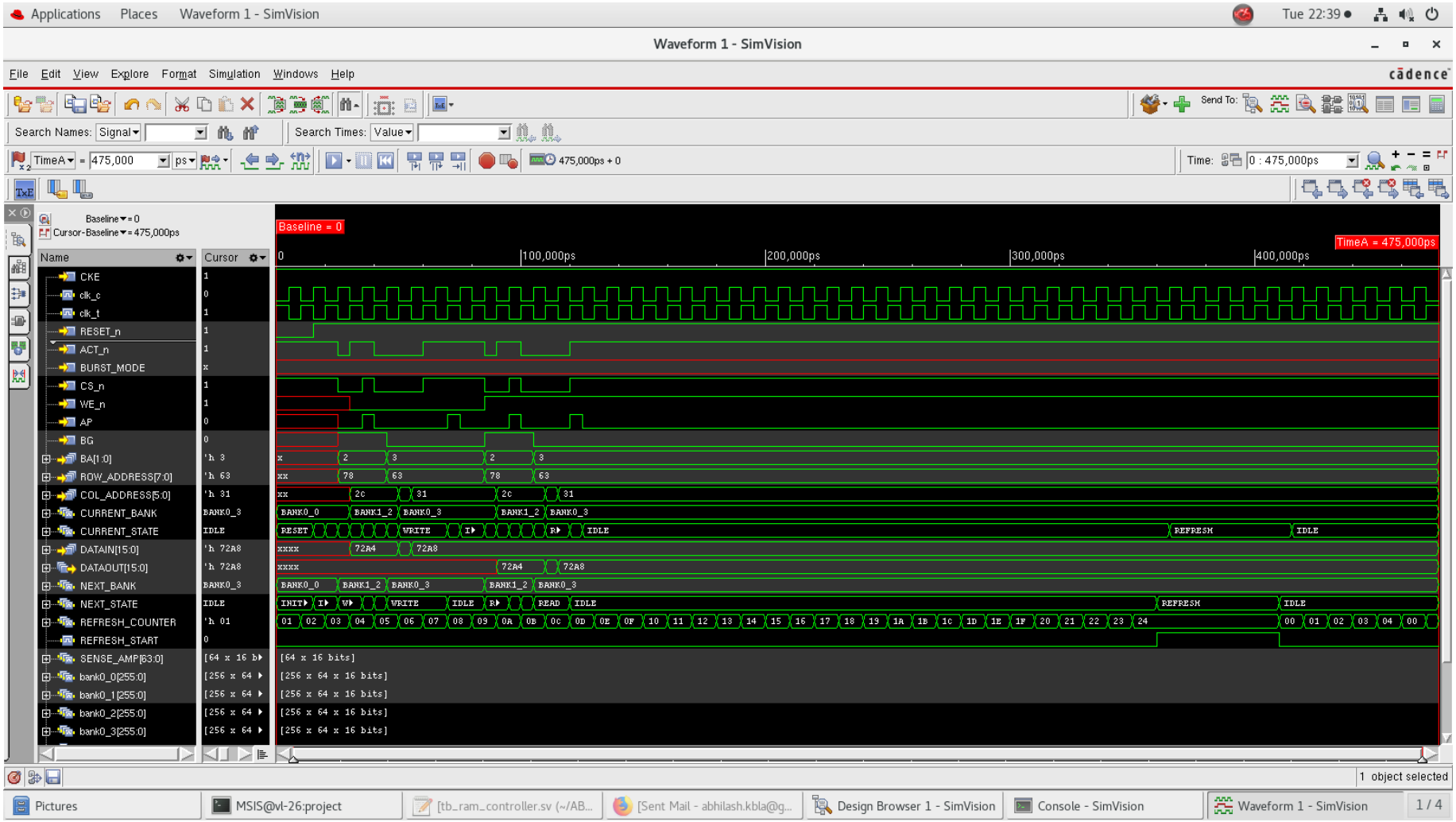

Fig 11: Achieving REFRESH state after 360ns

6. Conclusion

- The proposed functional DRAM model of the to be designed DDR4 is being implemented and verified under different parameters using System Verilog for a series of testbench cases.
- DDR4 RAM has achieved Double Data Rate (DDR) with successful read/write operation using both states of burst mode operations.

7. References

- **[1]** "Design of DDR4 SDRAM controller" – Md. Ashraful Islam, Md. Yeasin Arafath, Md. Jahid Hasan, 8th International conference on Electrical and Computer Engineering, 2014.
- **[2]** "Modelling of DDR4 Memory and Advanced Verifications of DDR4 Memory Subsystems" – Pavan G, V Siddeswara Prasad, International Research Journal of Engineering and Technology (IRJET), 2022.
- **[3]** Micron Technology Inc. Double Data Rate controller SDRAM data sheet.
- **[4]** JEDEC Standard, DDR4 SDRAM, JESD79-4, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.
- **[5]** "Design and Implementation of DDR4 SDRAM Controller Based on FPGA" 2nd IEEE Advanced Information Management, Communicates, Electronic and Automation Control Conference (IMCEC 2018), Jia Zheng, Kai Yan, Yue Zhang, Zengping Chen.
- **[6]** DDR4 SDRAM – Understanding the basics – "https://www.systemverilog.io/ddr4-basics"

Queries
&
Suggestions

THANK YOU…