Assignment-08
Design and Implementation of a Digital Synchronous UP/DOWN Counter

EE24BTECH11021-ESHAN RAY
EE24BTECH11048-NITHIN.K

April 8, 2025

1 Objective

To design and implement a **digital up/down counter** that displays the number of people currently in the mess during peak lunch hours. The system will help students decide whether they can enter the mess based on the current occupancy. The maximum count is set to **99**.

2 Components and Equipments

S.NO	Name of Material	Quantity
1	Dual J-K Flip-Flop(7476 ic)	4
2	Triple 3-Input AND gate(7411 ic)	12
3	Quad OR gate(7432 ic)	4
4	Pushbutton	2
5	Arduino/Power supply(5V)	1
6	Resistors(300 Ω)	2
7	Resistors(1 KΩ)	2
8	7-Segment Display	2
9	7-Segment Decoder(7447 ic)	2
10	Breadboard	5
11	Jumper wires	As much as required

3 Procedutre

3.1 System Design and Working Principle

1. The IR sensors or ultrasonic sensors will be placed at the entry and exit points of the mess. But the same can be simulated using Buttons if the IR sensors are not available.
2. When a person enters, the system increments the count (Up Counter).
3. When a person leaves, the system decrements the count (Down Counter).
4. The count is displayed on a 7-segment display.
5. The Circuit is made up of only Logic gates and T flip-flops made from JK flip-flops.
6. The outputs are then connected to a BCD decoder and then to a 7 Segment common anode display to show the count.

4 Circuit Design

The T flip flop can be constructed from JK flip flop from the truth table shown below

Q	**J**	**K**	**T**	**Q(next state)**
0	0	X	0	0
0	1	X	1	1
1	X	0	0	1
1	X	1	1	0

From the table above we can conclude that $\mathbf{J = K = T}$.

4.1 State Transition Table For UP counter:

Current State				Next State			
Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

Truth Table For UP counter:

Q3	**Q2**	**Q1**	**Q0**	**T3**	**T2**	**T1**	**T0**	**Q3-next**	**Q2-next**	**Q1-next**	**Q0-next**
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	1	0	0	1	0
0	0	1	0	0	0	0	1	0	0	1	1
0	0	1	1	0	1	1	1	0	1	0	0
0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	0	1	1	0	1	1	0
0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	1	1	1	1	1	0	0	0
1	0	0	0	0	0	0	1	1	0	0	1
1	0	0	1	1	0	0	1	0	0	0	0
1	0	1	0	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X

It is Obvious that T_0 is always 1 and for the remaining you have the below K-Maps

Q3Q2 \ Q1Q0	00	01	11	10
00				
01			1	
11	X	X	X	X
10		1	X	X

$$T_3 = Q_3Q_0 + Q_2Q_1Q_0$$

Q3Q2 \ Q1Q0	00	01	11	10
00			1	
01			1	
11	X	X	X	X
10			X	X

$$T_2 = Q_1Q_0$$

Q3Q2 \ Q1Q0	00	01	11	10
00		1	1	
01		1	1	
11	X	X	X	X
10			X	X

$$T_1 = \overline{Q_3}Q_0$$

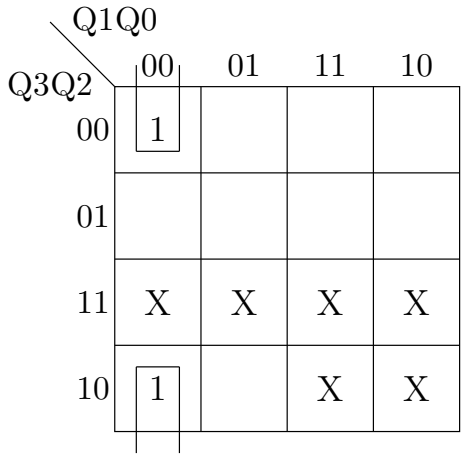
4.2 State Transition Table For DOWN counter:

Current State				Next State			
Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
1	0	0	1	1	0	0	0
1	0	0	0	0	1	1	1
0	1	1	1	0	1	1	0
0	1	1	0	0	1	0	1
0	1	0	1	0	1	0	0
0	1	0	0	0	0	1	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	1

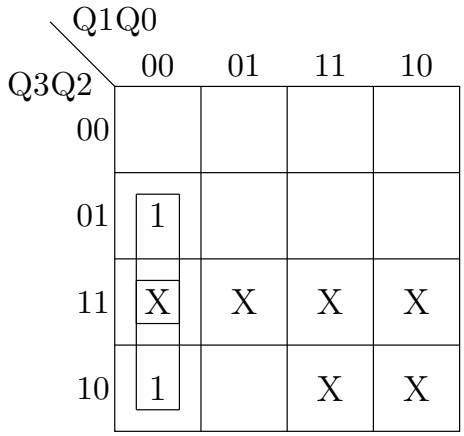
Truth Table For DOWN counter:

Q3	**Q2**	**Q1**	**Q0**	**T3**	**T2**	**T1**	**T0**	**Q3-next**	**Q2-next**	**Q1-next**	**Q0-next**
1	1	1	1	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X
1	0	1	0	X	X	X	X	X	X	X	X
1	0	0	1	0	0	0	1	1	0	0	0
1	0	0	0	1	1	1	1	0	1	1	1
0	1	1	1	0	0	0	1	0	1	1	0
0	1	1	0	0	0	1	1	0	1	0	1
0	1	0	1	0	0	0	1	0	1	0	0
0	1	0	0	0	1	1	1	0	0	1	1
0	0	1	1	0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0	0	0	1
0	0	0	1	0	0	0	1	0	0	0	0
0	0	0	0	1	0	0	1	1	0	0	1

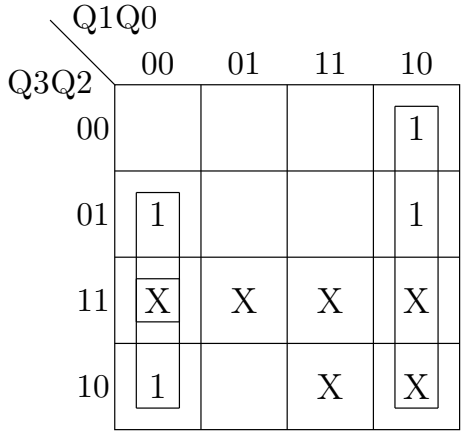
It is Obvious that T_0 is always 1 and for the remaining you have the below K-Maps



$$T_3 = \overline{Q_2}T,\ T = \overline{Q_1}\,\overline{Q_0}$$



$$T_2 = (Q_2 + Q_3)T,\ T = \overline{Q_1}\,\overline{Q_0}$$



$$T_1 = Q_1\overline{Q_0} + T_2$$

4.3 Circuit Diagram

The figures below are taken from Tinkercad simulated by us.

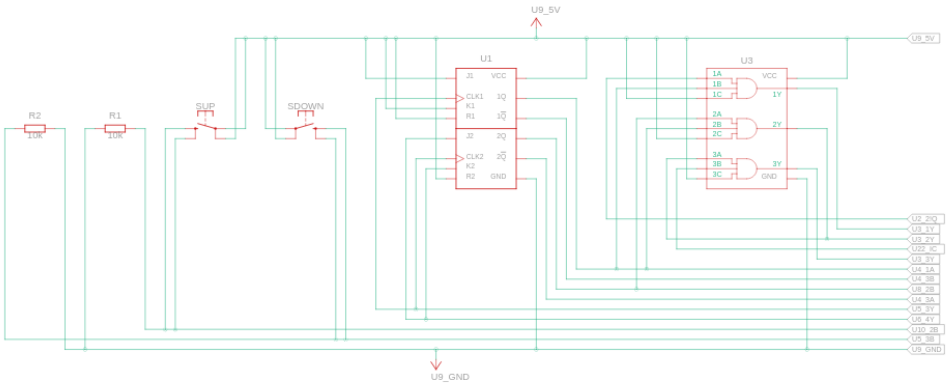


Figure 1

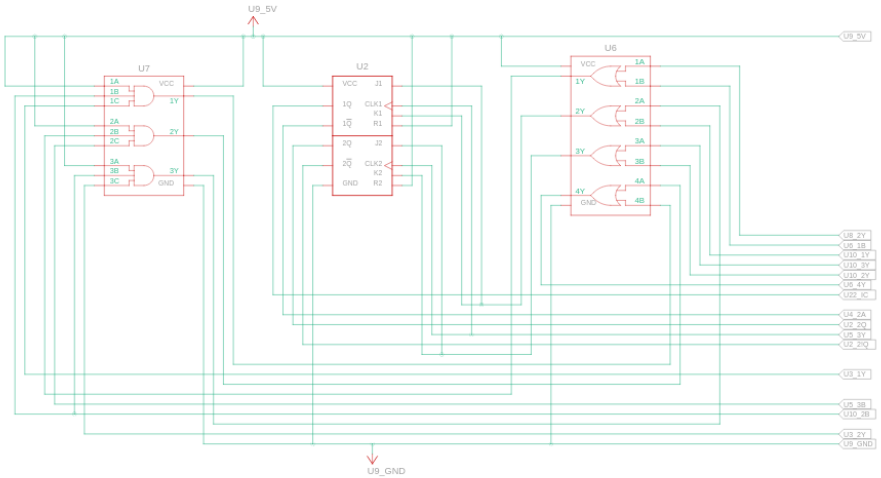


Figure 2

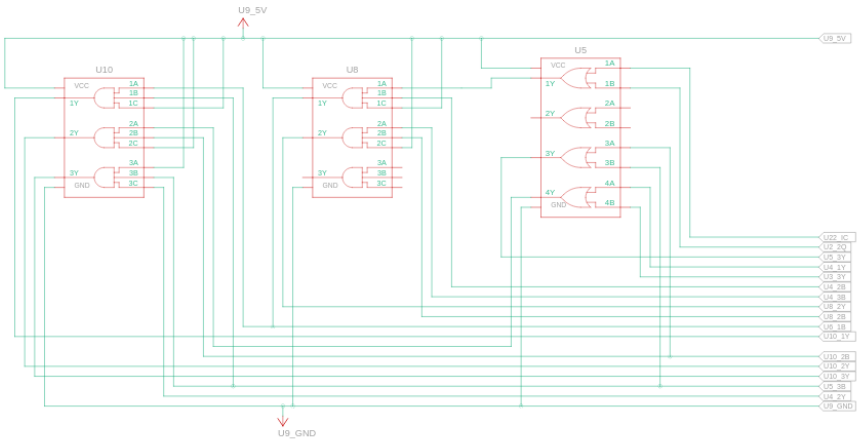


Figure 3

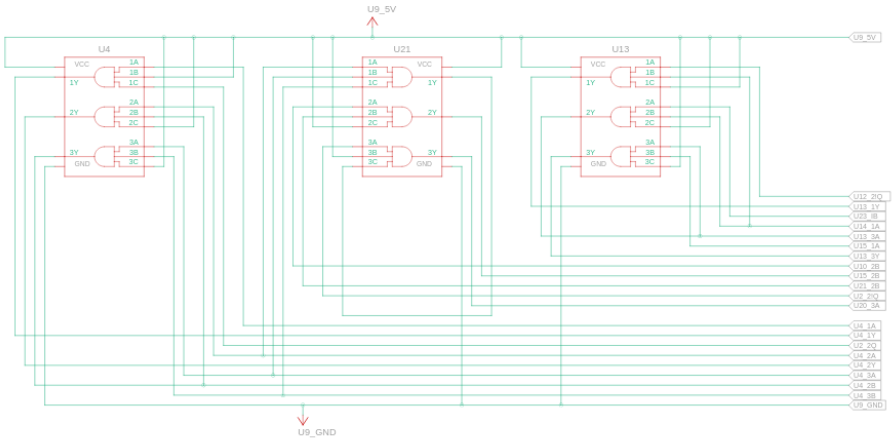


Figure 4

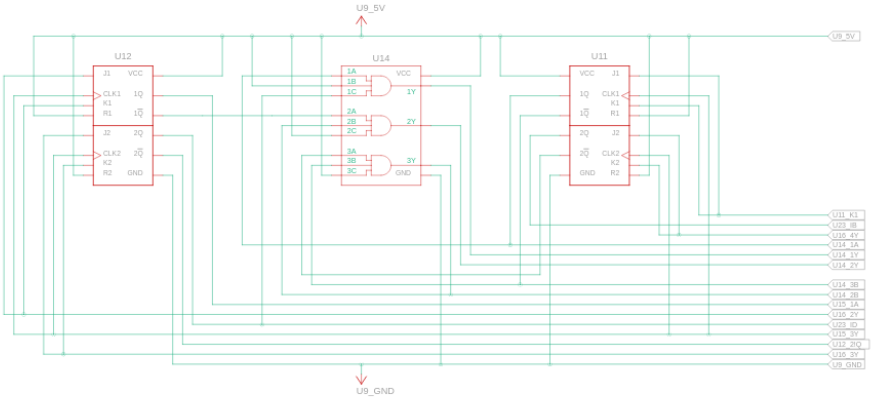


Figure 5

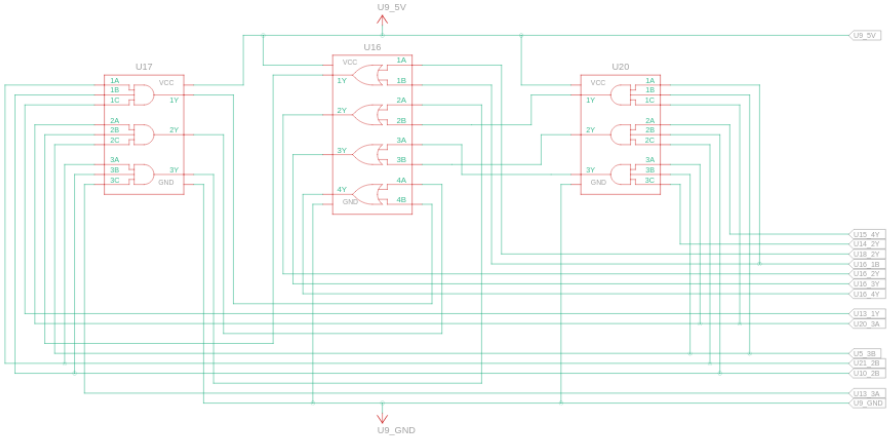


Figure 6

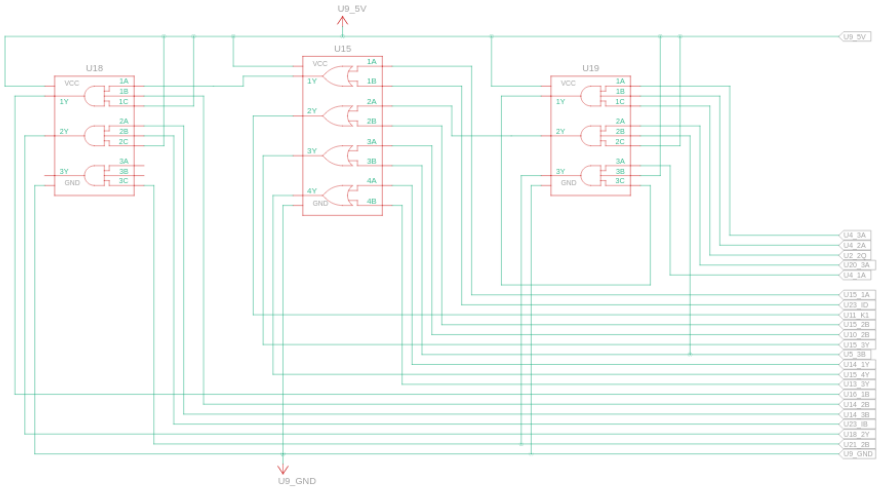


Figure 7

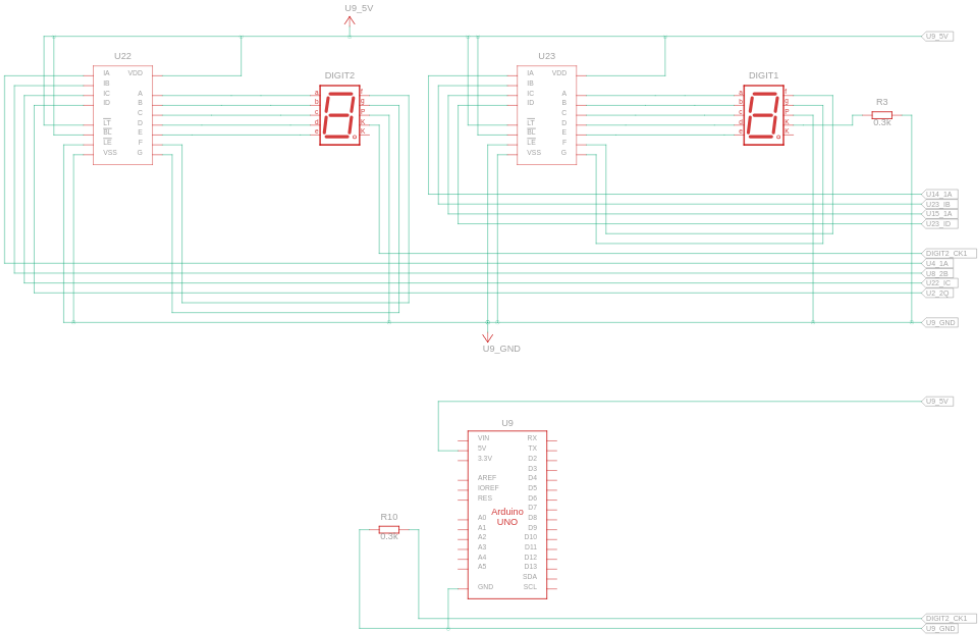
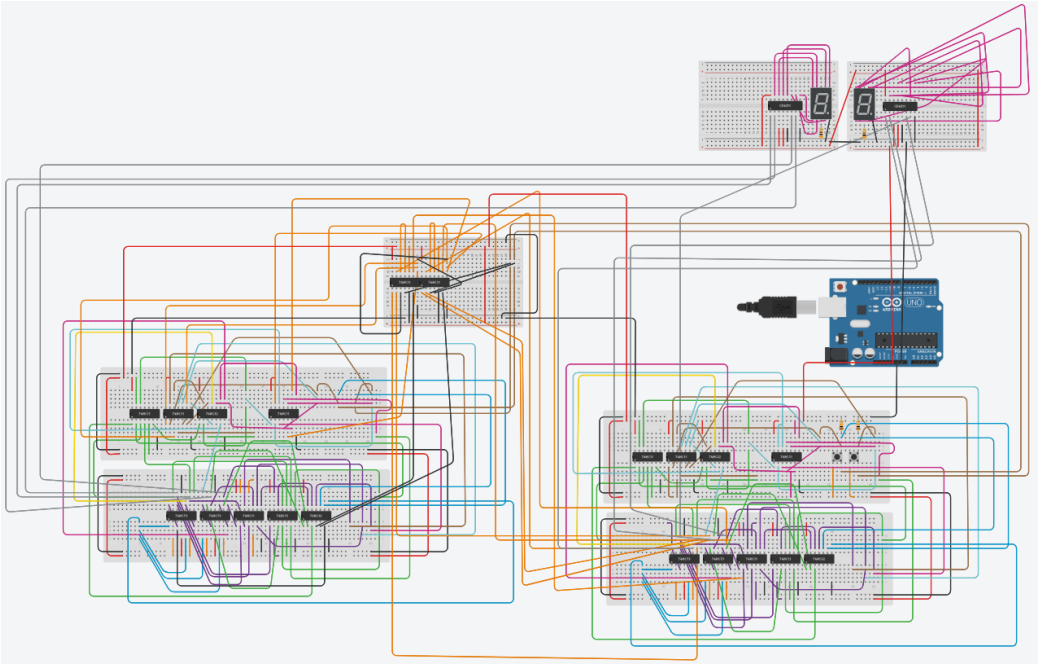


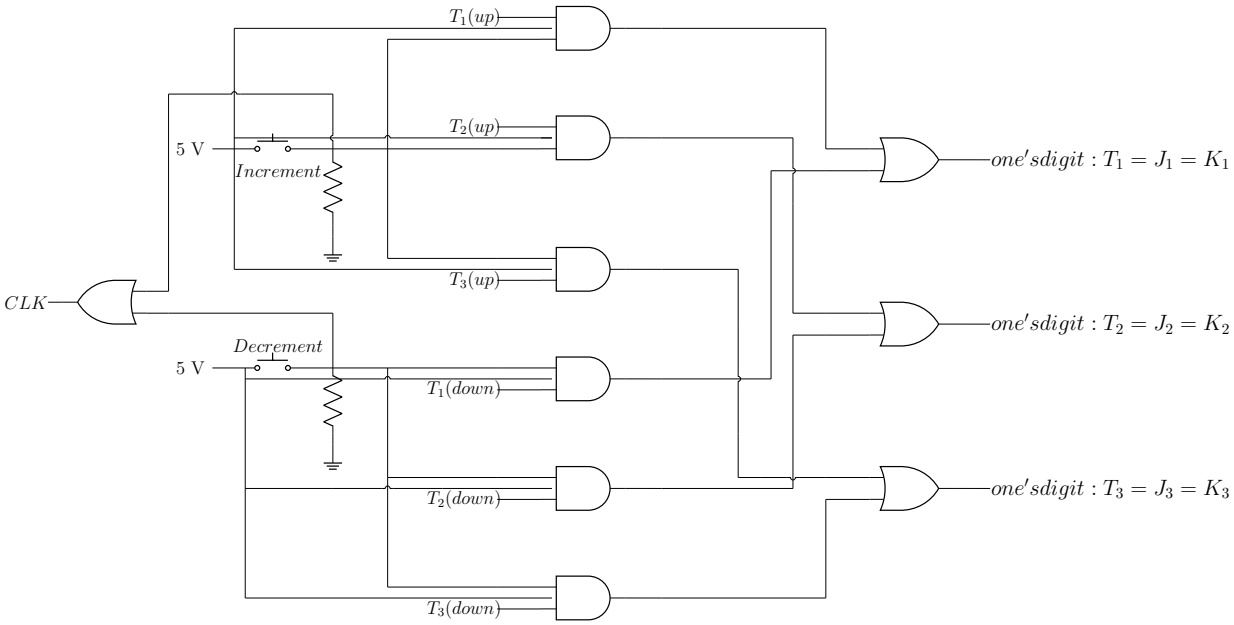
Figure 8



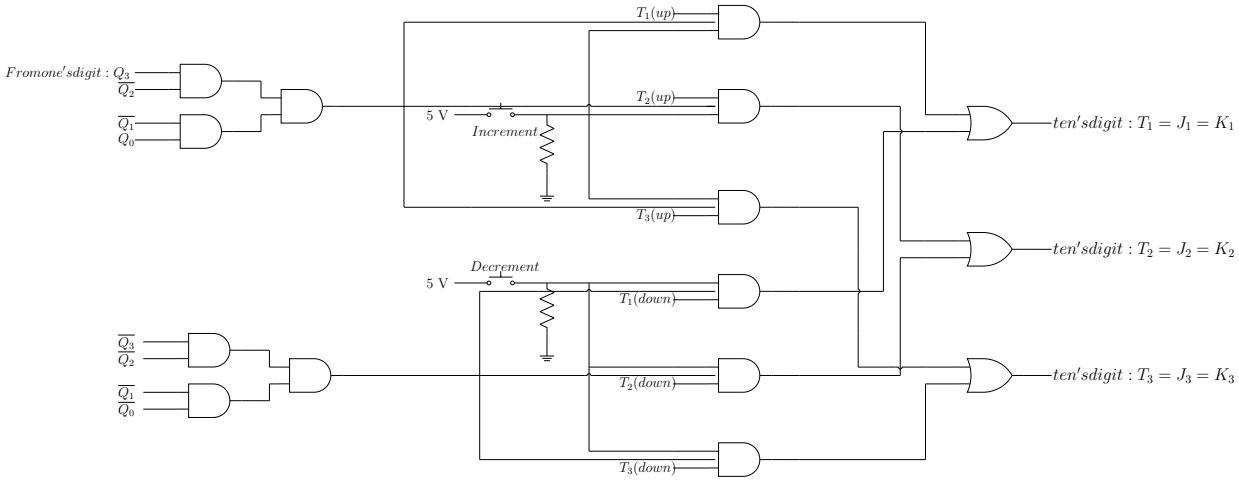
Circuit Figure In Simulation

4.4 The Logic for all the connections are given below:

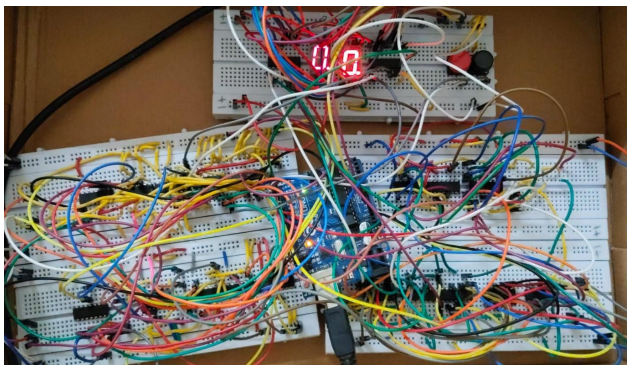
For One's Place Digit the Logic Gates are as follows:



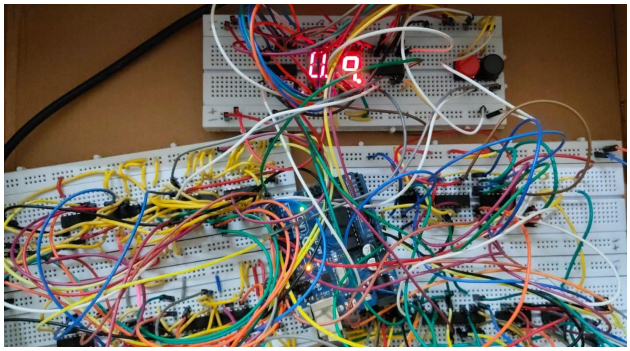
The below Logic is for connecting the Ten's Place Digit to One's Place Digit



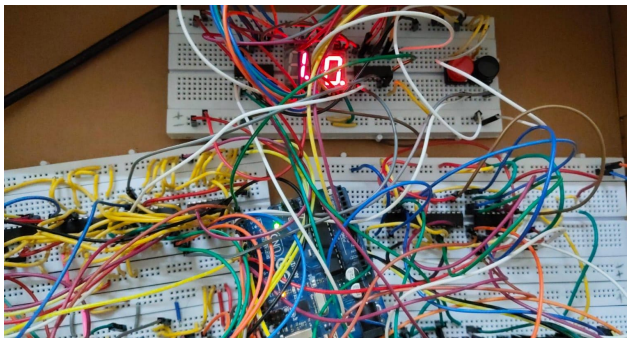
4.5 The Observations from the Circuit:



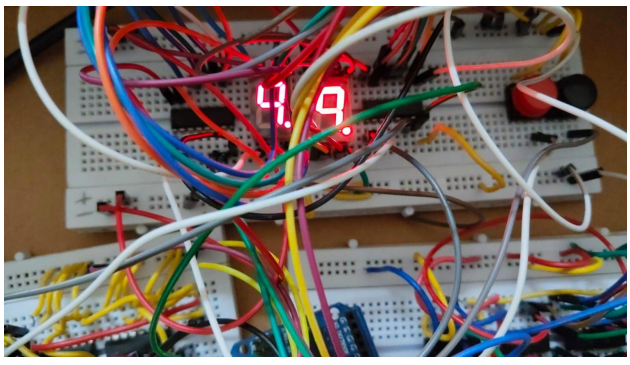
Circuit Displaying 0



Circuit Displaying 9

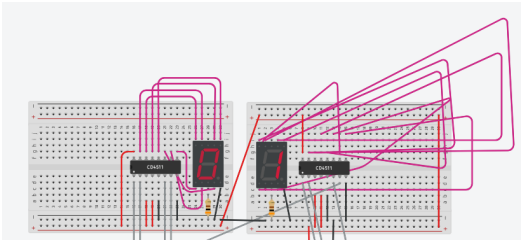


Circuit Displaying 10

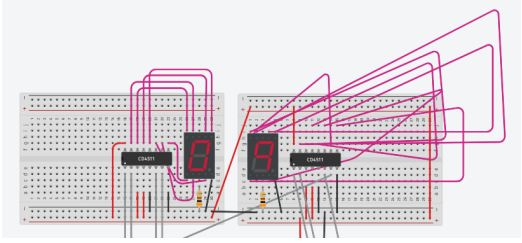


Circuit Displaying 99

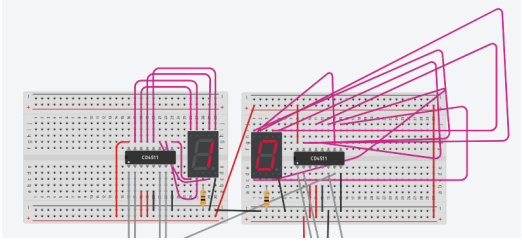
4.6 The Below are the Observations From the Simulation:



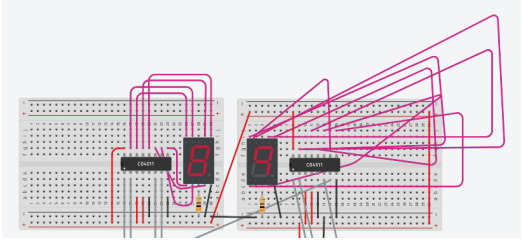
Displaying 1



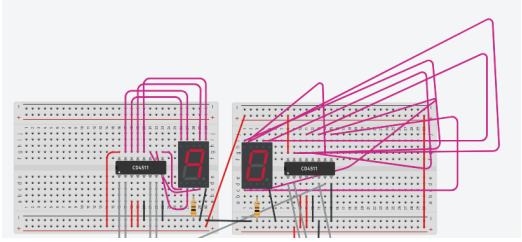
Displaying 9



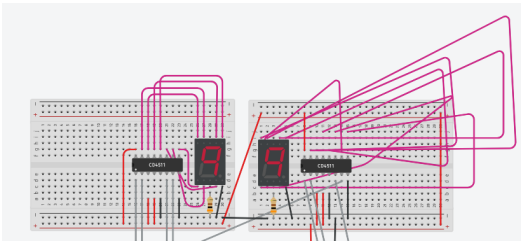
Displaying 10



Displaying 89



Displaying 90



Displaying 99

5 Conclusion

The up-down counter successfully demonstrates the fundamental principles of digital electronics and sequential logic. By counting in both increasing and decreasing order based on control input, it showcases how flip-flops and logic gates can be combined to perform controlled counting operations. This project not only enhances understanding of counter design but also provides practical insight into timing, synchronization, and direction control—key aspects in many digital systems. Overall, the implementation and testing of the up-down counter affirm its importance in applications such as digital clocks, memory addressing, and embedded systems.