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Running TraceTool in Genode for sabrelite platform

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Abstract

ACE(AXI coherency extensions) cache controller is a method to solve the cache coherence problem in shared memory with multi processor system.It takes less number of cycles then already existing methods.Previoues existing systems cache updated through write through method so every time it updates in main memory.In our method we will update the data by using MESIF protocal and if the data is unavailable in one cache it can access from another cache but in previoues existed system it goes to main memory

1 How to implement?

cache coherence problem will be implemented by using snooping method.this method listens the every operation of the processors and perform the MESIF protocal based on that operation.

2 MESIF protocal

Modified
The cache line is present only in the current cache, and is dirty; it has been modified from the value in main memory. The cache is required to write the data back to main memory at some time in the future, before permitting any other read of the (no longer valid) main memory state. The write-back changes the line to the Exclusive state

Exclusive
The cache line is present only in the current cache, but is clean; it matches main memory. It may be changed to the Shared state at any time, in response to a read request. Alternatively, it may be changed to the Modified state when writing to it.

Shared
Indicates that this cache line may be stored in other caches of the machine and is clean; it matches the main memory. The line may be discarded (changed to the Invalid state) at any time.

Invalid
Indicates that this cache line is invalid (unused).

Forward
The F state is a specialized form of the S state, and indicates that a cache should act as a designated responder for any requests for the given line. The protocol ensures that, if any cache holds a line in the S state, at most one (other) cache holds it in the F state.

3 AXI BUS

Here in our project we are using AXI bus.ACE, defined as part of the AMBA 4 specification, extends AXI with additional signalling introducing system wide coherency. This system coherency allows multiple processors to share memory and enables technology.

4 What Done Till now

i have studied the different protocals of cache coherence,I have modified the cache controller as per our requirement and i started the snoop mechanism