LAB 1-ARITHMETIC AND LOGIC UNIT: PROJECT REPORT

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EECS 361-COMPUTER ARCHITECTURE1

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Objective:

To perform basic arithmetic and logic operations like add,subtract,shift,and,or,xor,setlessthan using VHDL and simulate the results using ModelSim.

Design:

The ALU is realised structurally with the help of gates. The 32 bit ALU is designed with the help of bit-slicing. The one bit ALU is designed first and then extended to function for the required 32 bits. In the case of shift we perform only 32 bit operation as it is not possible to shift a 1 bit input.

CONCLUSION:

The ALU was designed and simulated successfully.