

# COMPUTER ARCHITECTURE

## Homework 1

 $P_1$ 

1. CLK rate of  $P_1 = 3 \text{ GHz}$  CPI = 1.2

$P_2$ : CLK rate = 2.6 GHz CPI = 1.0

$P_3$ : CLK rate = 4.2 GHz CPI = 3.

a) Execution Time = CPI  $\times$  Cycle time

for  $P_1 = 1.2 \times 1/3 = \frac{0.003}{3} \text{ seconds/instruction}$  P-0.

$P_2 = 1.0 \times 1/2.6 = \frac{1}{2.6} \text{ seconds/instruction}$

$P_3 = 3 \times 1/4.25$

a) Execution Time = CPI  $\times$  Cycle time

for  $P_1$ :  $1.2 \times 1/3 = \frac{1.2}{3} = \frac{4.2 \times 10^{-9}}{5} \text{ seconds/instruction}$

for  $P_2$ :  $1 \times 1/2.6 = \frac{1}{2.6} = \frac{5 \times 10^{-9}}{13} \text{ seconds/instruction}$

for  $P_3$ :  $3 \times 1/4.25 = \frac{3}{4.25} = \frac{12 \times 10^{-9}}{17} \text{ seconds/instruction}$

Performance =  $\frac{1}{\text{Execution Time}}$

$P_1 = \frac{1}{2.5} = \frac{5}{2} = 2.5 \times 10^9 \text{ Instructions/second}$

$P_2 = 1/5/13 = 13/5 = 2.6 \times 10^9 \text{ Instructions/second}$

$P_3 = 1/12/17 = 17/12 = 1.42 \times 10^9 \text{ Instructions/second}$

$P_3$  has highest Performance

b) Execution time = 10 seconds

Execution time = CPI × cycle time.

P<sub>1</sub>

$$T_{exec} = ?$$

$$\begin{aligned}\text{Number of Instructions} &= \text{Performance} \times \text{Execution} \\ &= 2.5 \times 10 \\ &= 25.\end{aligned}$$

Cycles per Instruction = 1.2

$$\text{Total Cycles} = 1.2 \times 25 = 30.$$

P<sub>2</sub>

$$\begin{aligned}\text{Number of Instructions} &= 2.6 \times 10 \\ &= 26.26.\end{aligned}$$

Cycles per Instructions 1.

$$\text{Total cycles} = 26 \times 1 = 26.$$

P<sub>3</sub>

$$\begin{aligned}\text{Number of Instructions} &= 1.42 \times 10 \\ &= 14.2\end{aligned}$$

CPI = 3.

$$\text{Total cycles} = 3 \times 14.2$$

$$= 42.6$$

c) Execution Time = CPI × Cycle Time

Let  $x$  be Execution time in seconds.

30% decrease in  $x = .7x$

~~Assume~~ CPI 'try be CPI. 20% increase my = 1.2y

~~P<sub>x</sub>~~

$$\frac{.7x}{1.2y} = \frac{(.7)(1.2)}{1.2y} \times \text{new cycle time}$$

~~new cycle time~~

$$.7x = 1.2y \text{ (cycle time)}$$

$$\text{Cycle time} = \frac{.7x}{1.2y}$$

$$\text{clk rate} = \frac{1.2y}{.7x}$$

$$P_1: \cancel{\text{Assume}} \text{ clk rate} = (1.2)(1.2) = \frac{1.44}{.7(0.4)} = 0.28$$

$$\text{new clk rate} = 5.14 \text{ GHz}$$

$$P_2: \text{clk rate} = (1.2)(1)(0.38)$$

$$\text{new clk rate} = 4.511 \text{ GHz}$$

$$P_3: \text{clk rate} = (1.2)(3) / (0.7)(0.05)$$

$$\text{new clk rate} = 7.29 \text{ GHz}$$

P<sub>1</sub>

2. CLK ratio = 2.25 GHz

$$CPI = \frac{1}{2} A$$

$$\frac{2}{3} B$$

$$\frac{3}{3} C$$

$$\frac{3}{3} D$$

P<sub>2</sub>

CLK ratio = 3.5 GHz

$$CPI = \frac{2}{2} A$$

$$\frac{2}{3} B$$

$$\frac{2}{3} C$$

$$\frac{3}{3} D$$

Instructions are divided as 10% A, 20% B, 50% C, 20% D.

a) Execution time = ~~CLK ratio~~ × CPI × cycle timeP<sub>1</sub>

$$CPI = A \ 20\% \ 1 \ 0.1$$

$$B \ 20\% \ 2 \ 0.4$$

$$C \ 50\% \ 3 \ 1.5$$

$$D \ 20\% \ 3 \ 0.6$$

2.6 Clocks per instruction

$$\text{Execution Time} = \frac{1}{2.6} \times 2.6 = 1.15 \times 10^{-9}$$

2.25

$$\text{Performance} = \frac{1}{E.T} = 0.86 \times 10^9 \text{ Instructions per second}$$

E.T

P<sub>2</sub>

$$\begin{array}{ll} \text{CPI}_0 = & 2 \\ \text{A 10Y.} & .2 \\ \text{B 20Y.} & .4 \\ \text{C 50Y.} & 1.0 \\ \text{D 20Y.} & .6 \\ \hline & 2.2 \end{array}$$

$$\text{Execution Time} = 2.2 \times \frac{l}{3.5} = 0.63 \times 10^{-9}$$

$$\text{Performance} = \frac{l}{\text{E.T.}} = 1.587 \times 10^9 \text{ Inst. per second}$$

P<sub>2</sub> is faster than P<sub>1</sub> in executing these set of statements.

b) Global CPI for each implementation

$$P_1 - \text{CPI} = 2.6$$

$$P_2 - \text{CPI} = 2.2$$

c) Clock cycles required for:

P<sub>1</sub>

$$\text{cycles} = \text{CPI} \times \text{Instruction}$$

$$\text{cycles} = 2.6 \times 10^6$$

Ø Ø

$$P_2 - \text{cycles} = 2.2 \times 10^6$$

3. Compiler A - Dynamic Instruction count =  $1.15 \times 10^9$ .  
 Execution time = 1.15 seconds  
 Compiler B - Dynamic Inst. count =  $1.6 \times 10^9$   
 Execution time = 1.75 s

a) Clock cycle time = 1 ns. =  $1 \times 10^{-9}$  s.

$$CPI = \frac{\text{cycles}}{\text{Inst. Count}} = \frac{\text{CPU Time} \times \text{Clock rate}}{\text{Instruction Count}}$$

$$CPU \text{ time} = \text{Cycle time} \times \text{Instruction Count}$$

Compiler A

$$CPI = \frac{1.15 \times 10^9}{1.15 \times 10^9} = 1. \text{ Clock per instruction}$$

Compiler B:

$$CPI = \frac{1.75 \times 10^9}{1.6 \times 10^9} = 1.09 \text{ Clock per Instruction}$$

b) Execution Time is same: 1 seconds

Compiler A on processor A

$$1 \text{ sec} = \frac{1 \text{ sec}}{1.15 \times 10^9} \Rightarrow \text{Clock rate}_A = \frac{1.15 \times 10^9}{1 \text{ sec}}$$

Compiler Bon Processor B.

$$1.09 = \frac{2 \times \text{CLKrate}}{1.6 \times 10^9} \Rightarrow \frac{1.75 \times 10^9}{2} = \text{CLKrate}_B$$

$$\frac{\text{CLKrate}_B}{\text{CLKrate}_A} = \frac{1.75 \times 10^9}{1.15 \times 10^9} = 1.52$$

$\therefore$  The clockrate on B runs 1.52 times faster than clockrate of A.

c) Compiler C : Dynamic Instruction Count:  $6 \times 10^8$

$$CPI = 1.1$$

$$CPI = \frac{\text{CPUtime} \times \text{CLKrate}}{\text{Inst. count}}$$

Inst. count:

$$1.1 = \frac{\text{CPUtime} \times 10^9}{6 \times 10^8} = \frac{6.6}{10}$$

CPUtime = 66 seconds

$$\text{Speedup wrt to A} = \frac{1.15}{\frac{66}{10}} = 1.74$$

$$\text{Speedup wrt to B} = \frac{1.75}{\frac{66}{10}} = 2.65$$

1. Wafer 1

diameter = 15cm

Cost = 13.5

Wafers = 74.

defects = 0.02 defects/cm<sup>2</sup>

Wafer 2

diameter = 11cm

Cost = 16

no. of dies = 110

defects = 0.031 defects/cm<sup>2</sup>

② Die Cost = Wafer cost

Die per wafer x Die Yield.

Dies per wafer =  $\frac{\text{Wafer area}}{\text{Die area}}$ 

Die Yield =

$$(1 + (\text{defects per area} \times \text{Die area}))^{-2}$$

a) Die yield (wafer) =

$$1 + (0.02) \times$$

Wafer 1.

$$\text{Die area} = \frac{\text{Wafer area}}{\text{no. of dies}} = \frac{3.14 \times (7.5)^2}{110} = \frac{176.625}{110} \text{ cm}^2 = 1.596 \text{ cm}^2$$

Die Yield =

$$\frac{1}{(1 + (0.02 \times 2.88(2)))^2}$$

0.907

$$\text{Die Yield} = \frac{1}{(1 + (0.02 \times \cancel{1.16}))^2} \quad 3 + \cancel{0.031} \cdot 1.02$$

Wafer 2:

$$\text{Die Area} = 346.5 \text{ cm}^2$$

100

$$\text{Die Yield} = \frac{1}{(1 + (0.031 \times 3.15(2)))^2}$$

0.90

b) Die Cost (Wafer 1) =  $\frac{13.5}{74 \times \cancel{1.02}} \quad 0.18$

~~0.18~~ 0.0173.

Die Cost (Wafer 2) =  $\frac{16}{100 \times \cancel{1.02}} \quad 0.161$

(2)

c) Number of Dies per wafer increased by  $10^{\circ}$ .

Number of Defects / area increased by  $15\%$

Wafer 1

$$\text{New Dies per wafer} = 1.1 \times 714 = 781.4$$

$$\text{New defects / area} = 1.15 \times 0.02 = 0.023 \text{ cm}^2$$

Wafer 2

$$\text{New Dies per wafer} = 1.1 \times 110 = 121$$

$$\text{New defects / area} = 1.15 \times 0.031 = 0.03565 \text{ cm}^2$$

Wafer 1

$$\text{Dies Yield} = \frac{1}{(1 + (0.023 \times 2.17/2))^2} = 0.95$$

$$\text{Die Area} = \frac{(7.5)^2}{12.5 \times 3.14 \times 2.17} = \frac{56.25}{78.5} =$$

Wafer 2

$$\text{Die Area} = \frac{1}{(121)} = 0.008286$$

$$\text{Dies Yield} = \frac{1}{(1 + (0.023 \times 143))^2} = 0.94$$

d) Defect area =  $200 \text{ mm}^2 = 0.2 \text{ cm}^2$

~~Wanted~~

$$Yield =$$

$$(1 + (\text{Defect area} \times \text{Die area}))^{-2}$$

$$= 95\% =$$

$$(1 + (\text{Defect area} \times 1))^{-2}$$

$$\frac{1}{95} = (1 + \text{Defect area} \times 1)^{-2}$$

$$1 + 0.1 \times \text{Defect area} = 1.026$$

$$\text{Defect area} = (1.026 - 1) / 0.1$$

$$= \frac{0.26}{0.1} = 2.6$$

$$\text{Defects area} = 2.6$$

5. C code:  $B[i] = A[i-j]$

MIPS code

SUBU \$2, \$6, \$1

ADDI \$5, (\$6+\$2), 0

~~SW \$5, 8(\$1)~~

SW \$5, 8(\$7)

6. C code:  $B[i] = A[i] - A[j]$

~~W~~

MIPS code:

W \$2, \$1 (\$6+\$1)

W \$3, (\$6+\$0)

SUBU \$5, \$3, \$2

~~SW \$5, 8(\$1)~~

SW \$5, 8(\$7)

7. Binary Instruction: 0000 0010 0001 0000 1000 0000 0010 0011

MIPS Instruction: ~~SUBU \$5, \$1, \$2, \$3, \$4, \$5, \$6, \$7~~

8. MIPS Instruction: SW \$t<sub>3</sub>, 32(\$t<sub>4</sub>)

Binary Instruction: 1010 1101 00 0011 0000 0000 0000 0000