Understanding the USB 3.1

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Abstract— **This document gives a comprehensive overview of the USB 3.1 standard and also discusses its differences over existing USB 2.0 standard.**

Keywords— **USB 3.1, USB 2.0, Cabin Management Systems, In-flight entertainment systems**

I. INTRODUCTION

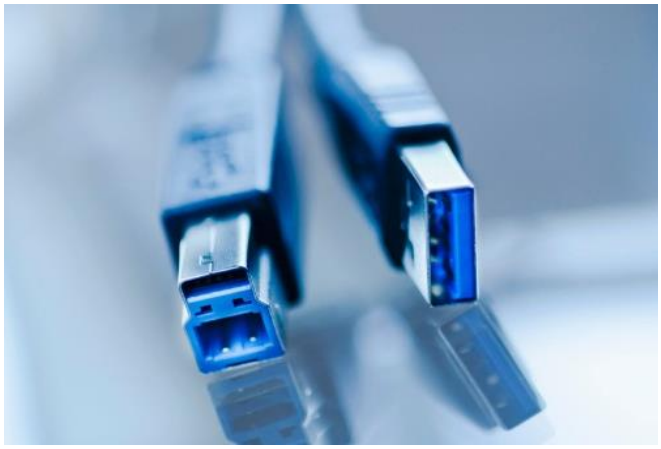

Fig. 1 Shows a standard USB type B and type A plug

The Universal serial bus USB is a PC industry standard which was earlier intended to replace the slower serial and PS/2 interface for the HID(Human interface devices) like keyboard and mouse with a fast bus with ease of use (plug and play).

Over a period of time the popularity of the USB has increased due to its low cost, robustness, high speed and ease of use enabling it to penetrate into diverse industry verticals like the industrial Automation ,Consumer electronics ,Automotive infotainment ,networking equipments and Aerospace in-flight entertainment systems.

Fig. 2 Shows Honeywell's Ovation select Aux panel showing 2 USB2.0 ports

Currently Honeywell's Ovation select Cabin management systems use USB 2.0 ports to connect USB mass storage devices for A/V files transfer and for charging devices. Upgrading to USB 3.1 ports will speed up the files transfer times by 20 times and also would charge the devices twice as fast.

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II. EVOLUTION OF USB

Fig. 3 Shows USB certified logos

The USB started with versions like 1.0 and 1.1 in 90s which allowed speeds from 1.5Mbps (Low speed) to 12Mbps (Full speed).In the year 2000 the USB 2.0 specification allowed speeds upto 480 Mbps (High speed) and also allowed backward compatibility with the low and full speed modes. However the USB 3.0 which was standardized in 2008 allowed speeds like 5 Gbps (super speed) and the latest USB 3.1 allows a maximum of 10 Gbps (super speed plus) to compete with Apple's thunderbolt.

III. **USB 3.1** DESCRIPTION

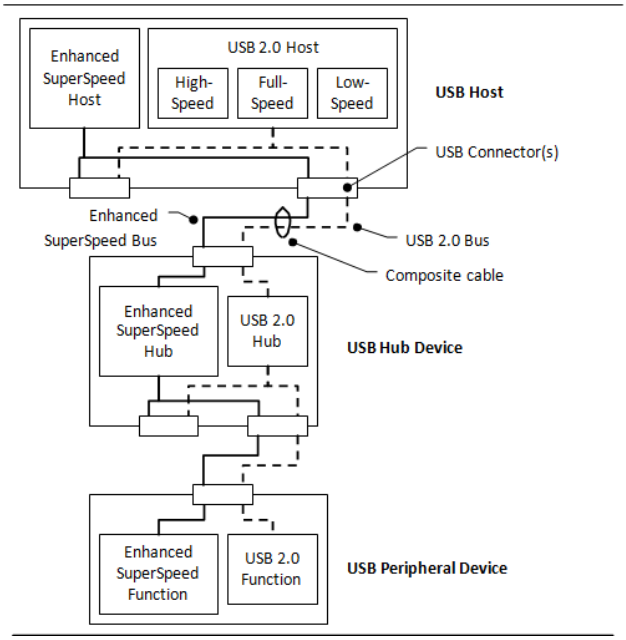

Fig. 4 Shows a block diagram of USB 3.1 dual bus

USB 3.1 is similar to the earlier versions of the USB 2.0 like the USB host sharing its bus bandwidth with the USB functions (devices) through a host scheduled protocol and allowing the USB function attachment ,configuration, usage and detachment during the operation of the USB bus.
The USB 3.1 is a dual bus system which supports both the USB 2.0 bus and the enhanced super speed bus. The USB 3.1 system is divided into 3 parts

- USB interconnect
- USB Host
- USB devices

. The USB 3.1 interconnect inherits core architectural elements from USB 2.0, although several are augmented to accommodate the dual bus architecture. The baseline structural topology is the same as USB 2.0. It consists of a tiered star topology with a single host at tier 1 and hubs at lower tiers to provide bus connectivity to devices. The USB 3.1 connection model accommodates backward and forward compatibility for connecting USB 3.1 or USB 2.0 devices into a USB 3.1 connector. The USB 3.1 connection model allows for the discovery and configuration of USB devices at the

- Highest signalling speed supported by the peripheral device,
- The highest signalling rate supported by hubs between the host and peripheral device
- The current host capability and configuration.

USB 3.1 supports USB devices (all speeds) attaching and detaching from the USB 3.1 at any time. Consequently, system software must accommodate dynamic changes in the physical bus topology. The architectural elements for the discovery of attachment and removal of devices on USB 3.1 are identical to those in USB 2.0. There are enhancements provided to manage the specifics of the Enhanced SuperSpeed bus for configuration and power management.
The independent, dual-bus architecture allows for activation of each of the buses independently and provides for the attachment of USB devices to the highest speed bus available for the device.
USB 3.1 hubs are a specific class of USB device whose purpose is to provide additional connection points to the bus beyond those provided by the host. An USB 3.1 device contains one or more logical entities called USB functions.
USB 3.1 power:
USB 3.1 power distribution is similar to USB 2.0, with increased supply budgets for devices operating on an Enhanced SuperSpeed bus with options to draw 10W(5V and 2A) and upto 100W(20 V 5 A).

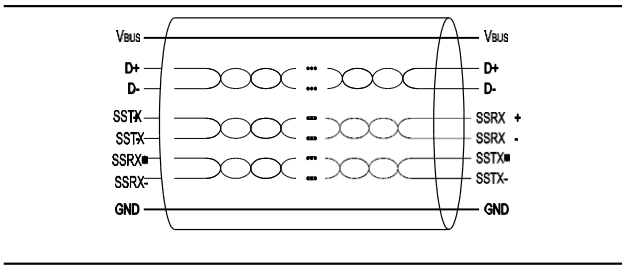

Fig. 5 Shows a USB 3.1 cable

USB 3.1 cables have eight primary conductors: three twisted signal pairs for USB data paths and a power pair. In addition to the twisted signal pair for USB 2.0 data path, two twisted signal pairs are used to provide the Enhanced SuperSpeed data path, one for the transmit path and one for the receive path.

IV. USB 3.1 Enhanced SuperSpeed Architecture

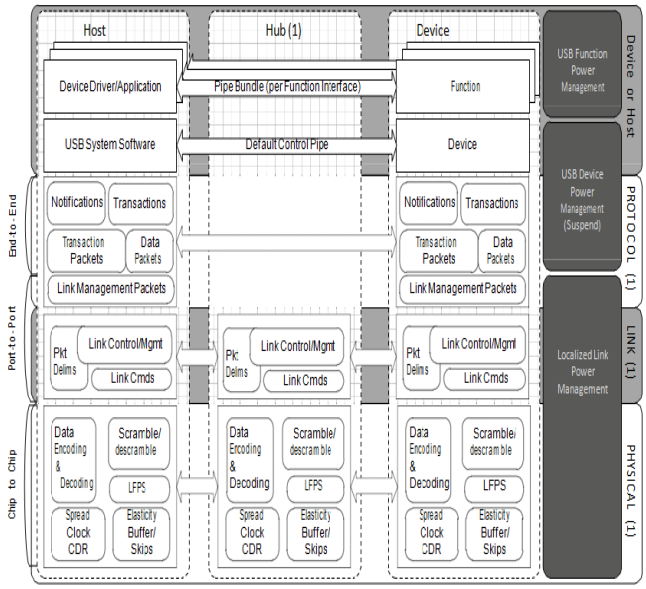

Fig. 6 a reference diagram of the Enhanced SuperSpeed interconnect represented as communications layers through a topology of host, zero to five levels of hubs, and devices.

- The rows (device or host, protocol, link, physical) realize the communications layers of the Enhanced SuperSpeed interconnect.
- The three, left-most columns (host, hub, and device) illustrate the topological relationships between devices connected to the Enhanced SuperSpeed bus.
- The right-most column illustrates the influence of power management mechanisms over the communications layers

The Enhanced SuperSpeed bus is a layered communications architecture that is comprised of the following elements:

• *Enhanced SuperSpeed Interconnect.* The Enhanced SuperSpeed interconnect is the manner in which devices are connected to and communicate with the host over the enhanced SuperSpeed bus. This includes the topology of devices connected to the bus, the communications layers, the relationships between them and how they interact to accomplish information exchanges between the host and devices.
• *Devices.* Enhanced SuperSpeed devices are sources or sinks of information exchanges. They implement the required device-end, Enhanced SuperSpeed communications layers to Accomplish information exchanges between a driver on the host and one or more logical functions on the device.

• *Host.* An Enhanced SuperSpeed host is a source or sink of information. It implements the required host-end, Enhanced SuperSpeed communications layers to accomplish information exchanges over the bus. It owns the Enhanced SuperSpeed data activity schedule and management of the Enhanced SuperSpeed bus and all devices connected to it.

V. USB 3.1 Physical Layer

The physical layer defines the PHY portion of a port and the physical connection between a downstream facing port (on a host or hub) and the upstream facing port on a device. The physical connection is comprised of two differential data pairs, one transmit path and one receive path.
The electrical aspects of each path are characterized as a transmitter, channel, and receiver; these collectively represent a unidirectional differential sub-link. At an electrical level, each differential sub-link is initialized by enabling its receiver termination.

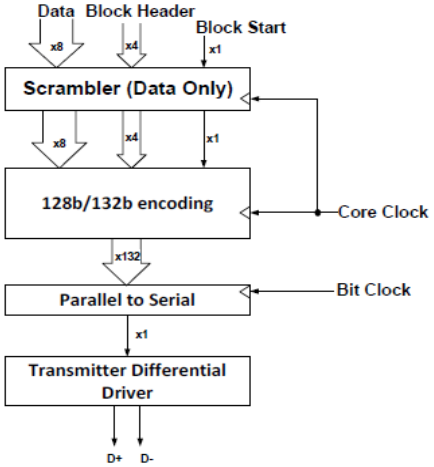

Fig. 7 Shows a USB 3.1 Physical layer Transmitter block

The transmitter is responsible for detecting the far end receiver termination as an indication of a bus connection and informing the link layer so the connect status can be factored into link operation and management.

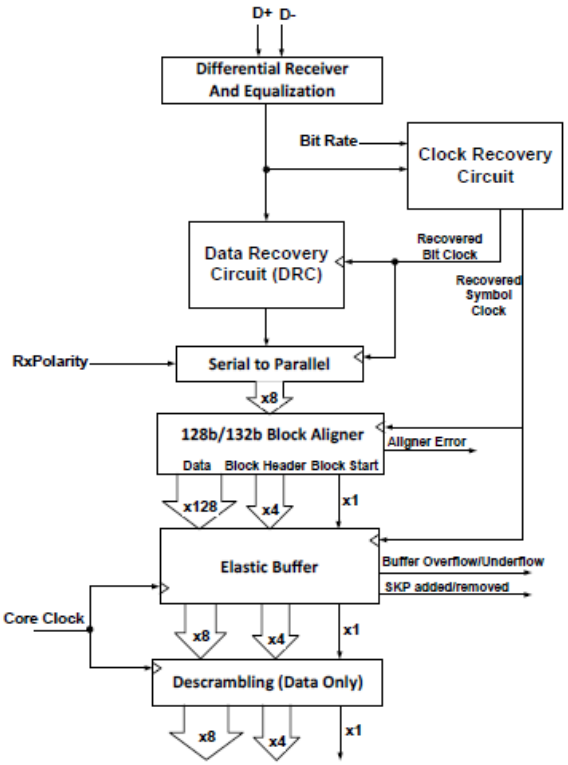

Fig. 8 Shows a USB 3.1 Physical layer receiver block

When receiver termination is present but no signaling is occurring on the differential sub-link, it is considered to be in the electrical idle state. When in this state, low frequency periodic signaling (LFPS) is used to signal initialization and power management information.

Each PHY has its own clock domain with Spread Spectrum Clocking (SSC) modulation. The USB 3.1 cable does not include a reference clock so the clock domains on each end of the physical connection are not explicitly connected. Bit-level timing synchronization relies on the local receiver aligning its bit recovery clock to the remote transmitter's clock by phase-locking to the signal transitions in the received bit stream. The receiver needs to reliably recover clock and data from the bit stream.

A USB 3.1 transmitter frames data and control bytes (referred to as Symbols) by prepending a 4-bit block identifier to 16 symbols (128 bits) to create a 128b132b block. The symbols of the block may be scrambled or not depending upon their source (whether they are data or which type of control symbol). The resultant data are sent out across the electrical interconnect using spread spectrum clocking to lower EMI emissions.

The bit stream is recovered from the electrical interconnect by the receiver and then assembled and aligned into 132 bit blocks. The data is descrambled and the identifier information and the descrambled bits are passed onto the link layer for further processing.

A USB 3.1 PHY uses a protocol over low frequency periodic signaling (LFPS) to negotiate to the highest common data rate capability of two connected PHYs

VI. USB 3.1 LINK LAYER

An Enhanced SuperSpeed link is a logical and physical connection of two ports. The connected ports are called link partners. The link layer defines the logical portion of a port and the communications between link partners.

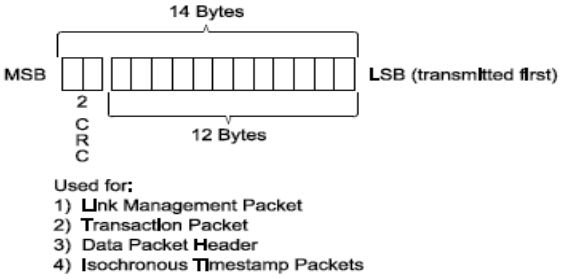

Fig. 9 Shows a USB 3.1 Link layer packet header

The logical portion of a port has:

- State machines for managing its end of the physical connection. These include physical layer initialization and event management, i.e., connect, removal, and power management.
- State machines and buffering for managing information exchanges with the link partner. It implements protocols for flow control, reliable delivery (port to port) of packet headers, and link power management.
- Buffering for data and protocol layer information elements.

VII. USB 3.1 PROTOCOL LAYER

This protocol layer defines the "end-to-end" communications rules between a host and device.

The Enhanced SuperSpeed protocol provides for application data information exchanges between a host and a device endpoint. This communications relationship is called a pipe. It is a host-directed protocol, which means the host determines when application data is transferred between the host and device. The Enhanced SuperSpeed protocol is not a polled protocol, as a device is able to asynchronously request service from the host on behalf of a particular endpoint.

All protocol layer communications are accomplished via the exchange of packets. Packets are sequences of data bytes with specific control sequences which serve as delimiters managed by the link layer. Host transmitted protocol packets are routed through intervening hubs directly to a peripheral device. They

do not traverse bus paths that are not part of the direct path between the host and the target peripheral device. A peripheral device expects it has been targeted by any protocol layer packet it receives. Device transmitted protocol packets simply flow upstream through hubs to the host. Application data is transmitted within data packet payloads. Data may be transmitted in bursts of back-to-back sequences of data packets. The protocol provides flow control support for some transfer types.

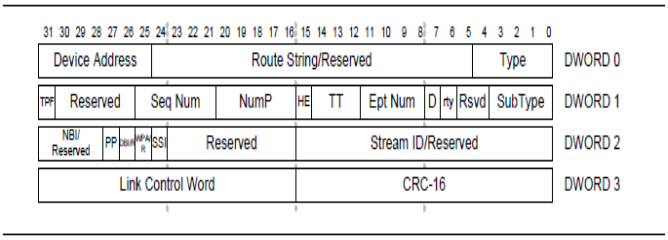

Fig. 10 Shows a USB 3.1 protocol layer Transaction packet

ACK Transaction Packets (TPs) and Data Packets (DPs) are annotated with the transfer type of
the endpoint and upstream flowing asynchronous DPs on SuperSpeed Plus bus segments are annotated with an arbitration weight (AW) used by SuperSpeed Plus hub arbiters for fair service.

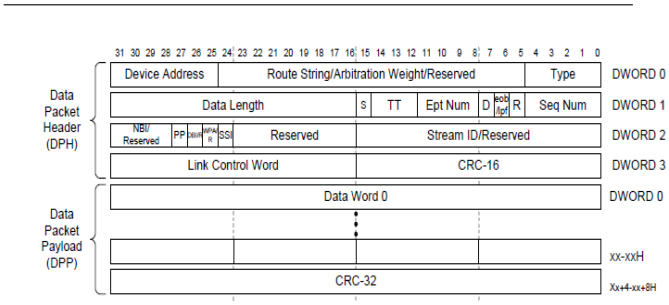

Fig. 11 Shows a USB 3.1protocol layer data packet

• Relaxed Enhanced SuperSpeed host concurrent endpoint scheduling rules for SuperSpeed Plus endpoints. This decouples asynchronous and periodic transaction scheduling and allows concurrent IN endpoint scheduling for SuperSpeed Plus endpoints and for SuperSpeed endpoints on different SuperSpeed bus-instances
• Packets to or from simultaneously active endpoints moving over a SuperSpeed Plus bus can be intermingled with each other and reordered (with respect to different endpoints flows) by each SuperSpeed Plus hub they transit.

VIII. USB 3.1 DEVICE

All devices are assigned a USB address when enumerated by the host. Each device supports one or more pipes through which the host may communicate with the device. All devices must support a designated pipe at endpoint zero to which the device's Default Control Pipe is attached. All devices support a common access mechanism for accessing information through this control pipe. There are 2 types of devices namely peripheral devices and Hubs

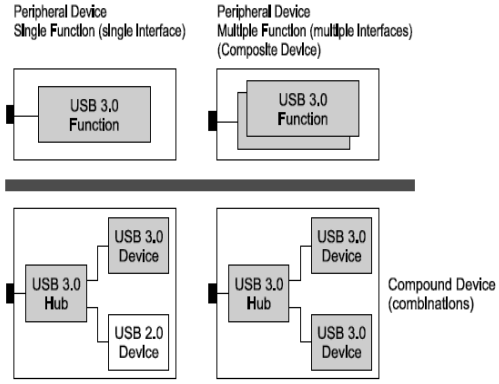

FIG. 12 SHOWS A USB 3.1 DEVICE TYPES

IX. USB 3.1 HOSTS

A USB 3.1 host interacts with USB devices through a host controller. To support the dual-bus architecture of USB 3.1, a host controller must include both Enhanced SuperSpeed and USB 2.0 elements, which can simultaneously manage control, status and information exchanges between the host and devices over each bus.
The host includes an implementation-specific number of root downstream ports for Enhanced SuperSpeed and USB 2.0. Through these ports the host:
• Detects the attachment and removal of USB devices
• Manages control flow between the host and USB devices
• Manages data flow between the host and USB devices
• Collects status and activity statistics
• Provides power to attached USB devices
• A SuperSpeed Plus host is required to implement USB PTM (Precision Time Management)..
USB System Software inherits its architectural requirements from USB 2.0, including:
• Device enumeration and configuration
• Scheduling of periodic and asynchronous data transfers
• Device and function power management
  • Device and bus management information

X. USB 3.1 DATA FLOW MODEL

The Enhanced SuperSpeed bus inherits the data flow models from USB 2.0, including:

• Data and control exchanges between the host and devices are via sets of either unidirectional or bi-directional pipes.

• Data transfers occur between host software and a particular endpoint on a device.

The endpoint is associated with a particular function on the device. These associations between host software to endpoints related to a particular function are called pipes. A device may have more than one active pipe.

There are two types of pipes:

- Stream
- message.

Stream data has no USB defined structure, while message does. Pipes have associations of data bandwidth, transfer Service type and endpoint characteristics, like direction and buffer size.

• Most pipes come into existence when the device is configured by system software. However, one message pipe, the Default Control Pipe, always exists once a device has been powered and is in the default state, to provide access to the device's configuration, status, and control information.

A pipe supports one of four transfer types as defined in USB 2.0 (bulk, control, interrupt, and isochronous). The basic architectural elements of these transfer types are unchanged from USB 2.0.

• The bulk transfer type has an extension for Enhanced SuperSpeed protocol called Streams. Streams provide in-band, protocol-level support for multiplexing multiple independent logical data streams through a standard bulk pipe.

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A. Conclusions

The USB 3.1 is a signification improvement over the existing USB 2.0 standard in terms of speed of data transfer giving almost 20 times more speed in transferring data and offering twice the power for charging the bigger devices like iPad and tablets which are increasing popular.

In the context of aircraft cabin USB 3.1 will offer faster transfer of passengers' data like big A/V files from their personal devices to be played on the aircraft personal or bulk head monitors. The USB 3.1 will reduce the waiting time for loading of the personal files onto the IFE and hence improves the in-flight experience in the aircraft cabin.

REFERENCES

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[2] USB 3.0 from Wikipedia http://en.wikipedia.org/wiki/USB_3.0