Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree Examination June 2022 (2019 scheme)

Course Code: ITT204

Course Name: COMPUTER ORGANIZATION

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1		Illustrate the basic operational concepts in transferring data between main memory and processor with neat diagram.	3
2		Specify the actions needed to execute the instruction Load R1,10(R2)	3
3		How many cycles are required to execute 10 instructions on a 7 stage pipeline assuming no stalls occur during the execution of 10 instructions and each stage takes 1 cycle for execution?	3
4		Discuss about locality of reference in cache memory.	3
5		Write notes on arithmetic pipeline.	3
6		Explain the characteristics of Reduced Instruction Set Architectures.	3
7		Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, SET and WORD fields are respectively:	3
8		Explain memory interleaving.	3
9		List and describe the registers in a DMA interface.	3
10		What are interrupts? List the sequence of steps following an interrupt request.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Discuss the sequence of control signals for the following instructions. i) Store R1,10(R2) ii) Sub R1, R2	8
	b)	What are the factors to be considered while using stack for subroutine call? Discuss with appropriate example.	6
12	a)	List the advantages of using addressing modes? Justify with example the need for addressing modes in a RISC processor.	7

b) Give the sequence of control steps required to execute branch instruction in a single-bus organization. 7

Module -2

13 a) Illustrate the difference in the performance of an Arithmetic Right Shifter & a Logical Right Shifter. 7

b) Explain in detail the design of the processor unit. 7

14 a) Draw and explain the block diagram for a 4-bit complete accumulator 7

b) Mention the advantages of using a scratch pad memory. Explain with diagram how processor uses scratch pad memory. 7

Module -3

15 a) Consider a pipelined processor with the following four stages- 7

IF : Instruction Fetch

ID : Instruction Decode and Operand Fetch

EX : Execute

WB : Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction need 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD R2, R1, R0 { R2 ← R0 + R1}

MUL R4, R3, R2 {R4 ← R3 + R2}

SUB R6, R5, R4 { R6 ← R5 + R4 }

b) Illustrate with an example instruction pipelining. List its advantages. 7

16 a) List and explain the different pipeline hazards and their possible solutions with appropriate examples. 10

b) Discus about delayed branch. 4

Module -4

17 a) Elaborate the various cache mapping techniques with an example. 10

b) Explain the working of a DRAM memory cell. 4

18	a)	What are various performance optimization methods used in cache memory? Explain.	8
	b)	Explain DRAM scheduling policies	6

Module -5

19	a)	Compare the working of PCI and SCSI.	7
	b)	Explain in detail hardware interrupts.	7
20	a)	Explain the working of Universal Serial Bus (USB).	7
	b)	Differentiate serial port and parallel port. Draw the diagram of a bidirectional 8-bit parallel interface and explain its working.	7

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