# Digital System Design Module 4 - SEQUENTIAL LOGIC CIRCUITS

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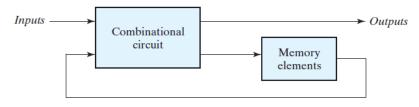
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### SEQUENTIAL CIRCUITS

- A combinational circuit its output depends only and immediately on its inputs — they have no memory
- Sequential circuits, however, act as storage elements and have memory
- They can store, retain, and then retrieve information when needed at a later time
- The binary information stored in these elements at any given time defines the state of the sequential circuit at that time

## SEQUENTIAL CIRCUITS



Block diagram of sequential circuit

A sequential circuit is specified by a time sequence of inputs, outputs, and internal states

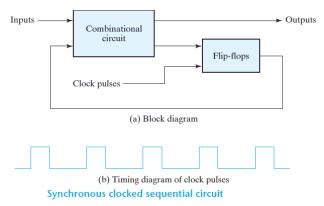


# SEQUENTIAL CIRCUITS

- There are two main types of sequential circuits, and their classification is a function of the timing of their signals.
  - A synchronous sequential circuit: it is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time.
  - Synchronization is achieved by a timing device called a clock generator, which provides a clock signal having the form of a periodic train of clock pulses.
  - An asynchronous Sequential Circuit: The behavior depends upon the input signals at any instant of time and the order in which the inputs change.
  - The storage elements commonly used in asynchronous sequential circuits are time-delay devices



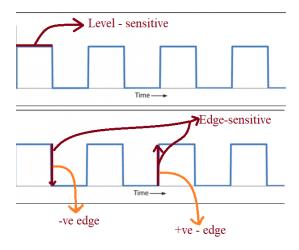
# Synchronous Circuit



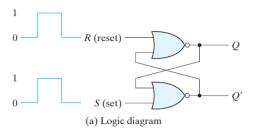
A flip-flop is a binary storage device capable of storing one bit of information

## STORAGE ELEMENTS: LATCHES

- Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches; those controlled by a clock transition are flip-flops.
- Latches are said to be level sensitive devices; flip-flops are edge-sensitive devices.
- The two types of storage elements are related because latches are the basic circuits from which all flip-flops are constructed



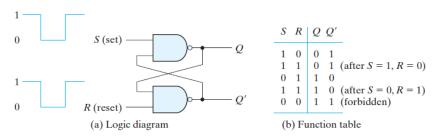
# SR Latch



|                    | S | R | Q | Q' |                                     |  |  |  |
|--------------------|---|---|---|----|-------------------------------------|--|--|--|
|                    | 1 | 0 | 1 | 0  |                                     |  |  |  |
|                    | 0 | 0 | 1 | 0  | (after $S = 1, R = 0$ )             |  |  |  |
|                    | 0 | 1 | 0 | 1  |                                     |  |  |  |
|                    | 0 | 0 | 0 | 1  | (after $S = 0, R = 1$ ) (forbidden) |  |  |  |
|                    | 1 | 1 | 0 | 0  | (forbidden)                         |  |  |  |
| (b) Function table |   |   |   |    |                                     |  |  |  |

SR latch with NOR gates

### SR Latch

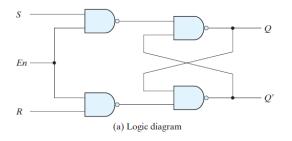


**SR** latch with NAND gates

Because the NAND latch requires a 0 signal to change its state, it is sometimes referred to as an S'R' latch.



## SR Latch



| En                    | S                | R                     | Next state of Q   |
|-----------------------|------------------|-----------------------|---|
| 0<br>1<br>1<br>1<br>1 | X<br>0<br>0<br>1 | X<br>0<br>1<br>0<br>1 | No change<br>No change<br>Q = 0; reset state<br>Q = 1; set state<br>Indeterminate |

(b) Function table

SR latch with control input