Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: IT201

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Convert the hexadecimal number 153.125 to decimal, binary and octal. (4)

b) Perform addition, subtraction, multiplication, and division of the following binary numbers without converting them to decimal : 1000110 and 110 (6)

c) Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. (5)

i) 11010 – 100111

ii) 1100011 – 1010

2 a) (i) Find the decimal equivalent of $(A40F)_{16}$ (6)

(ii) Find the 16's complement of $(A40F)_{16}$

(iii) Convert to binary $(A40F)_{16}$

(iv) Finds the 2's complement of the result in (iii)

b) For the Boolean function (9)

$$F = w'xy' + xy'z + x'y'z + w'xy + wx'y + wxy$$

(i) Draw the logic diagram, using the original Boolean expression.

(ii) Simplify the Boolean algebra to a minimum number of literals.

(iii) Obtain the truth table of the function from the simplified expression and show that it is the same as the original Boolean expression.

3 a) Simplify the following functions using Quine- McClusky method : (7)

$$f(a,b,c,d) = \sum m(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11).$$

b) Using K-map simplify following Boolean expression & give implementation of same using gates $F(A,B,C,D) = \sum(2,4,8,15) + \sum D(0,3,9,12)$ (8)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Derive characteristics equations for SR, JK, D and T flip flops. (8)

b) Design a combinational circuit to implement a 4-bit carry look-ahead adder. (7)

5 a) Explain the difference between a latch and a flip-flop using D-latch and D-flip-flop. (5)

b) Design a 4-bit code-converter to convert BCD to gray code. (10)

6 a) What is encoder? Design octal to binary encoder. (5)

b) For the following state table (10)

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
a	b	c	0	0
b	d	f	1	0
c	b	e	0	0
d	f	h	1	0
e	b	e	0	0
f	g	a	1	1
g	a	h	0	0
h	g	e	1	1

i. Draw the corresponding state diagram.
ii. Tabulate the reduced state table.
iii. Draw the state diagram corresponding to the reduced state table.
iv. Design the sequential circuit using flip-flops. [Hint: Unused states may be considered as don't cares.]

PART C

Answer any two full questions, each carries20 marks.

7 a) Implement a four-bit universal shift register. Explain its design. (10)

b) What do you mean by ripple counter? Design and implement a BCD ripple counter. (10)

8 a) What are the operations that can be performed on a RAM? What are the steps involved? Explain. (10)

b) Write the Algorithm for addition of binary numbers. (10)

9 a) Design a three bit counter that counts only odd numbers (1-3-5-7-1), using JK Flip-flops. (10)

b) Tabulate the PLA programming table for the four Boolean functions listed below. Minimize the numbers of product terms. (10)

$A(x, y, z) = \sum_m(1, 3, 5, 6)$
$B(x, y, z) = \sum_m(0, 1, 6, 7)$
$C(x, y, z) = \sum_m(3, 5)$
$D(x, y, z) = \sum_m(1, 2, 4, 5, 7)$

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