Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third semester B.Tech examinations (S) September 2020

Course Code: IT201

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Convert the hexadecimal number $(112.75)_{10}$ to decimal, binary and octal. (4)

b) Perform subtraction using 10's complement and 2's complement for 3456 - 245. (6)

c) Represent 3851.2 and 349.8 in BCD and perform addition using BCD arithmetic. (5)

2 a) Represent 320.625 in single precision floating point representation (5)

b) Simplify the following Boolean function into (i) sum-of-products form and (ii) product-of-sums form: (8)

$F(A, B, C, D) = \sum_m(0, 1, 2, 5, 8, 9, 10)$

c) Determine the base of the number in the operation 155+12=200 (2)

3 a) Simplify the following functions using Quine- McClusky method : (7)

$F(w,x,y,z) = \sum_m(3,4,5,6,7,11,12,14,15)$

b) Using K-map simplify following Boolean expressions & give implementation of same using gates (8)

F(A,B,C,D)=AB(C+D)+$\bar{A}$ (B+C+BCD)

d(A,B,C,D)=$\bar{A}\bar{B}\bar{C}$+AB$\bar{C}$D+A$\bar{B}\bar{C}$

PART B

Answer any two full questions, each carries 15 marks.

4 a) Implement 8x1 MUX using 4x1 MUX. (8)

b) Design & implement Full Adder with truth table. (5)

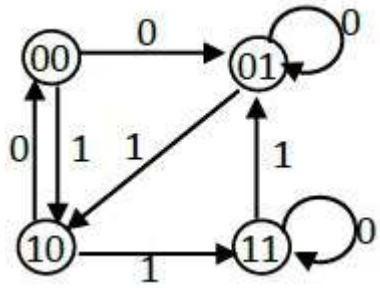
c) Explain the functioning a D-Flip Flop with its circuit. (2)

5 a) Derive the circuit for two bit magnitude comparator (5)

b) Design a sequential circuit with two D Flip-Flops, A and B, and one input x. When x = 0, then the state of the circuit remains the same. When x =1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats. (10)

6 a) What is encoder? Design octal to binary encoder. (5)

b) For the following state table (10)



i. Draw the corresponding state diagram.

ii. Tabulate the reduced state table.

iii. Draw the state diagram corresponding to the reduced state table.

iv. Design the sequential circuit using flip-flops. [Hint: Unused states may be considered as don't cares.]

PART C

Answer any two full questions, each carries 20 marks.

7 a) Explain Booth's Algorithm. Perform -5 * -7 using this algorithm. (10)

b) Design 3 bit up/down Asynchronous counter. (10)

8 a) Explain various types of ROMs. (5)

b) Explain the purpose of Hamming Code, Given the 11-bit data word 00100101010, generate the corresponding 15-bit Hamming code word. (5)

c) Design and implement a 4 bit binary synchronous up counter. (10)

9 a) Explain about different types of shift registers. (10)

b) Tabulate the PLA programming table for the four Boolean functions listed below. (10)

$F_1(A,B,C)=\sum m(0,2,4,7)$. $F_2(A,B,C))=\sum m(3,5,6,7)$.

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