Digital System Design

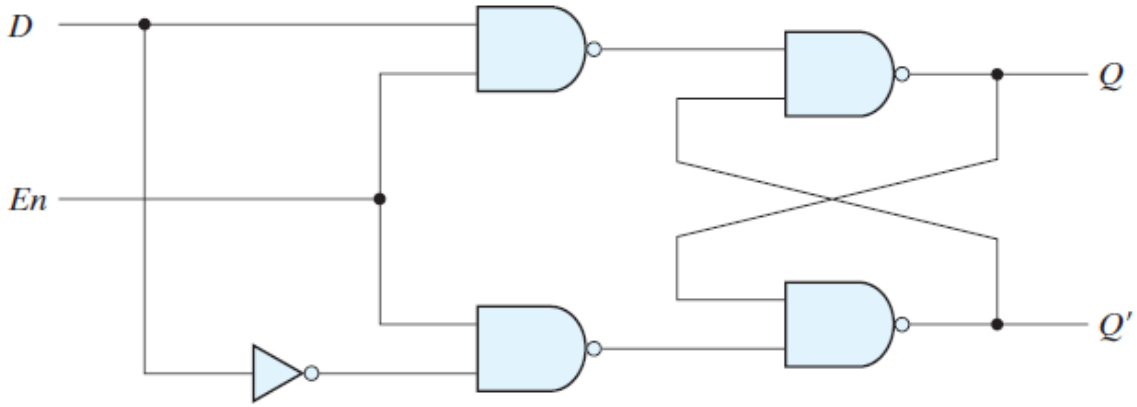
Module 4 - SEQUENTIAL LOGIC CIRCUITS

Dr. Deepthi Sasidharan

Assistant Professor, Department of Information Technology
GEC Barton Hill, Thiruvananthapuram

November 2, 2020

D Latch (Transparent Latch)

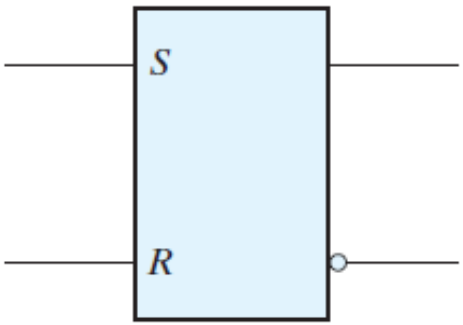


(a) Logic diagram

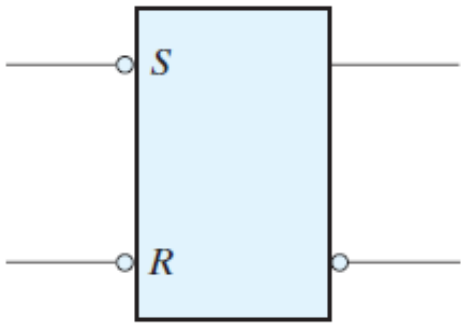
En	*D*	Next state of *Q*
0	X	No change
1	0	$Q = 0$; reset state
1	1	$Q = 1$; set state

(b) Function table

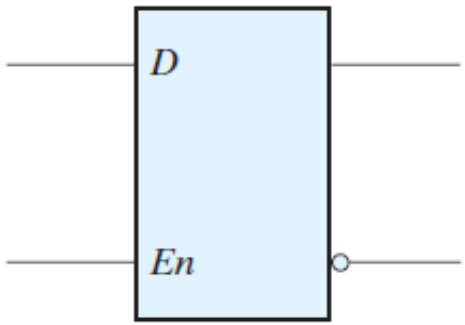
Graphic symbols for latches



SR

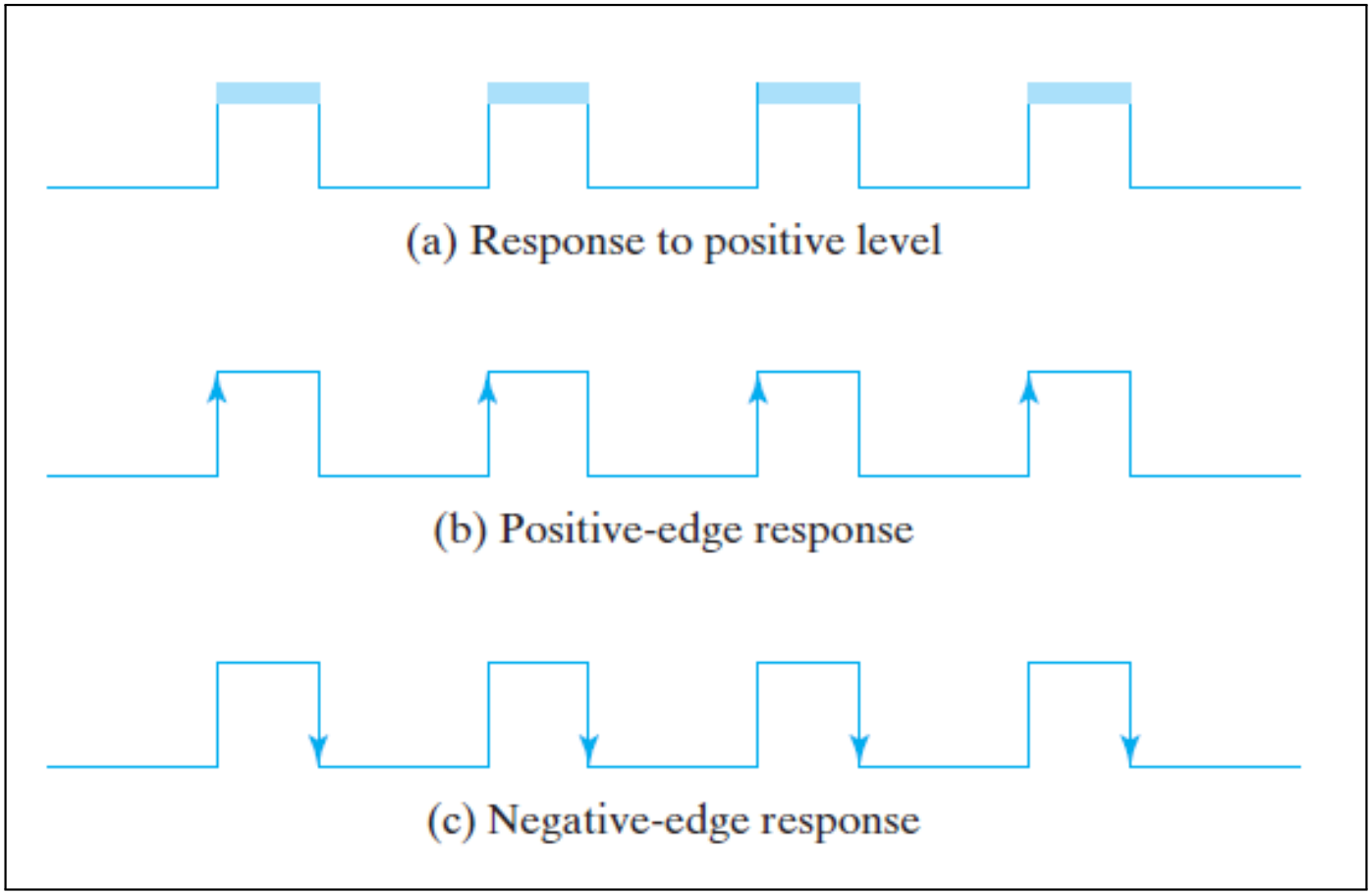


$\overline{S}\overline{R}$



D

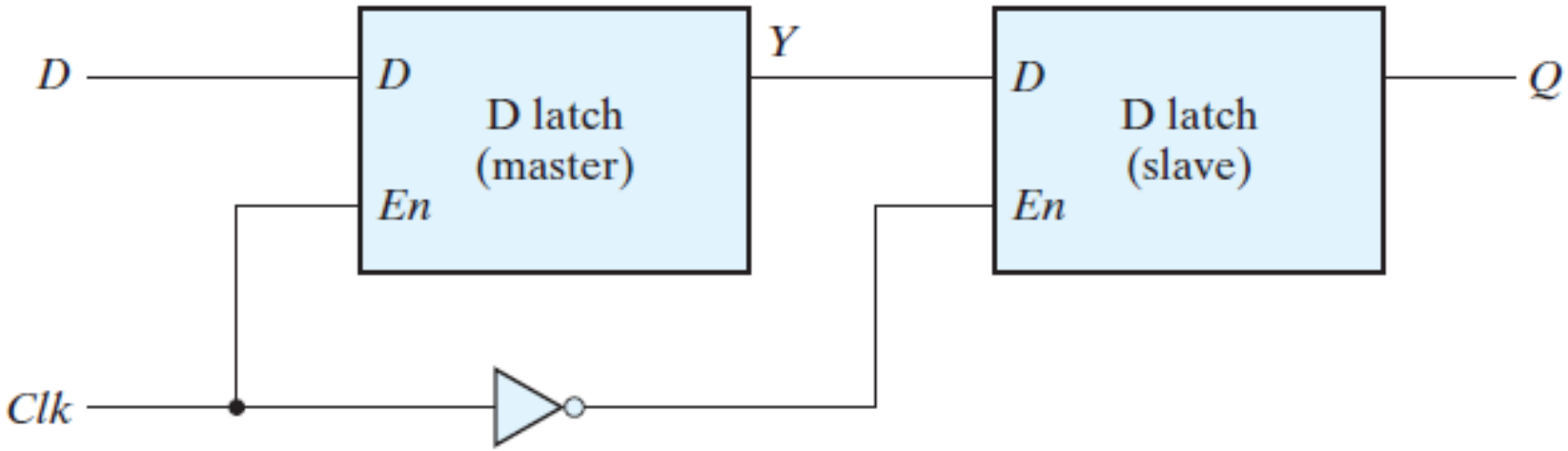
Clock response in latch and flip-flop



Flip-Flops

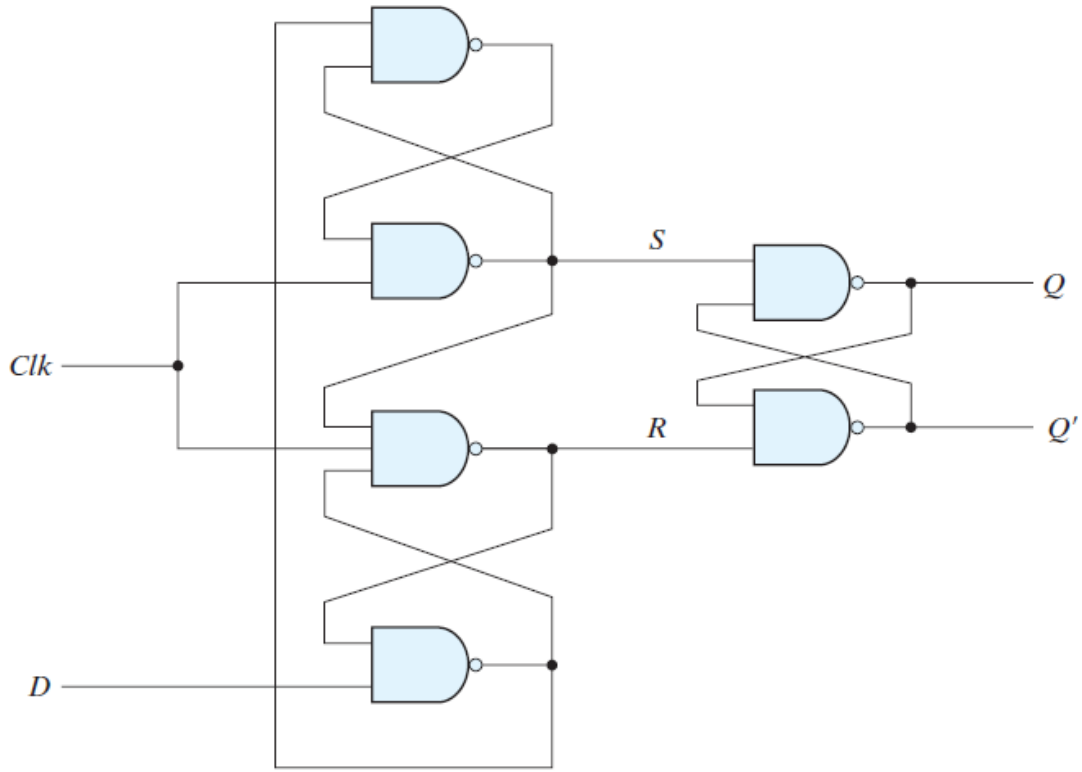
- There are two ways that a latch can be modified to form a flip-flop.
  1. Employ two latches in a special configuration that isolates the output of the flip-flop and prevents it from being affected while the input to the flip-flop is changing.
  2. Trigger only during a signal transition (from 0 to 1 or from 1 to 0) of the synchronizing signal (clock) and is disabled during the rest of the clock pulse

Master–slave D flip-flop

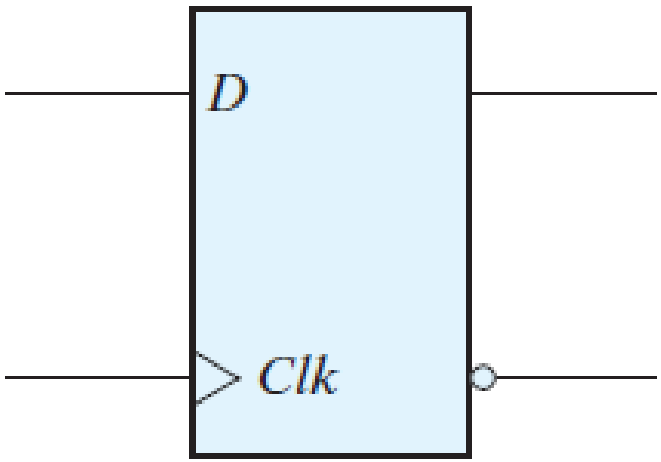


- Edge-Triggered D Flip-Flop

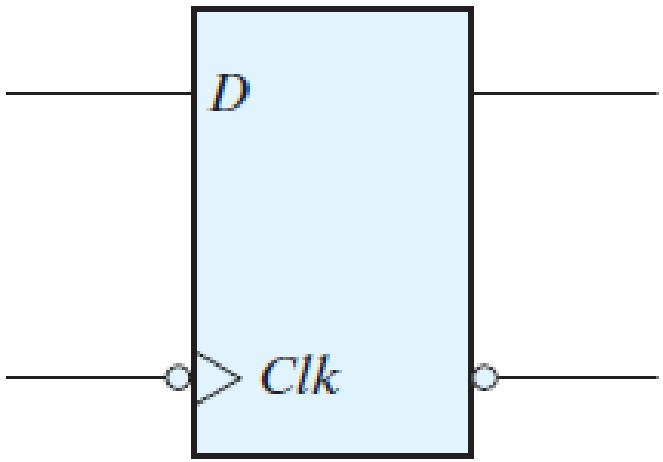
D -type positive-edge-triggered flip-flop



Graphic symbol for edge-triggered D flip-flop



(a) Positive-edge



(a) Negative-edge