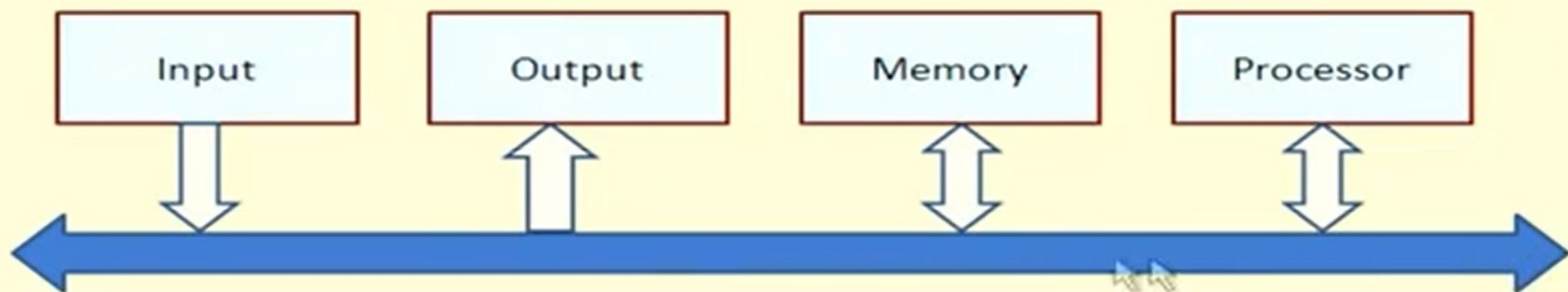


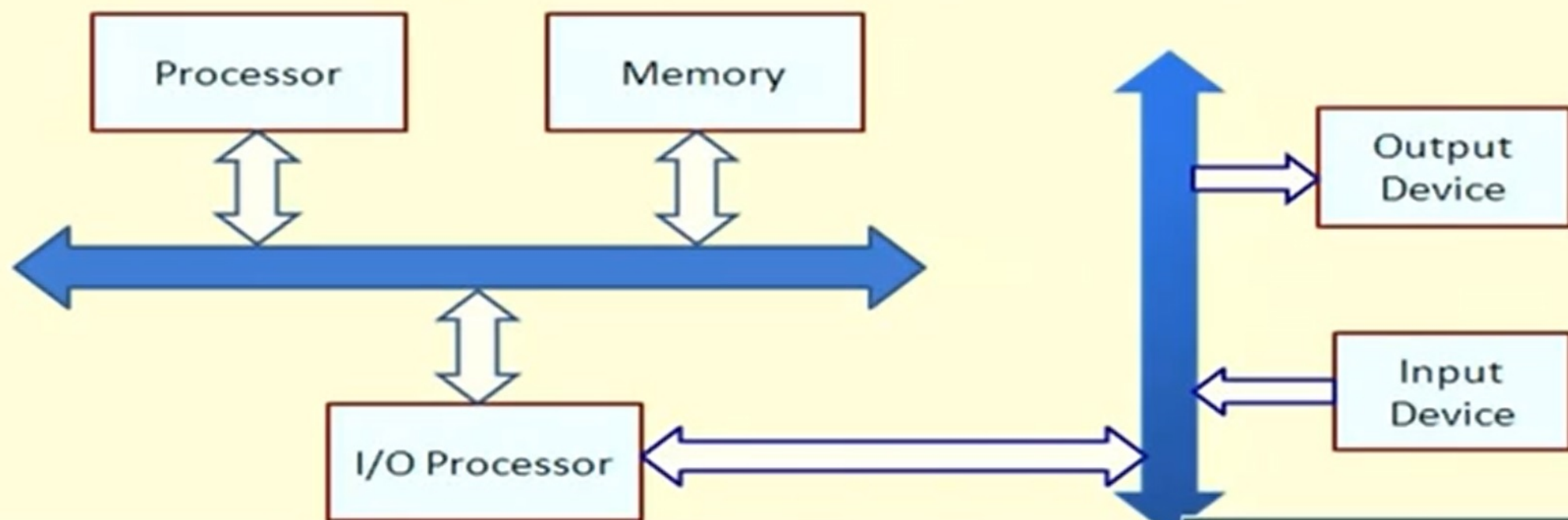
Bus Architecture

- The different functional modules must be connected in an organized manner to form an operational system.
- Bus refers to a group of lines that serves as a connecting path for several devices.
- The simplest way to connect the functional unit is to use the single bus architecture.
 - Only one data transfer allowed in one clock cycle.
 - For multi-bus architecture, parallelism in data transfer is allowed.

System-Level Single Bus Architecture

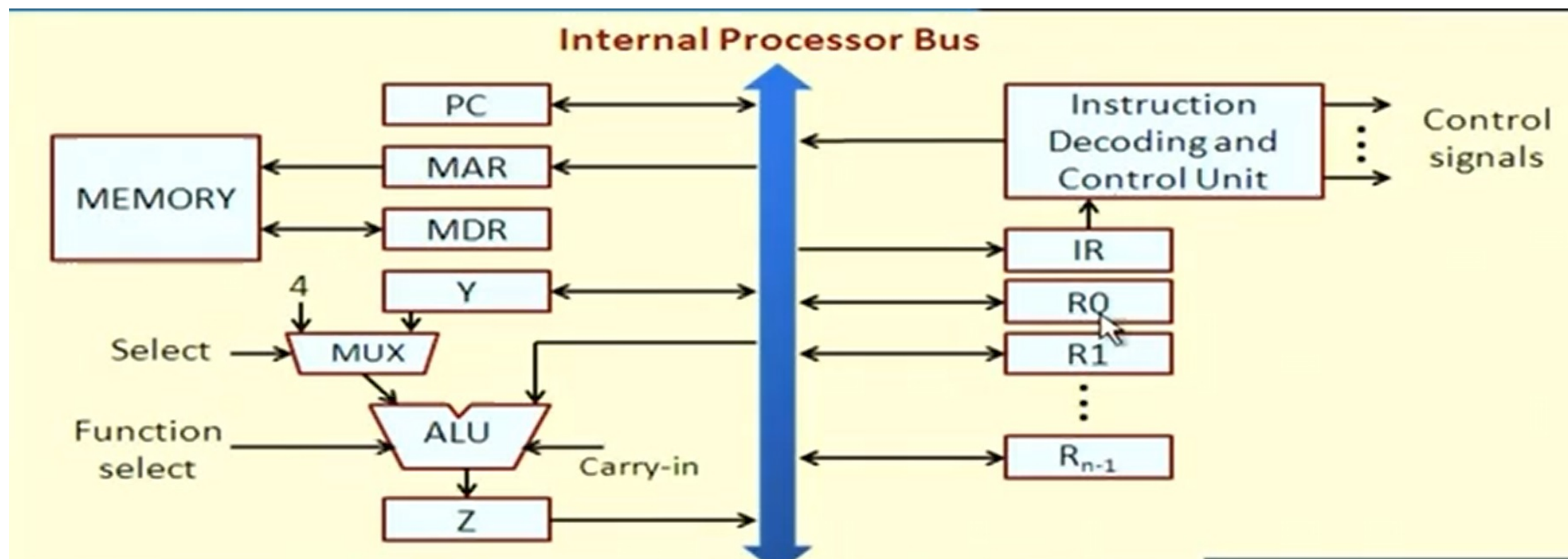


System-Level Two-Bus Architecture



Single-Bus Architecture Inside the Processor

- There is a single bus inside the processor.
 - ALU and the registers are all connected via the single bus.
 - This bus is internal to the processor and should not be confused with the external bus that connects the processor to the memory and I/O devices.
- A typical single-bus processor architecture is shown on the next slide.
 - Two temporary registers *Y* and *Z* are also included.
 - Register *Y* temporarily holds one of the operands of the ALU.
 - Register *Z* temporarily holds the result of the ALU operation.
 - The multiplexer selects a constant operand 4 during execution of the micro-operation: $PC \leftarrow PC + 4$.



Multi-Bus Architectures

- Modern processors have multiple buses that connect the registers and other functional units.
 - Allows multiple data transfer micro-operations to be executed in the same clock cycle.
 - Results in overall faster instruction execution.
- Also advantageous to have multiple shorter buses rather than a single long bus.
 - Smaller parasitic capacitance, and hence smaller delay.