

INSTITUTE OF PRINTING TECHNOLOGY & GOVERNMENT POLYTECHNIC COLLEGE SHORANUR, KERALA



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Seminar report on
FERROELECTRIC RAM [FRAM]

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CERTIFICATE

This is to certify that seminar report entitled **FERROELECTRIC RAM [FRAM]** submitted by **SOUMYA .M ,Reg.No: 18130708** to the Department of Computer Engineering, **Institute of Printing Technology Government Polytechnic College Shoranur, Kerala**, in partial fulfilment of the requirement for the award of Diploma under the Directorate of Technical Education, Government of Kerala is a bonafide record of the work carried out by her.

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ABSTRACT

Ferroelectric memory is a new type of semiconductor memory, which exhibit short programming time, low power consumption and nonvolatile memory, making highly suitable for application like contact less smart card, digital cameras which demands many memory write operations.

A ferroelectric memory technology consists of a complementary metal- oxide-semiconductor (CMOS) technology with added layers on top for ferroelectric capacitors. A ferroelectric memory cell has at least one ferroelectric capacitor to store the binary data, and one transistor that provide access to the capacitor or amplify its content for a read operation. Once a cell is accessed for a read operation, its data are presented in the form of an analog signal to a sense amplifier, where they are compared against a reference voltage to determine their logic level.

Ferroelectric memories have borrowed many circuit techniques (such as folded-bitline architecture) from DRAM's due to similarities of their cells and DRAM's maturity. Some architectures are reviewed here.

INTRODUCTION

Before the 1950's, ferromagnetic cores were the only type of random-access, nonvolatile memories available. A core memory is a regular array of tiny magnetic cores that can be magnetized in one of two opposite directions, making it possible to store binary data in the form of a magnetic field. The success of the core memory was due to a simple architecture that resulted in a relatively dense array of cells. This approach was emulated in the semiconductor memories of today (DRAM's, EEPROM's, and FRAM's). Ferromagnetic cores, however, were too bulky and expensive compared to the smaller, low-power semiconductor memories. In place of ferromagnetic cores ferroelectric memories are a good substitute. The term "ferroelectric" indicates the similarity, despite the lack of iron in the materials themselves.

Ferroelectric memory exhibit short programming time, low power consumption and nonvolatile memory, making highly suitable for application like contact less smart card, digital cameras which demanding many memory write operations. In other word FRAM has the feature of both RAM and ROM. A ferroelectric memory technology consists of a complementary metal-oxide- semiconductor (CMOS) technology with added layers on top for ferroelectric capacitors. A ferroelectric memory cell has at least one ferroelectric capacitor to store the binary data, and one or two transistors that provide access to the capacitor or amplify its content for a read operation.

A ferroelectric capacitor is different from a regular capacitor in that it substitutes the dielectric with a ferroelectric material when an electric field is applied

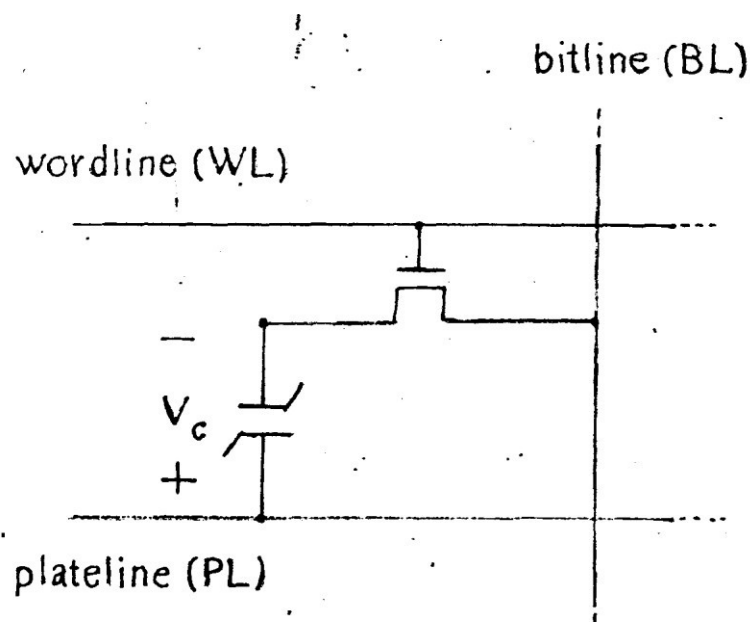
and the charges displace from their original position spontaneous polarization occurs and displacement becomes evident in the crystal structure of the material importantly, the displacement does not disappear in the absence of the electric field .Moreover, the direction of polarization can be reversed or reoriented by applying an appropriate electric field.

A hysteresis loop for a ferroelectric capacitor displays the total charge on the capacitor as a function of the applied voltage. It behaves similarly to that of a magnetic core, but for the sharp transitions around its coercive points, which implies that even a moderate voltage can disturb the state of the capacitor. One remedy for this would be to modify a ferroelectric memory cell including a transistor in series with the ferroelectric capacitor. Called an access transistor, it t wo control the access to the capacitor and eliminate the need for a square like hysteresis loop compensating for the softness of the hysteresis loop characteristics and blocking unwanted disturb signals from neighboring memory cells.

Once a cell is accessed for a read operation, its data are presented in the form of an anal signal to a sense amplifier, where they are compared against a reference voltage to determine the logic level.

BASIC MEMORY CELL STRUCTURE

A ferroelectric memory cell, known as 1T-1C (one transistor, one capacitor) structure which is similar to that of DRAM. The difference is that ferroelectric film is used as its storage capacitor rather than paraelectric material as in DRAM.

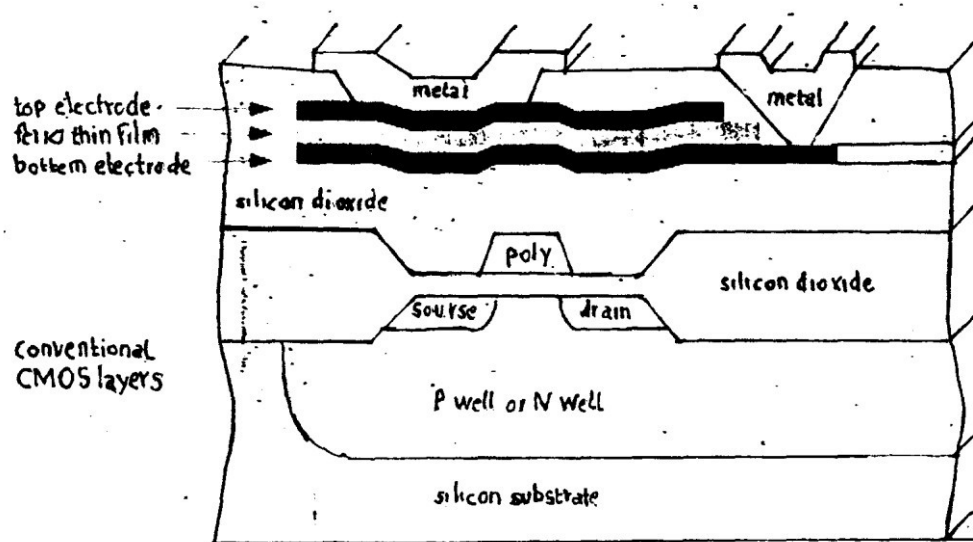


-Ferroelectric 1T-1C structure-

Figure above shows memory cell structure, consists of a single ferroelectric capacitor that is connected to a Plateline(PL) at one end and, via an access transistor, to a Bitline(BL) at the other end. Raising the wordline (WL) and hence turning ON the access transistor accesses the cell.

As shown in fig 2 ferroelectric memory technology consists of a CMOS technology with added layers on top for ferroelectric capacitors. Therefore, by

masking parts of the design that are not using ferroelectric capacitors, CMOS digital and analog circuits can be integrated together with ferroelectric memories, all in the same chip. Ferroelectric capacitors sit directly on the top of the transistors by means of stacked vias, hence reducing cell area.

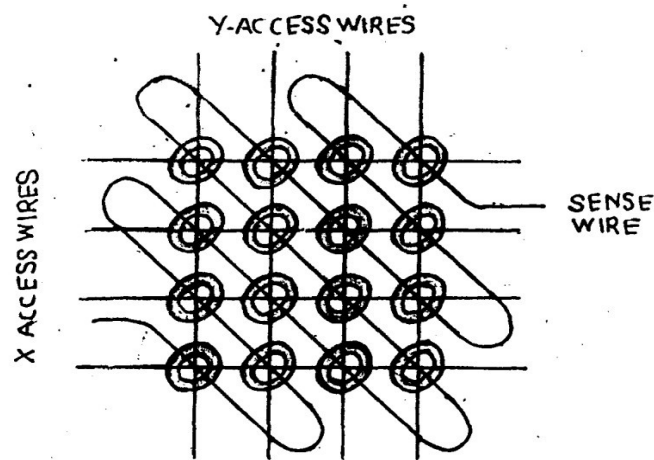


- Ferroelectric Capacitor layers on top of conventional CMOS process-

BASIC MEMORY CELL OPERATION

The principles of operation of ferroelectric capacitor and ferromagnetic core are similar. We first discuss the principle of operation of ferromagnetic memories, which make it easier to understand the operation of ferro electric cell.

FERROMAGNETIC CORE



-Two dimensional array of Ferroelectric-

A core memory consist of a regular array of tiny . Magnetic core that can be magnetized in one of two opposite directions, hence storing binary data in the form of a magnetic field. A write access into a core consist of sending simultaneous current pluses through the core via its x-access and y-access wires. Depending on the directions of the current pluses, a core is magnetized in “0” or a “1” direction. The best assumption here is thst only the core that receives two simultaneous current pluses is affected. All the

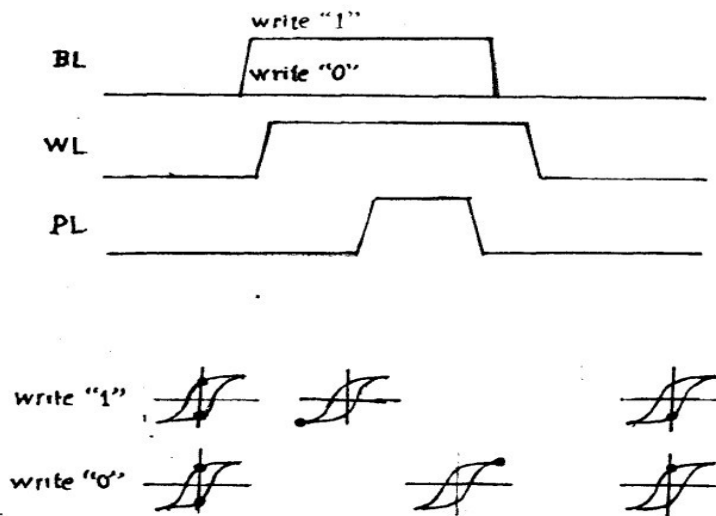
remaining cores, including those that receives one current plus or none retain their original magnetization.

A read access Consists of a write access followed by sensing. We write a “0” to the core in order to discover the original data content of the core. If the original content of the core is a “1”, writing a “0” would mean changing the magnetic direction of the core. This induces a large current spike on the sense wire. On the other hand, there will be no current spike on the sensing wire if the original content of the core was also a “0.” Therefore, by sensing the presence of a current spike on the sensing wire, the original data of the accessed core are determined.

The read operation as explained above is destructive since a “0” is written to any core that is accessed for a read. The original data, however, are saved at the sense amplifier and can be restored back into the accessed core. In other words, a read access is only complete after the second write that restores the original data.

FRAM WRITE OPERATION

The cell consists of a single ferroelectric capacitor that is connected to a PL at one end and via an access transistor, to a BL at the other end. The cell is accessed by raising the wordline (WL) and hence turning ON the access transistor. The access is one of two types: a write access or a read access.



- Timing diagram for a write operation of the Memory Cell -

The timing diagram for a write operation is shown in Figure. To write a "1" into the memory cell, the BL is raised to V_{DD} . Then the WL is raised to $V_{DD} + V_r$ (known as boosted V_{DD}) where V_T is the threshold voltage of the access transistor. This allows a full V_{DD} to appear across the ferroelectric capacitor ($-V_{DD}$) according to the voltage convention adopted in Figure). At this time, the state of the ferroelectric capacitor is independent of the initial state of the FE capacitor, as shown in Figure. At this time the state of ferroelectric is independent of its initial state.

Next, the PL is pulsed, that is, pulled UP to V_{DD} and subsequently pulled back down to ground. Note that the WL stays activated until the PL is.

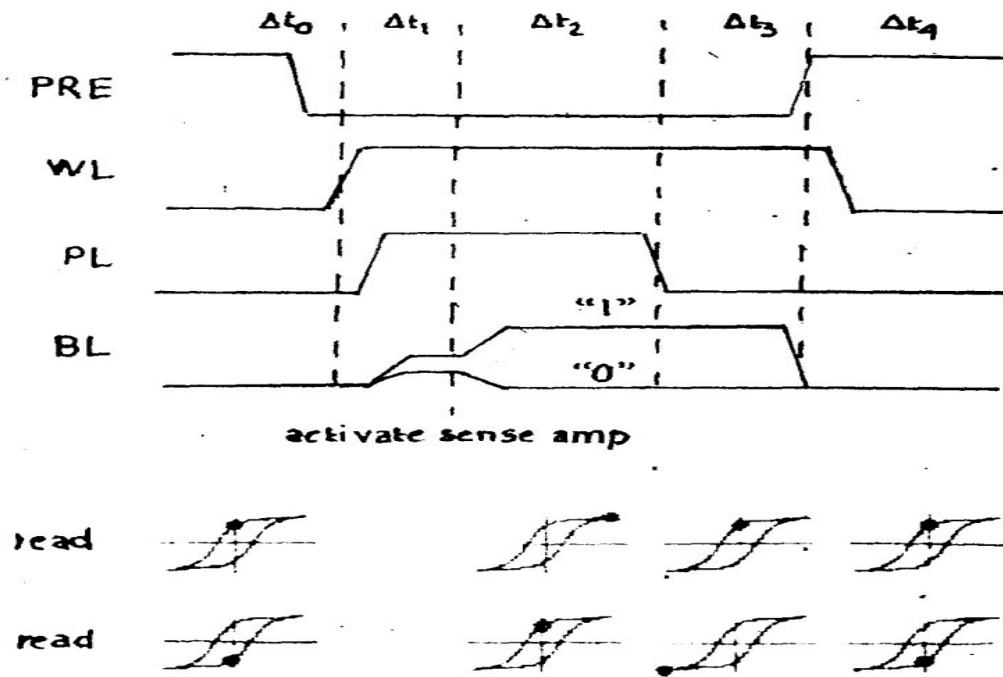
pulled down completely and the BL is driven back to zero. The final state of the capacitor is a negative charge state S_1 . Finally, deactivating the WL leaves this state undisturbed until the next access.

To write a “0” into the cell, the BL is driven to 0V prior to activating the WL. The rest of the operation is similar to that of writing a “1” as shown in Figure

The written data is held in the cell even though the selection of the wordline is changed to non selected state (i.e. transistor is OFF), so it is nonvolatile. The level of polarization that correspond to the data remain as the state of remnant polarization after the applied voltage is removed.

FRAM READ OPERATION

Similar to ferromagnetic capacitor, read operation is destructive. The original data, however, are saved at sense amplifier and can be restored back. In another word a read access is. Only complete after the second write that restores the original data.



-Timing diagram of Read Operation of the Memory cell -

The timing diagram for a read access is shown in Fig. 7. A read access begins by precharging the BL to 0V, followed by activating the WL (Δt_0). This establishes a capacitor divider consisting of C_{FE} and C_{BL} between the PL and the ground. Where C_{BL} represent the total amount of parasitic capacitance of the bit line. Depending on the data stored, the capacitance of the FE capacitor can be: approximated by C_0 or C_1 . That is C_{BL} and C_0 or C_1 act as a voltage divider, therefore the voltage developed on the bitline (V_x) can be one of the two.

$$V_X = \begin{cases} V_0 = \frac{C_0}{C_0 + C_{BL}} V_{DD} & \text{If the stored data is a "0"} \\ V_1 = \frac{C_1}{C_1 + C_{BL}} V_{DD} & \text{If the stored data is a "1"} \end{cases}$$

At this point, the sense amplifier is activated to drive the BL to V_{DD} if the voltage developed on the BL is V_1 or to 0V if the voltage on the BL is V_0 . The WL is kept activated until the sensed voltage on the BL restores the original data back into the memory cell and the BL is precharged back to 0V. The sense amplifier can discriminate between a "0" and "1" voltage signal on the BL. This is only possible if a reference voltage, midway between a "0" and a "1" signal.

COMPARISON

The memory cell of FRAM is configured with one transistor and one capacitor is DRAM. It can also hold data even when the power is switched off as can flash memory, which is a representative nonvolatile memory device. FRAM has a well-balanced combination of features of both RAM and ROM. FRAM can be rewritten more than 10^8 times, which is comparable to DRAM or SRAM in actual applications, while flash memory can be written to 10^5 times at maximum.

FRAM does not need an erase operation before it is rewritten. This is similar to DRAM or SRAM. On the other hand, Flash memory (or specific sectors) must be erased once to be rewritten. FRAM is characteristically easy to operate because it does not need to be refreshed to hold data unlike DRAM.

	FRAM	EEPROM	Flash Memory	DRAM	SRAM
Memory Type	Non-volatile	Non-volatile	Non-volatile	Volatile	Volatile
Read Cycle	100ns	200ns	120ns	70ns	85ns
Write Cycle	100ns	10us	100us	70ns	85ns
Power Consumption	1nJ	1uJ	2uJ	4uJ	3uJ
Current to retain Data	Unnecessary	Unnecessary	Unnecessary	Necessary	Necessary
Internal Write Voltage	2V-5V	14V	9V	3.3V	3.3V
Cell Structure	1T-1C	2T	1T	1T-1C	6T,4T+R
Area/Cell	4	3	1	2	4

CONCLUSION

Looking toward the future, we-anticipate progress in three areas: density, access and cycle times, and use as an embedded memory in system- on-chip technology. The density of commercial ferroelectric memory has improved dramatically over the past three years from 64 to 256 kb, with I-Mb densities expected soon.

Ferroelectric memories, on the other hand, are superior to EPROM's and Flash memories in terms of write-access time and overall power consumption, and hence, target applications where a nonvolatile memory is required with such features. Two examples of such applications are Contactless smart cards and digital cameras. Contactless smart cards require nonvolatile memories with low power consumption, as they use only electromagnetic coupling to power up the electronic chips on the card. Digital cameras require both low power consumption and fast frequent writes in order to store and restore an entire image into the memory in less than 0.1s.

Another advantage of ferroelectric memories over EEPROM's and Flash memories is that they can be easily embedded as part of a larger integrated circuit to provide system-on-a-chip solutions to various applications. Future personal wireless connectivity applications that are battery driven, such as third-generation cellular phones and personal digital assistants, will demand large amounts (multiple megabytes) of nonvolatile storage to retain accessed Internet Web pages, containing compressed video; voice, and data. The density and energy efficiency of writing data to memory would seem to indicate that ferroelectric memory will play a major role in these types of consumer products.

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