Memory

EBEY.S.RAJ

Contents

Random Access Memory

A memory unit is ***a collection of storage cells*** together with ***associated circuits*** needed to transfer information in and out the device.

Memory cells can be accessed for information transfer to or from any desired random location and hence the name ***Random Access Memory***.

Random Access Memory

A memory unit stores binary information in groups of bits called ***Words.***

A word in memory is an entity of bits that move in and out of storage as unit.

A memory word is a group of 1’s and 0’s and may represent a number, an instruction, one or more alphanumeric characters or any other binary coded information.

Random Access Memory

A group of 8 bits is called a ***Byte***.

Most computer memories use words that are multiples of 8 bits in length.

- 16 bit words
- 32 bit words

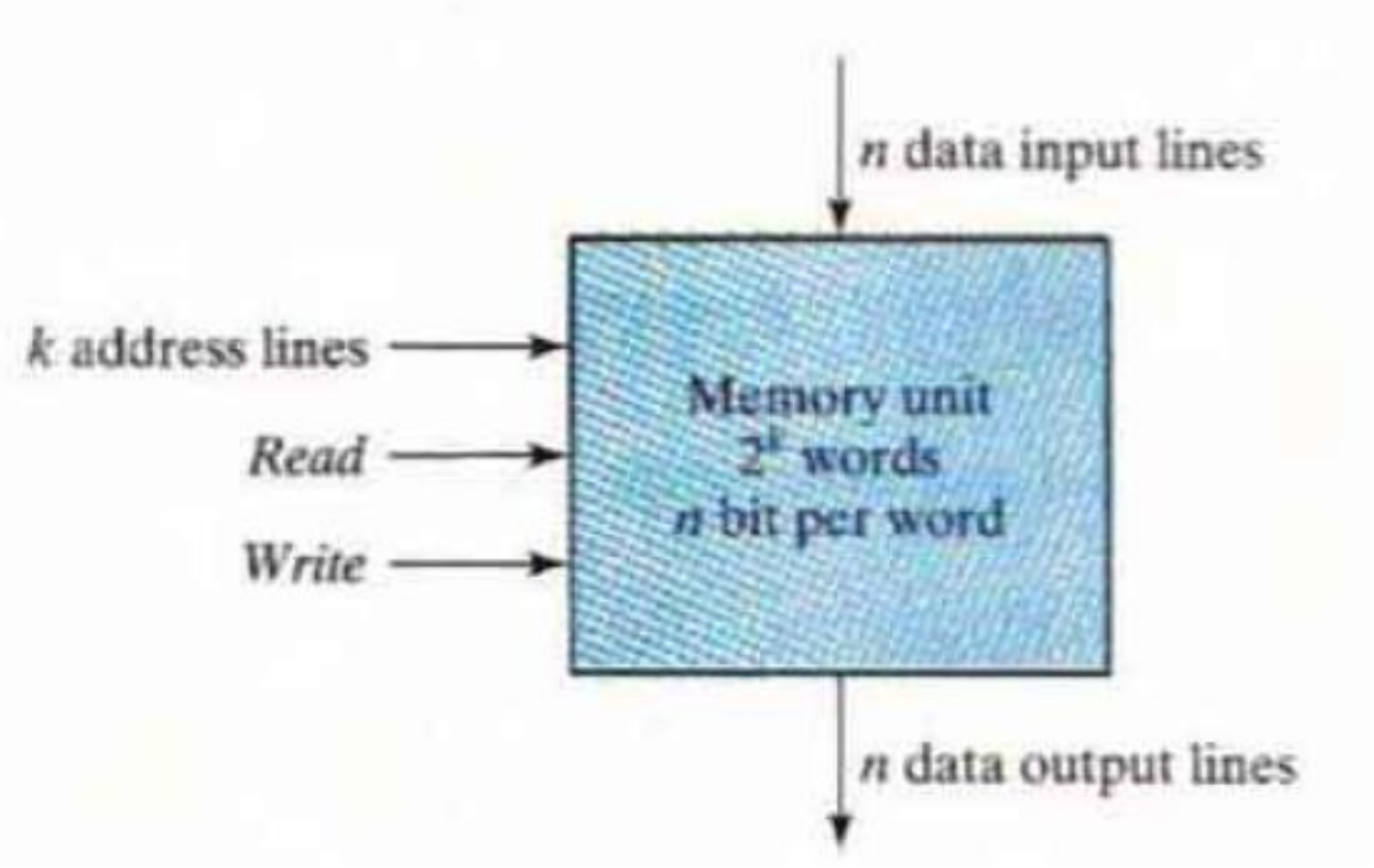
The capacity of memory unit is usually stated as the ***total number of bits*** that it can store.

Random Access Memory

The communication between a memory and its environment is achieved through

- ***Data input and output lines***
- ***Address selection lines***
- ***Control lines*** that specify the direction of transfer
  - Read
    - Binary data to be transferred out of the memory
  - Write
    - Binary data to be transferred into the memory

Block diagram of a memory unit



Random Access Memory

A memory unit is specified by the ***number of words it contains*** and the ***number of bits in each word***.

The address lines select one particular word.

Each word in memory is assigned an identification number called an address starting from 0 to 2^k -1 where k is the number of address lines.

The selection of a specific word inside the memory is done by applying the k-bit binary address to the address lines.

Random Access Memory

A decoder inside the memory accepts the address and opens the paths needed to select the word specified.

An example of 1024 x 16 memory

- 1024 words
- 16 bits per word

Contents of a 1024 x 16 memory

Memory address		Memory content
Binary	Decimal	
0000000000	0	1011010101011101
0000000001	1	1010101110001001
0000000010	2	0000110101000110
⋮	⋮	⋮
1111111101	1021	1001110100010100
1111111110	1022	0000110100011110
1111111111	1023	1101111000100101

Random Access Memory: Write and read

Write operation

- Write signal specifies a **transfer-in** operation
- Steps
  - Transfer the **binary address** of the desired word into the **address lines**
  - Transfer the **data bits** that must be stored in memory to the **data lines**
  - Activate the **write** signal
- The memory unit will then take the bits from the input data lines and store them in the word specified by the address lines

Random Access Memory: Write and read

Read operation

- Read signal specifies a **transfer-out** operation.
- Steps
  - Transfer the **binary address** of the desired word into the **address lines**
  - Activate the **Read** signal
- The memory unit will then take the bits from the selected word and apply them to the output data lines.
- The content of the selected word does not change after reading.

Random Access Memory: Write and read

Memory Enable (Chip Select)

- Instead of having separate read and write inputs, some ICs provide two other control inputs
  - One input selects the unit which is called Memory Enable (Chip Select)
  - Other determines the operation(Read/$\overline{\text{Write}}$)
- Memory Enable is used to enable the particular memory chip in a multichip implementation of a large memory.

Memory Enable	Read/ $\overline{\text{Write}}$	Memory Operation
0	X	None
1	0	Write to Selected Word
1	1	Read from Selected Word

Types of Memories

Volatile Memory

- Lose the stored information when the power is turned off.
- Both Static RAM and Dynamic RAM are Volatile Memories
- SRAM
  - Consists essentially of internal flip flops that store the binary information
  - The stored information remains valid as long as the power is applied to the unit.
  - Static RAMs are easier to use and have shorter read and write cycles.
  - Used in Cache Memory

Types of Memories

- DRAM
  - Stores the binary information in the form of electric charges that are applied to the capacitors.
  - The stored charge on the capacitors tends to discharge with time.
  - The capacitors must be periodically recharged by refreshing the dynamic memory.
  - Refreshing is done by cycling through the words every few milliseconds to restore the decaying charge.
  - Reduced power consumption
  - Larger storage capacity in a single memory chip.

Types of Memories

Non Volatile Memory

- Retains its stored information after removal of power.

Examples

- Magnetic Disks
  - Data stored on magnetic components is manifested by the direction of magnetization.
- Read Only Memory(ROM)
  - Programs and data that cannot be altered are stored in ROM

Memory Decoding

In addition to the storage components in a memory unit, there is a need for decoding circuits to select the memory word specified by the input address.

Such circuits are **Internal decoders**

In addition to internal decoders, there are external decoders.

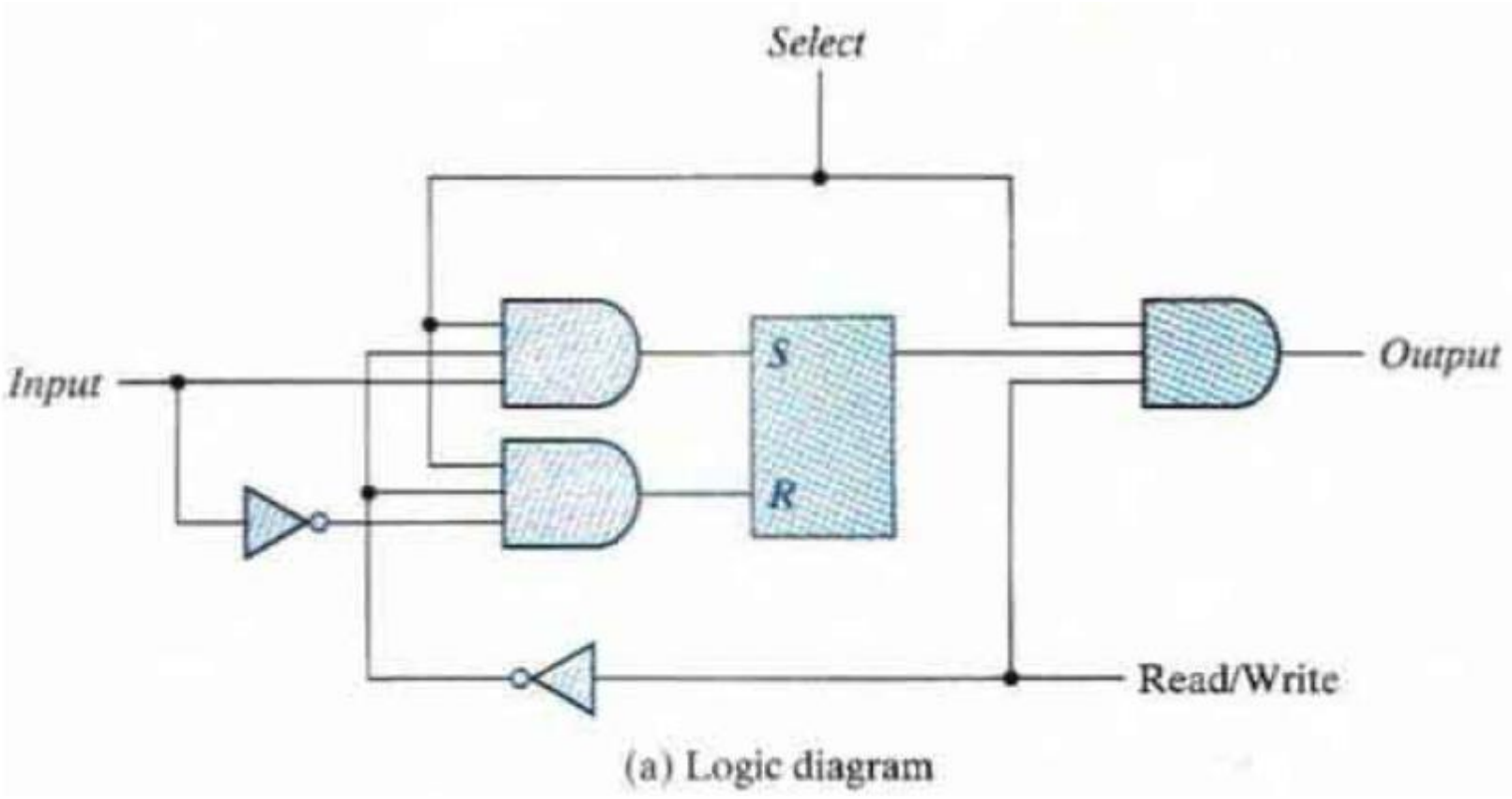
External decoders are used when integrated circuit RAM chips are connected in a multichip memory configuration

Memory Decoding

The internal construction of a RAM of *m* words with *n* bits per word consists of ***m x n*** binary storage cells and associated decoding circuits for selecting individual words.

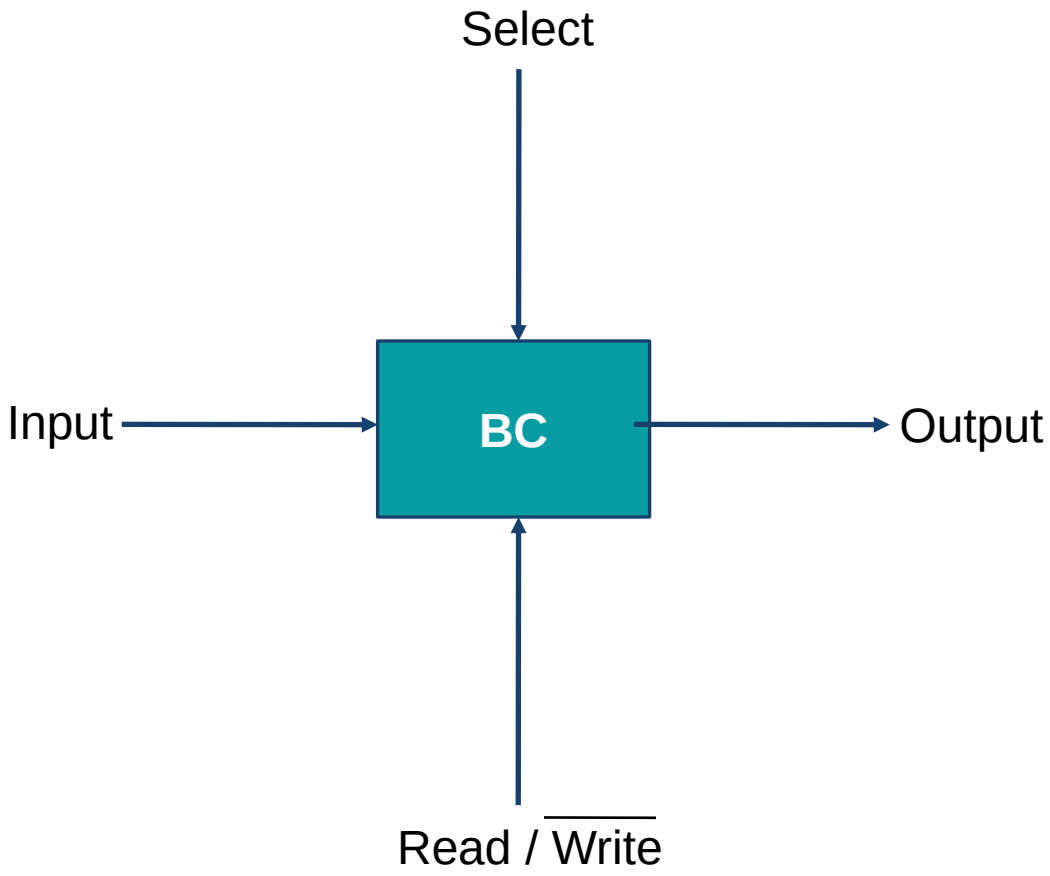
The binary storage cell is the basic building block of a memory unit.

Memory Decoding: Logic diagram of a Memory Cell

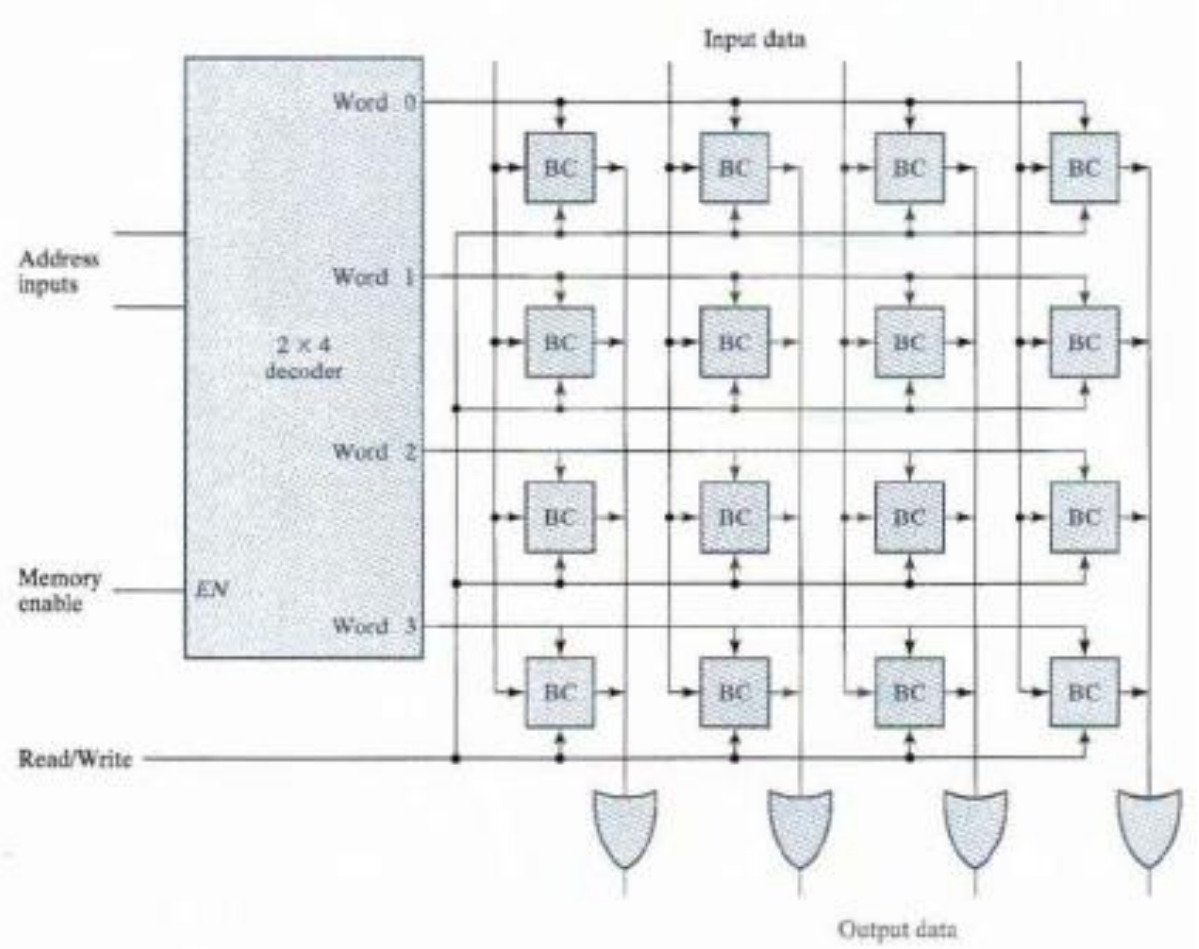


(a) Logic diagram

Memory Decoding: Logic diagram of a Memory Cell



Logic construction of a 4 x 4 RAM



Logical Construction

The RAM consists of four words of four bits each and has a total of 16 binary cells.

The small blocks labeled BC represent the binary cell with its three inputs and one output.

A memory with four words need two address lines. The two address inputs go through a 2 x 4 decoder to select one of the four words.

The decoder is enabled with the memory-enable input.

When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected.

When the memory enable is 1, one of the four words is selected, dictated by the value in the two address lines.

Once a word has been selected. the read/write input determine the operation.

During the read operation. the four bits of the selected word go through OR gates to the output terminal.

During the write operation. the data available in the input lines are transferred into the four binary cells of the selected word.

The binary cells that are not selected are disabled and their previous binary values remain unchanged.

Memory Decoding

Commercial RAMs may have a capacity of thousands of words and each word may range from 1 to 64 bits.

A memory with 2^k words of n bits per word requires

k address lines that go into a k to 2^k decoder.

Each one of the decoder outputs selects one word of n bits for reading or writing.

Memory Decoding: Array of RAM chips

If the memory unit needed for an application is larger than the capacity of one chip, it is necessary to combine a number of chips in an array to form the required memory size.

The capacity of the memory depends on two parameters

- Number of words.
- Number of bits per word.

Memory Decoding: array of RAM chips

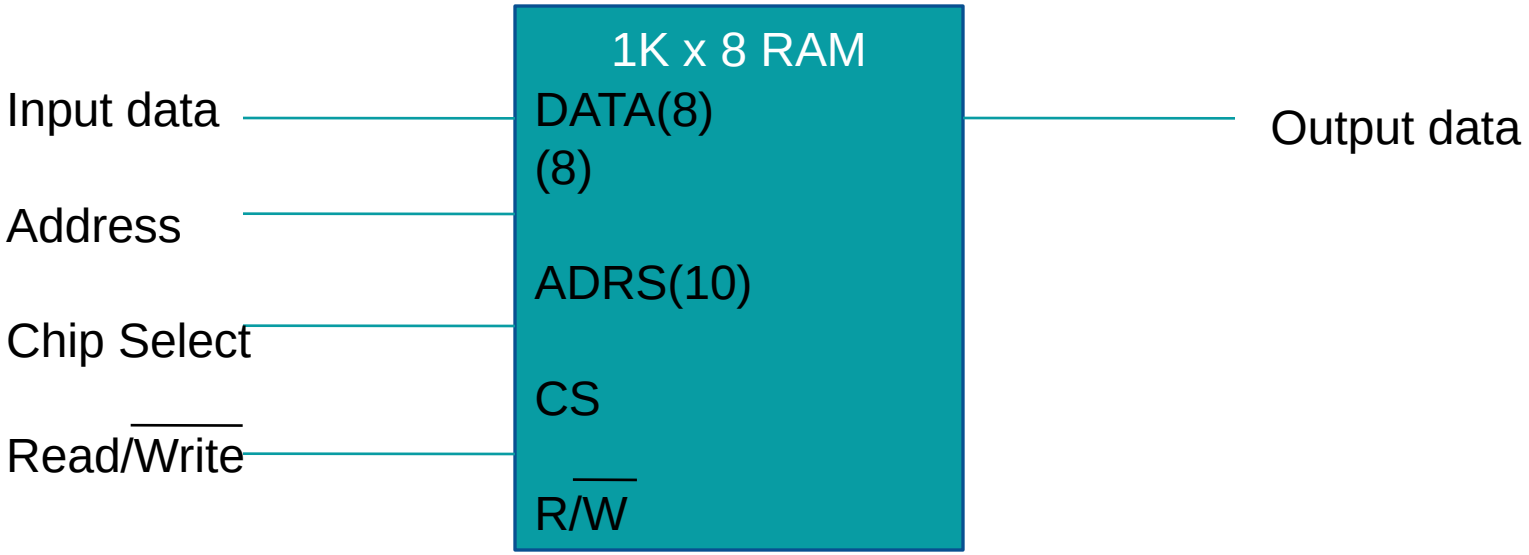
An **increase in the number of words** requires that we increase the address length

- Every bit added to the address length doubles the number of words in memory.

An **increase in the number of bits per word** requires that we increase the length of the input and output data lines, but the address length remains the same.

Block diagram of a typical RAM chip

1K x 8 RAM chip : Contains1024 words of 8 bits each



Address Multiplexing

The SRAM memory cell typically contains six transistors.

For memories with higher density, it is necessary to reduce the number of transistors in a cell.

The DRAM cell contains a single MOS transistor and a capacitor.

The charge stored on the capacitor discharges with time, and the memory cells must be periodically recharged by refreshing the memory.

DRAMs typically have four times the density of SRAMs.

The cost per bit of DRAM storage is three to four times less than that of SRAM storage.

Lower Power requirement of DRAM cells.

These advantages make DRAM the preferred technology for large memories in personal digital computers.

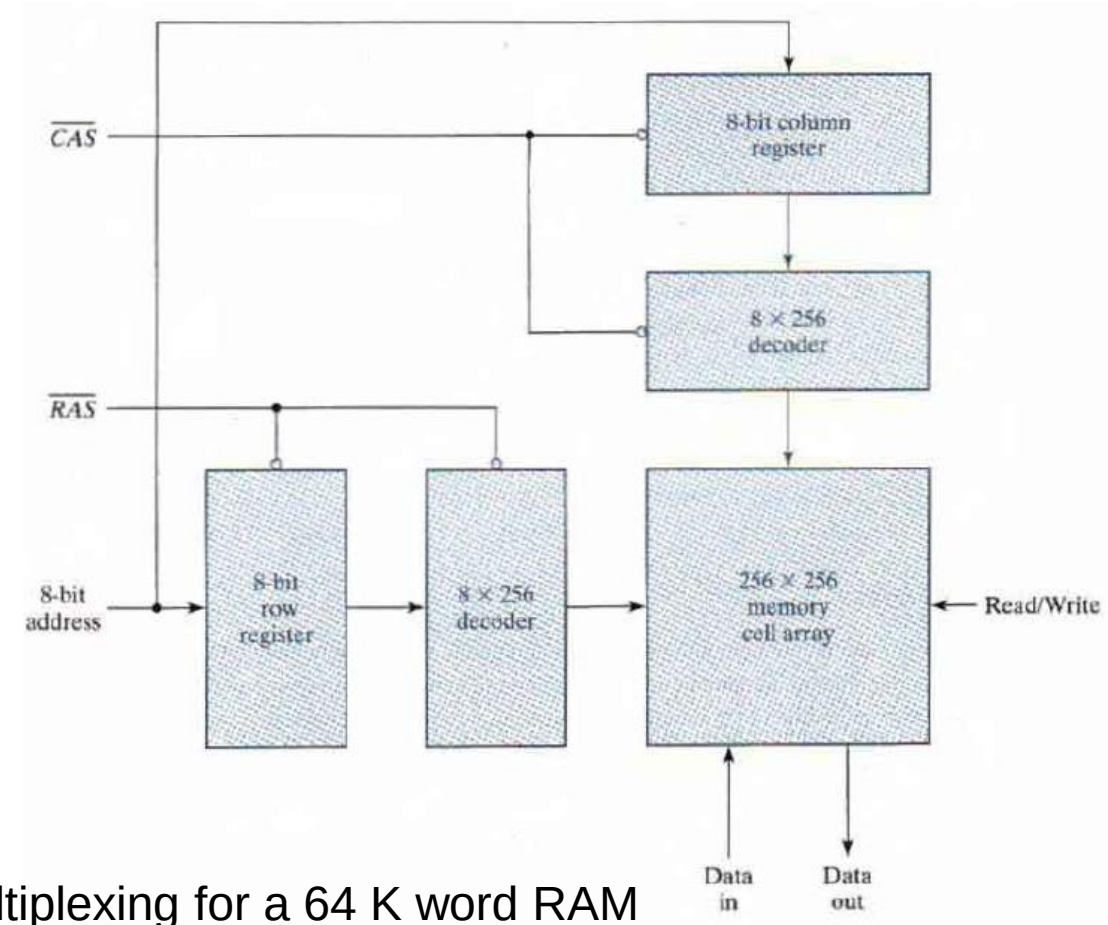
Address Multiplexing

To reduce the number of pins in the IC package, designers utilize address multiplexing whereby one set of address input pins accommodates the address components.

In a two-dimensional array, the address is applied in two parts at different times, with the row address first and the column address second.

Since the same set of pins is used for both parts of the address, the size of the package is decreased significantly.

Address Multiplexing



Address Multiplexing for a 64 K word RAM

Address Multiplexing

There is a single data input line, a single data output line, and a read/write control as well as an eight-bit address input and two address **strobes**.

The strobes are included for enabling the row and column address into their respective registers.

The Row Address Strobe (RAS) enables the eight-bit row register and the Column Address Strobe (CAS) enables the eight-bit column register.

The bar on top of the name of the strobe symbol indicates that the registers are enabled on the zero level of the signal

Read Only Memory(ROM)

A ROM is essentially a memory device in which permanent binary information is stored.

The binary information must be specified by the designer and is then embedded in the unit to form the required interconnection pattern.

Once the pattern is established, it stays within the unit even when power is turned off and on again.

Read Only Memory(ROM)

A block diagram of a ROM consisting of ***k inputs*** and ***n outputs***

Inputs : The address for memory

Outputs : Data bits of the stored word that is selected by the address.

Read Only Memory(ROM)

The number of words in a ROM is determined from the fact that ***k address input lines*** are needed to specify ***2^k words***.

ROM does not have data inputs.

Integrated circuit ROM chips have one or more enable inputs

ROM Example: 32 x 8 ROM

The unit consists of 32 words of 8 bits each.

There are five input lines that form the binary numbers from 0 through 31 for the address.

The five inputs are decoded into 32 distinct outputs by means of a 5 X 32 decoder.

Each output of the decoder represents a memory address.

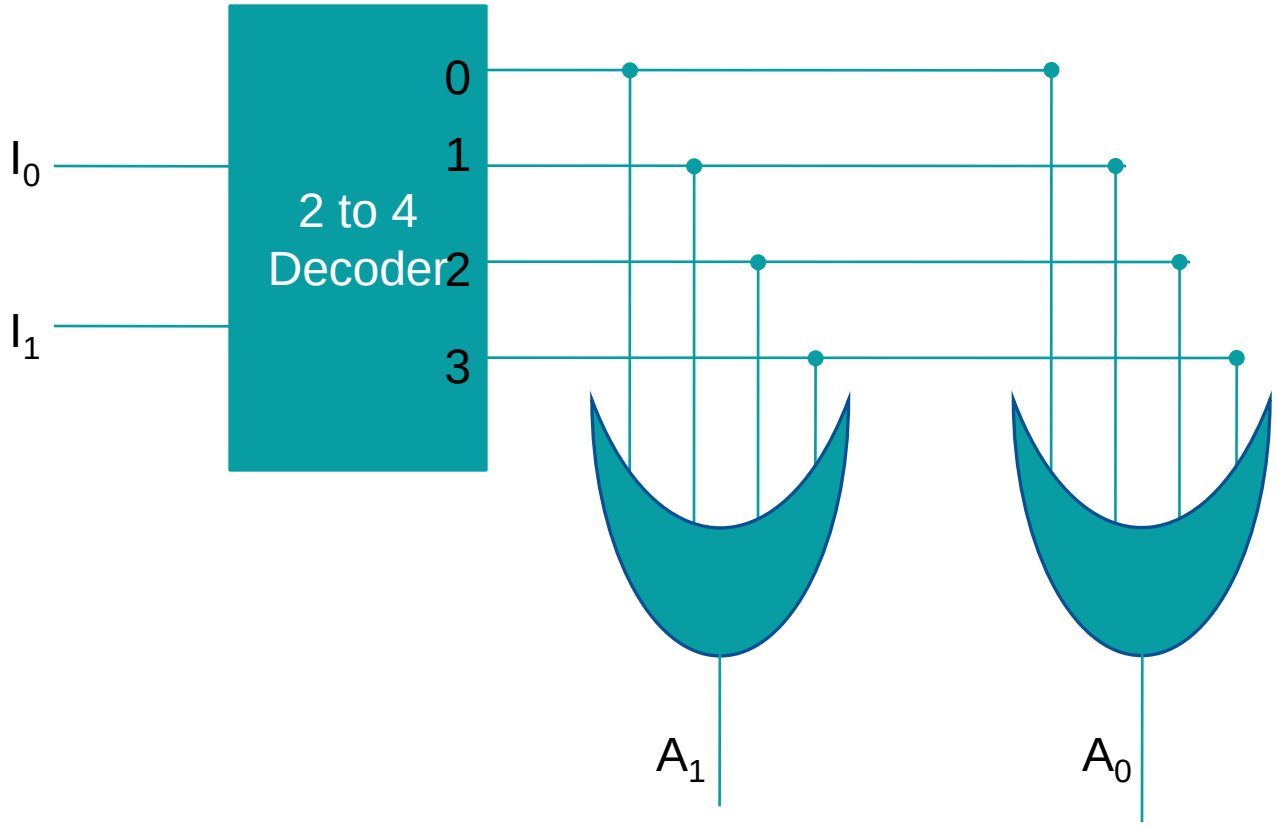
ROM Example: 32 x 8 ROM

The 32 outputs of the decoder are connected to each of the eight OR gates.

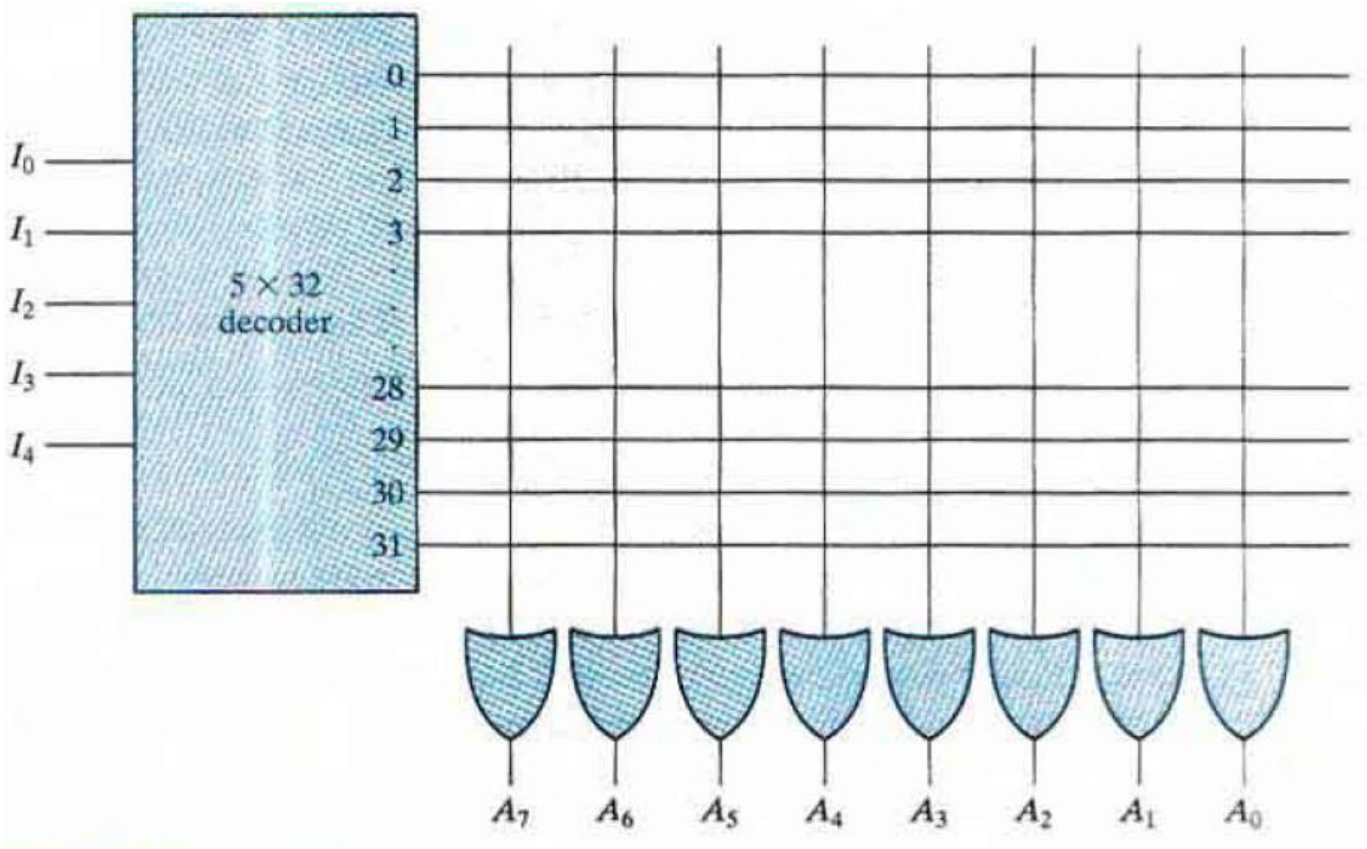
- Each OR gate must be considered as having 32 inputs.
- Each output of the decoder is connected to one of the inputs of each OR gate.
- Since each OR gate has 32 input connections and there are 8 OR gates, the ROM contains **32 x 8 = 256 internal connections**.

Generally a '2^k x n' ROM will have an internal 'k x 2^k' decoder and 'n' OR gates. Each OR gate has 2^k inputs, which are connected to each of the outputs of the decoder.

4 x 2 ROM



Internal construction of 32 x 8 rom



Programmable Read Only Memory(PROM)

A programmable connection between two lines is logically equivalent to a switch that can be altered to be either **closed** (meaning that the two lines are connected) or **open** (meaning that the two lines are disconnected).

The programmable intersection between two lines is sometimes called a ***crosspoint.***

Various physical devices are used to implement crosspoint switches.

- One of the simplest technologies employs a fuse that normally connects the two points but is opened or "blown" by the application of a high-voltage pulse into the fuse.

Programmable Read only memory(PROM)

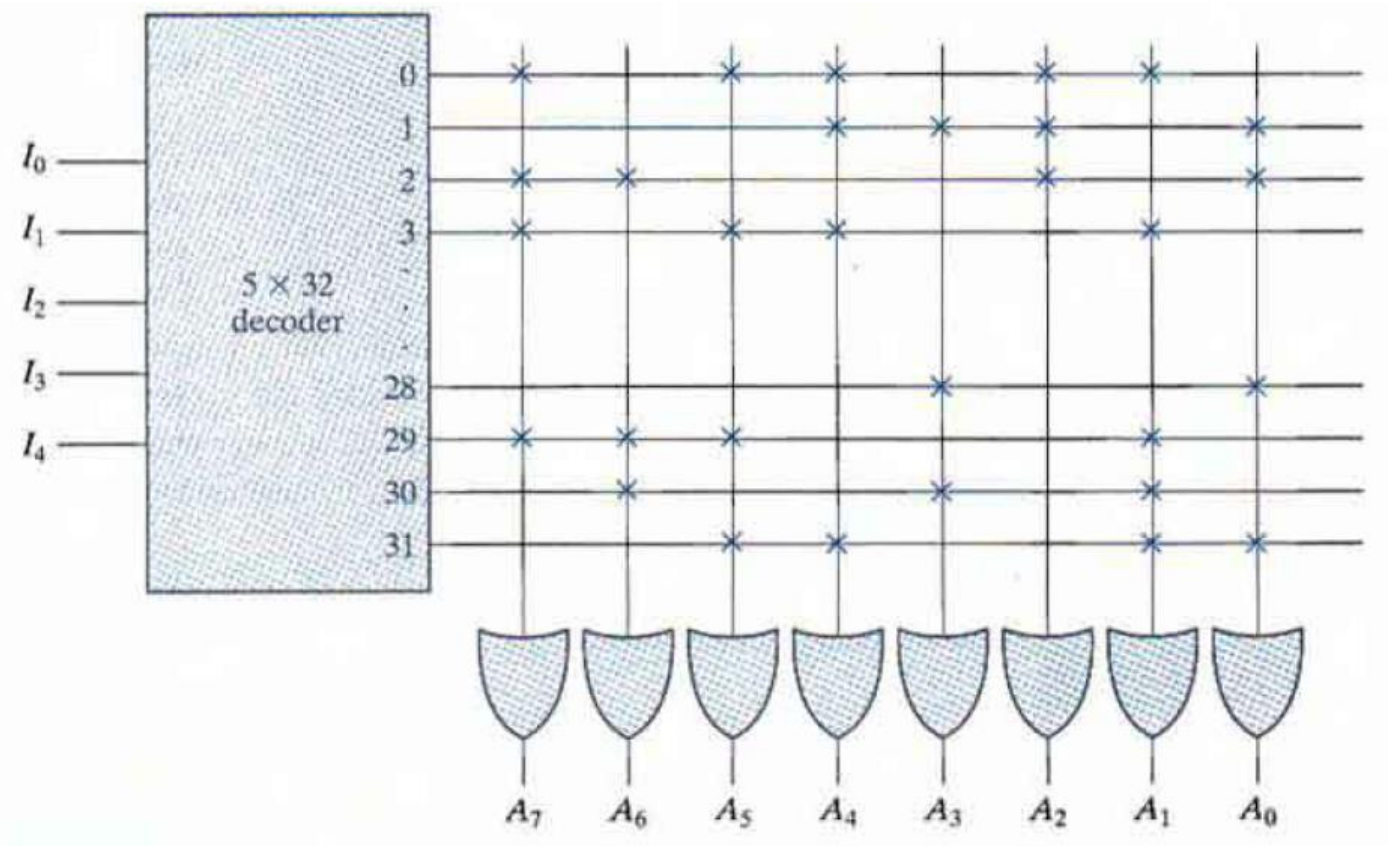
The internal binary storage of a ROM is specified by a truth table that shows the word content in each address.

An Example

ROM Truth Table (Partial)

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		⋮							⋮			
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

Programming the ROM according to the truth table



Every 0 listed in the truth table specifies the absence of a connection and every 1 listed specifies a path that is obtained by a connection.

Combinational Circuit implementation using PROM

The ROM is a device that includes both the decoder and the OR gates within a single device to form a minterm generator.

By choosing connections for those minterms which are included in the function, the ROM outputs can be programmed to represent the Boolean functions of the output variables in a combinational circuit.

Each output terminal is considered separately as the output of a Boolean function expressed as a sum of minterms.

Output A_7, can be expressed in sum of minterms as

$$A_7(I_4, I_3, I_2, I_1, I_0) = \sum m(0, 2, 3.... . 29)$$

Combinational Circuit implementation using PROM: An example

Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number.

Inputs			Outputs						
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

Combinational Circuit implementation using PROM

Three inputs and six outputs are needed to accommodate all possible binary numbers. So 8 x 6 ROMs can be used.

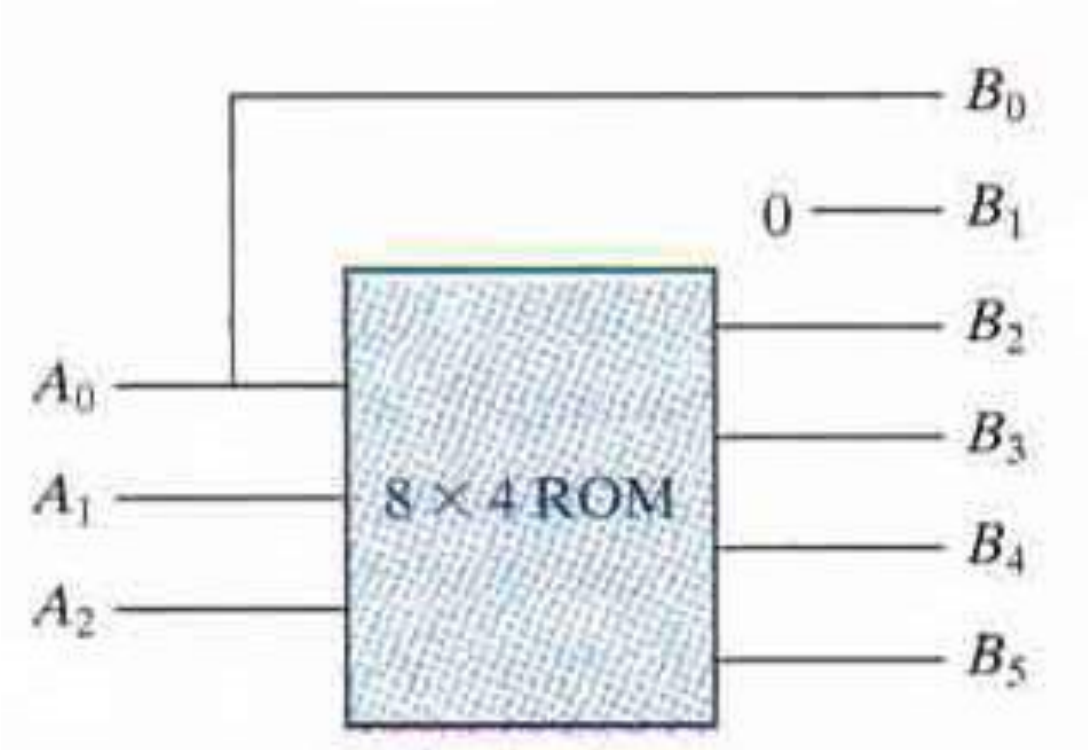
But output B_0 is always equal to input A_0, so there is no need to generate B_0 with a ROM.

Output B_1 is always 0, so this output is a known constant.

So we actually need to generate only four outputs with the ROM

So the minimum size of ROM needed must have three inputs and four outputs. So we need only 8 x 4 ROM.

Combinational Circuit implementation using PROM



A_2	A_1	A_0	B_5	B_4	B_3	B_2
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

(b) ROM truth table

Types of ROMs

The required paths in a ROM may be programmed in four different ways.

- Mask Programming
- Programmable ROMs(PROMs)
- Erasable Programmable ROMs(EPROMs)
- Electrically Erasable Programmable ROMs(EEPROMs)

Types of ROMs: Mask Programming

Done by the semiconductor company during the last fabrication process of the unit.

The procedure for fabricating a ROM requires that

- The customer fill out the truth table
- The truth table may be submitted to the manufacturer
- The manufacturer makes the corresponding mask for the paths to produce the 1's and 0's according to the customer's truth table.

This procedure is costly because the vendor charges the customer a special fee for custom masking the particular ROM.

Mask programming is economical only if a large quantity of the same ROM configuration is to be ordered.

Types of ROMs: PROM

For small quantities, it is more economical to use **Programmable Read-Only Memory, or PROM.**

PROM units contain all the fuses intact, giving all 1's in the bits of the stored words.

- The fuses in the PROM are blown by the application of a high-voltage pulse to the device through a special pin.
- A blown fuse defines a binary 0 state and an intact fuse gives a binary 1 state.

Special instruments called PROM programmers are available commercially to facilitate the procedure.

Procedures for programming ROMs are hardware procedures

Types of ROMs: EPROM

PROMs is irreversible

- Once programmed, the fixed pattern is permanent and cannot be altered.

A third type of ROM is the **Erasable PROM** or **EPROM**.

It can be restructured to the initial state even though it has been programmed previously.

- When the EPROM is placed under a special ultraviolet light for a given length of time, the shortwave radiation discharges the internal floating gates that serve as the programmed connections.

After erasure, the EPROM returns to its initial state and can be reprogrammed to a new set of values.

Types of ROMs: EEPROM

The fourth type of ROM is the **Electrically Erasable PROM (EEP ROM)**.

Similar to EPROM, except that the previously programmed connections can be erased with **an electrical signal** instead of ultraviolet light.

The advantage is that the device can be **erased without removing it from its socket**.

Flash memory devices are similar to EEPROMs, but have additional built-in circuitry to selectively program and erase the device in-circuit, without the need for a special programmer.

Their low power consumption makes them an attractive storage medium for laptop and notebook computers.

Combinational PLDs

Combinational Programmable Logic Device (Combinational PLD) is an integrated circuit with programmable gates divided into an AND array and an OR array to provide an AND-OR sum-of-product implementation.

Three types of Combinational Programmable Logic Devices(Combinational PLDs), differing in the placement of the programmable connections in the AND-OR array.

- PROMS
- PAL
- PLA

Combinational PLDs

PROM

- The PROM has a fixed AND array constructed as a decoder and a programmable OR array. The programmable OR gates implement the Boolean functions in sum-of-minterms form.

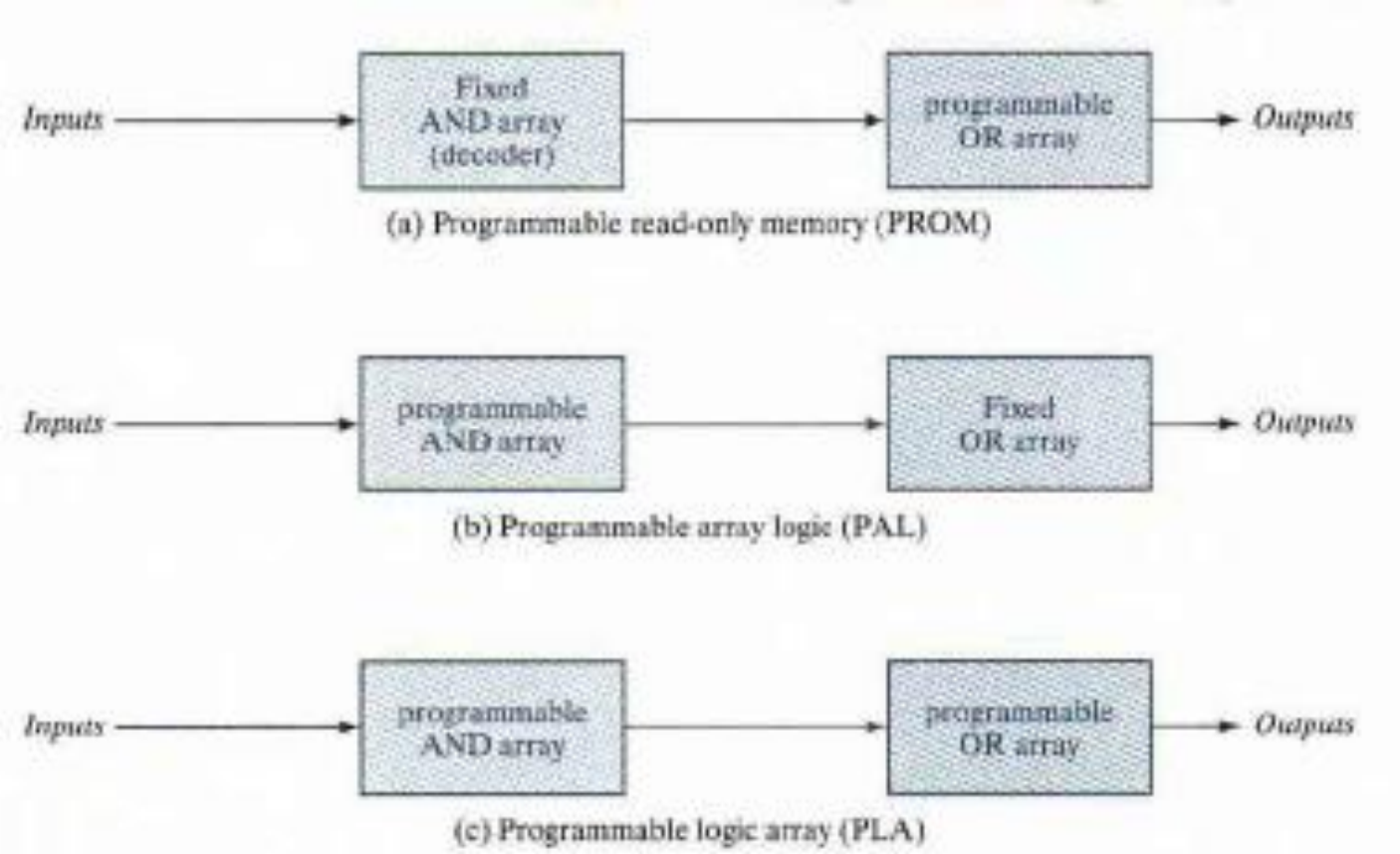
PAL

- The PAL has a programmable AND array and a fixed OR array.
- The AND gates are programmed to provide the product terms for the Boolean functions. which are logically summed in each OR gate.

PLA

- The most flexible PLD is the PLA, in which both the AND and OR arrays can be programmed.
- The product terms in the AND array may be shared by any OR gate to provide the required sum-of-products implementation.

Combinational PLDs



References

Digital Logic and Computer Design : M.Morris Mano

Digital Design : M.Morris Mano and Michael .D.Ciletti

Thank You

PREPARED BY

EBEY S.RAJ

ASST PROF(IT)

GECPKD