

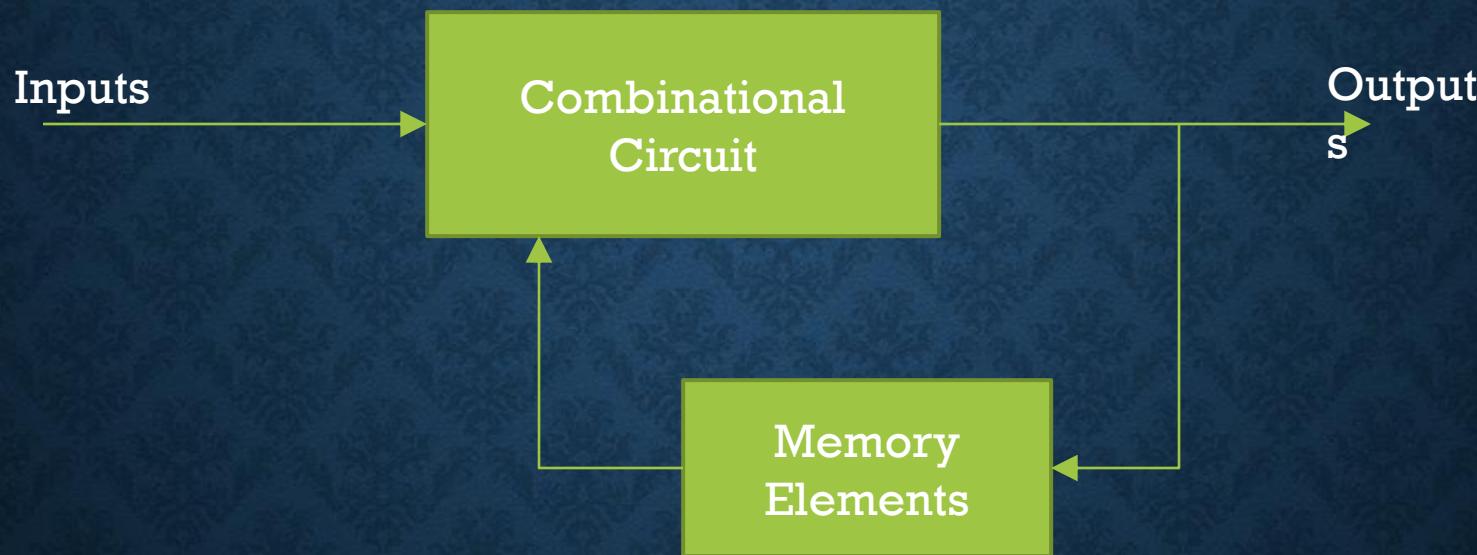
SEQUENTIAL CIRCUITS

Ebey S.Raj

INTRODUCTION

- Combinational switching circuits
 - O/p at any instant depends only on the present inputs at that time
 - Eg: Adders, Subtractors, Encoders, Multiplexers etc
- Sequential Switching Circuits
 - O/p at any instant depends not only on the present inputs at that time but also on the present state of the circuit.
 - Eg: Counters, Shift Registers, Serial Adder, Sequence Generator etc

BLOCK DIAGRAM OF A SEQUENTIAL CIRCUIT



The information stored in the memory element at any given time defines the present state of the sequential circuit

COMPARISON BETWEEN COMBINATIONAL AND SEQUENTIAL CIRCUITS

Combinational circuits

- Output
 - The o/p variable at any instant of time depends only on present input variables.
- Memory
 - Memory Unit is not required

Sequential circuits

- Output
 - The o/p variable at any instant of time depends not only on the present input variables but also on the present state.
- Memory
 - Memory Unit is required to store the past history of the input variables

COMPARISON BETWEEN COMBINATIONAL AND SEQUENTIAL CIRCUITS

Combinational circuits

- Speed
 - Faster because the delay between the i/p and o/p is due to the propagation delay of gates only
- Design
 - Easy to design

Sequential circuits

- Speed
 - Slower than combinational circuits
- Design
 - Comparatively harder to design

SEQUENTIAL CIRCUITS

- Depending on the timing of their signals, there are two types of Sequential Circuits
 - Synchronous Sequential Circuits
 - Its behavior can be defined from the knowledge of its signals at discrete instants of time.
 - Controlled by a Clock
 - Asynchronous Sequential Circuits
 - Its behavior depends upon the order in which its input signals change and can be affected at any instant of time.
 - Not controlled by a clock.

SYNCHRONOUS SEQUENTIAL CIRCUITS

- Synchronization is achieved by a timing device called a **Master Clock Generator**, which generates a periodic train of clock pulses.
- Periodic recurring pulse is called a **Clock**.
- The desired operations take place only when the **clock pulse occurs**.

COMPARISON BETWEEN SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS

Synchronous sequential circuits

- Memory elements are **clocked Flip flops**.
- Change in i/p signals affect memory elements upon activation of **clock signal**.
- Maximum operating speed of the clock depends on the **time-delays involved**.
- **Easier** to design

Asynchronous sequential circuits

- Memory elements are either **Unclocked FlipFlops** or time delay elements
- Change in i/p signals can affect memory elements **at any instant of time**.
- Operate **faster** than synchronous circuits due to the absence of clock
- More **difficult** to design.

FLIP FLOPS AND LATCHES

- Flip flops are the basic building blocks of most sequential circuits.
- Flip flop is formally a **Bistable Multivibrator**, having two stable states.
- It can remain in either of the states indefinitely.
- Its state can be changed by applying the proper triggering signal.
- It is also called a Binary or One-bit memory.

FLIP FLOPS AND LATCHES



The state of the flip flop always refer to the state of the normal o/p, Q

FLIP FLOPS AND LATCHES

- A flip flop is said to be in HIGH state or logic-1 state or SET state when $Q = 1$.
- A flip flop is said to be in LOW state or logic-0 state or RESET state or CLEAR state when $Q = 0$.

FLIP FLOPS AND LATCHES

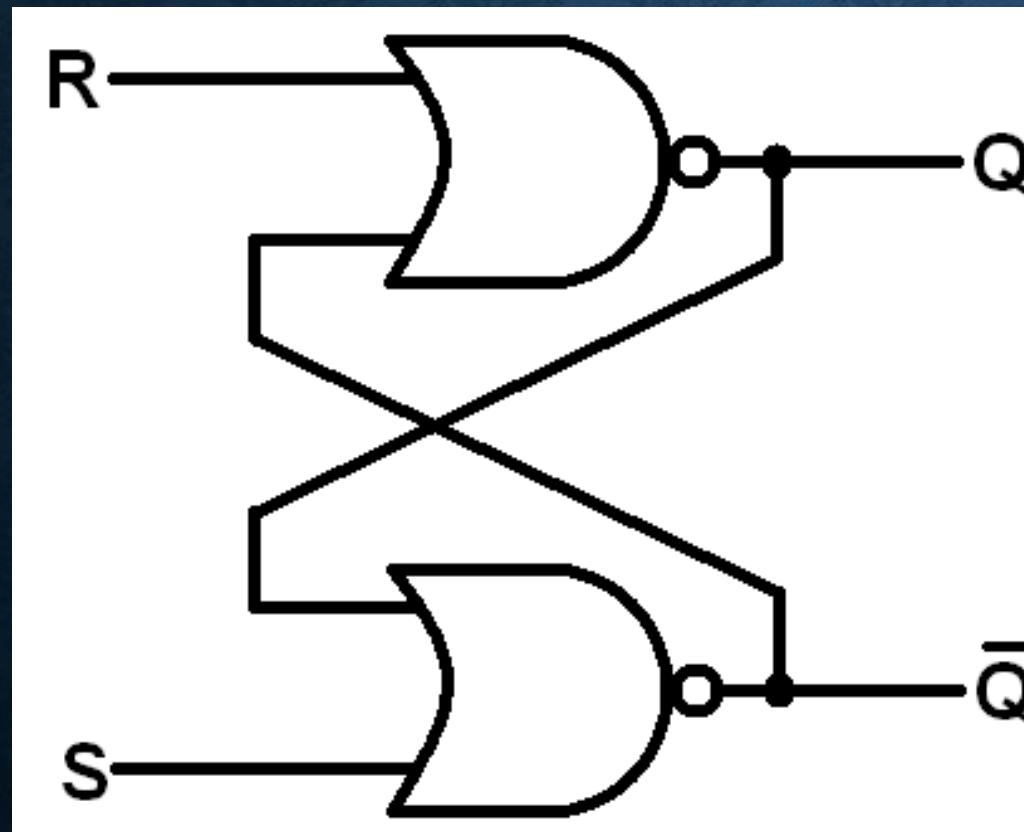
- A flip flop can have one or more inputs.
- The input signals which command the flip flop to change state are called **Excitations**.
- These i/p's are used to cause the flip flop to switch back and forth between its possible outputs.
- The o/p will remain in the new state even after the input pulse has been removed. This is the flip flop's memory characteristic.
- Flip Flop serves as a storage device. It stores a 1 when its Q o/p is a 1 and stores a 0 when its Q o/p is 0.

FLIP FLOPS AND LATCHES

- Latch refers to non-clocked flip flops, not dependent on the clock signal.
- Latches ‘latch on’ to a ‘1’ or a ‘0’ immediately upon receiving the input pulse called SET or RESET.
- Gated latches(Clocked Flip flops) are latches which respond to the i/p/s and latch on to a ‘1’ or a ‘0’ only when they are **enabled**, ie when the ENABLE i/p or gating signal is HIGH.

BASIC FLIP FLOP CIRCUITS

Direct Coupled RS Flip Flop (SR Latch)



Active HIGH S-R Latch

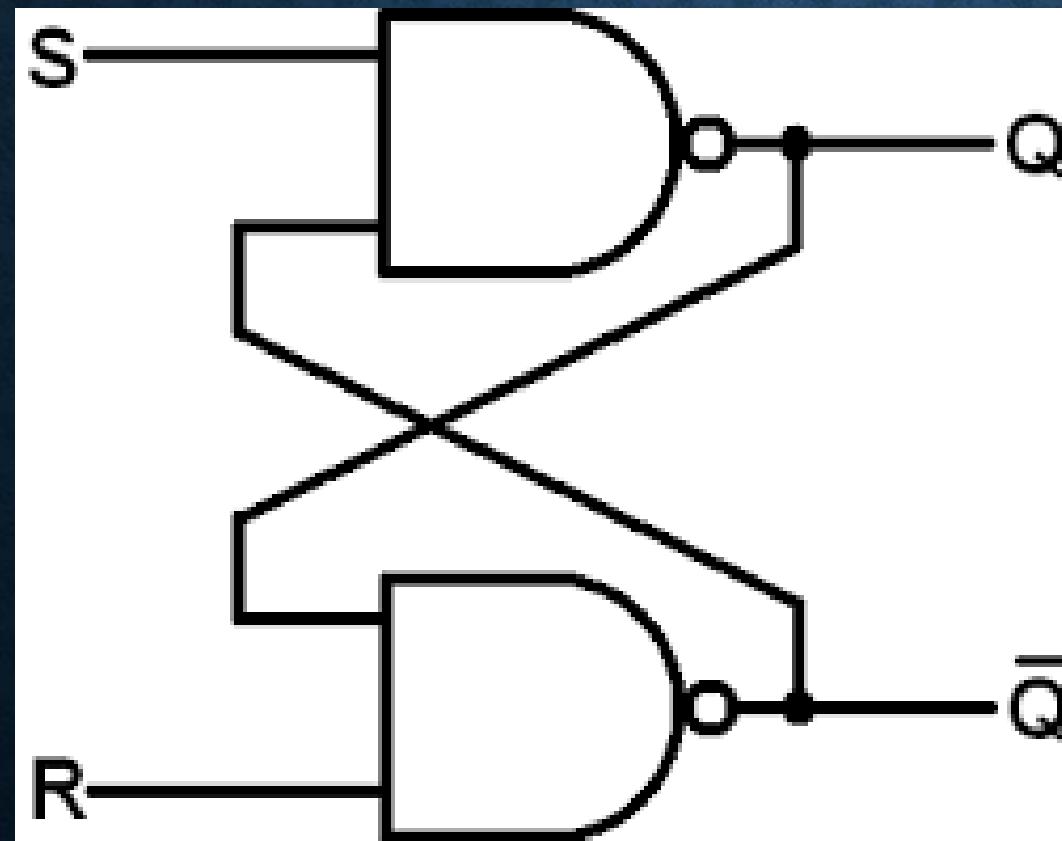
S	R	Q	Q'	
1	0	1	0	SET
0	0	1	0	Memory
0	1	0	1	RESET
0	0	0	1	Memory
1	1	0	0	Unstable

BASIC FLIP FLOP CIRCUITS

- A flip flop ckt can be constructed from two NAND gates or two NOR gates.
- The cross coupled connection from the o/p of one gate to the i/p of the other gate constitutes a Feedback path.
- Asynchronous sequential circuit
- Each FF has 2 o/p's, Q and Q and 2 i/p's, SET and RESET.

BASIC FLIP FLOP CIRCUITS

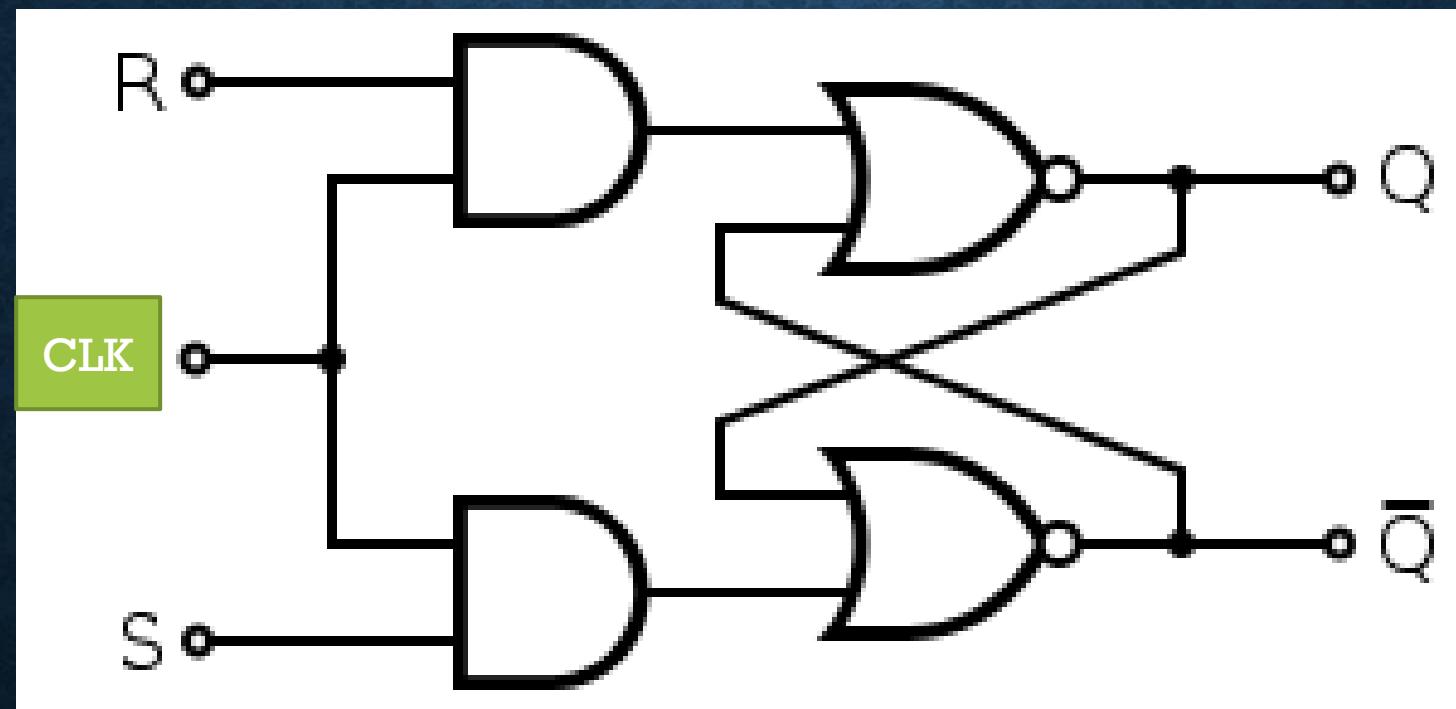
Direct Coupled RS Flip Flop (SR Latch)



Active LOW S-R Latch

S	R	Q	Q'	
1	0	0	1	RESET
1	1	0	1	Memory
0	1	1	0	SET
1	1	1	0	Memory
0	0	1	1	Unstable

CLOCKED R-S FLIP FLOP



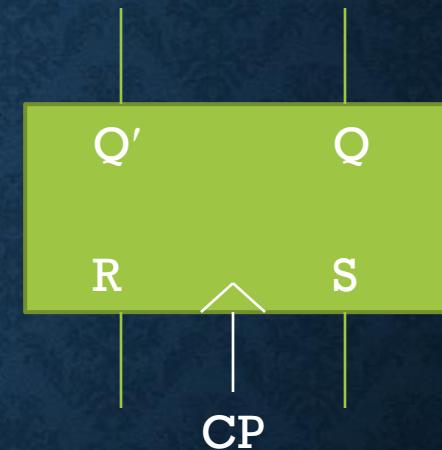
CLOCKED R-S FLIP FLOP

Q	S	R	Q_{t+1}	
0	0	0	0	Memory
0	0	1	0	RESET
0	1	0	1	SET
0	1	1	-	Indeterminate
1	0	0	1	Memory
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	-	Indeterminate

Characteristic Table

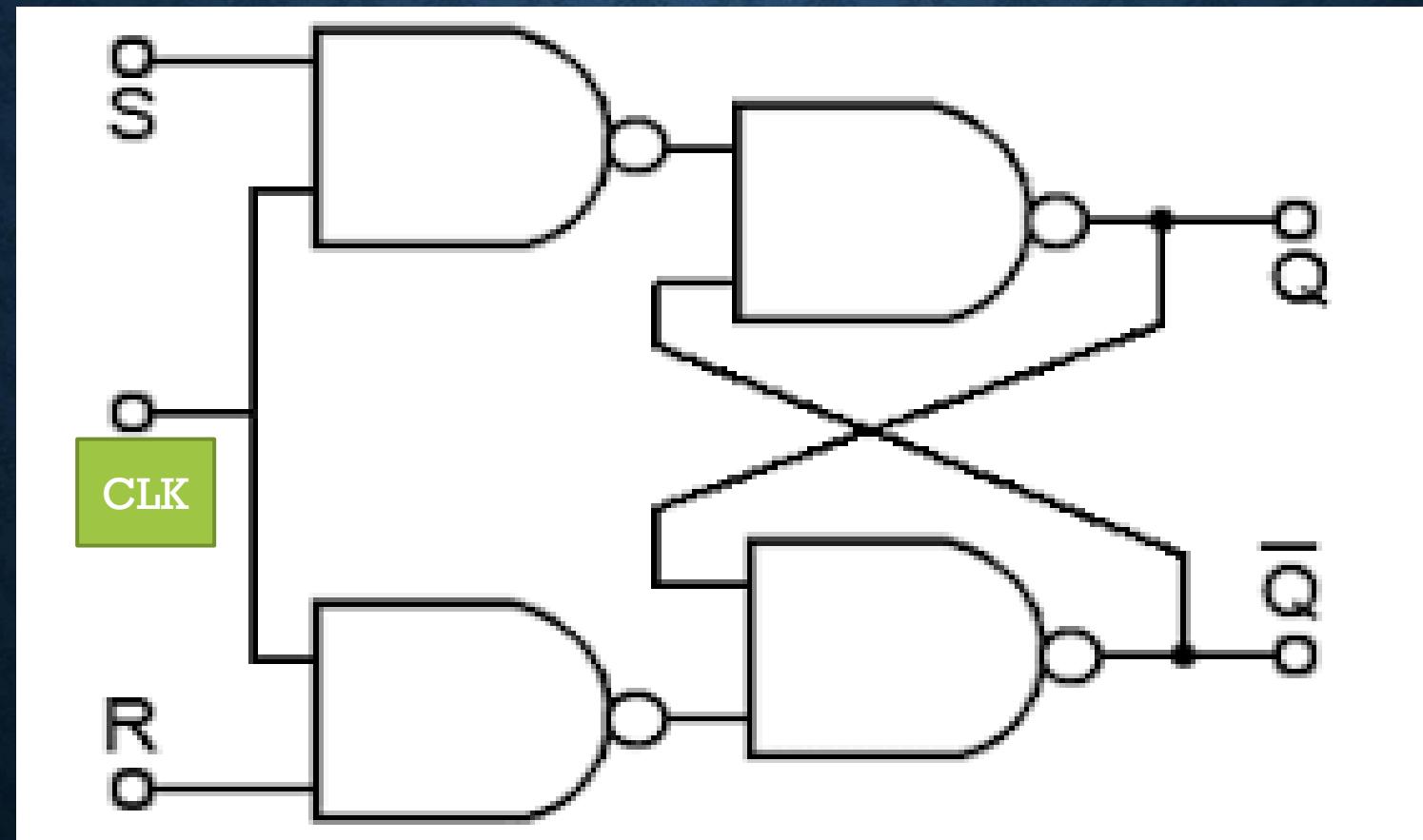
Also called **Gated S-R Latch** or
Synchronous S-R Latch

Characteristic Equation
 $Q_{t+1} = S + QR'$
 $S \cdot R = 0$



Logic Symbol
(Edge Triggered)

CLOCKED R-S FLIP FLOP/ GATED S-R LATCH (USING NAND GATES ONLY)



CLOCKED R-S FLIP FLOP

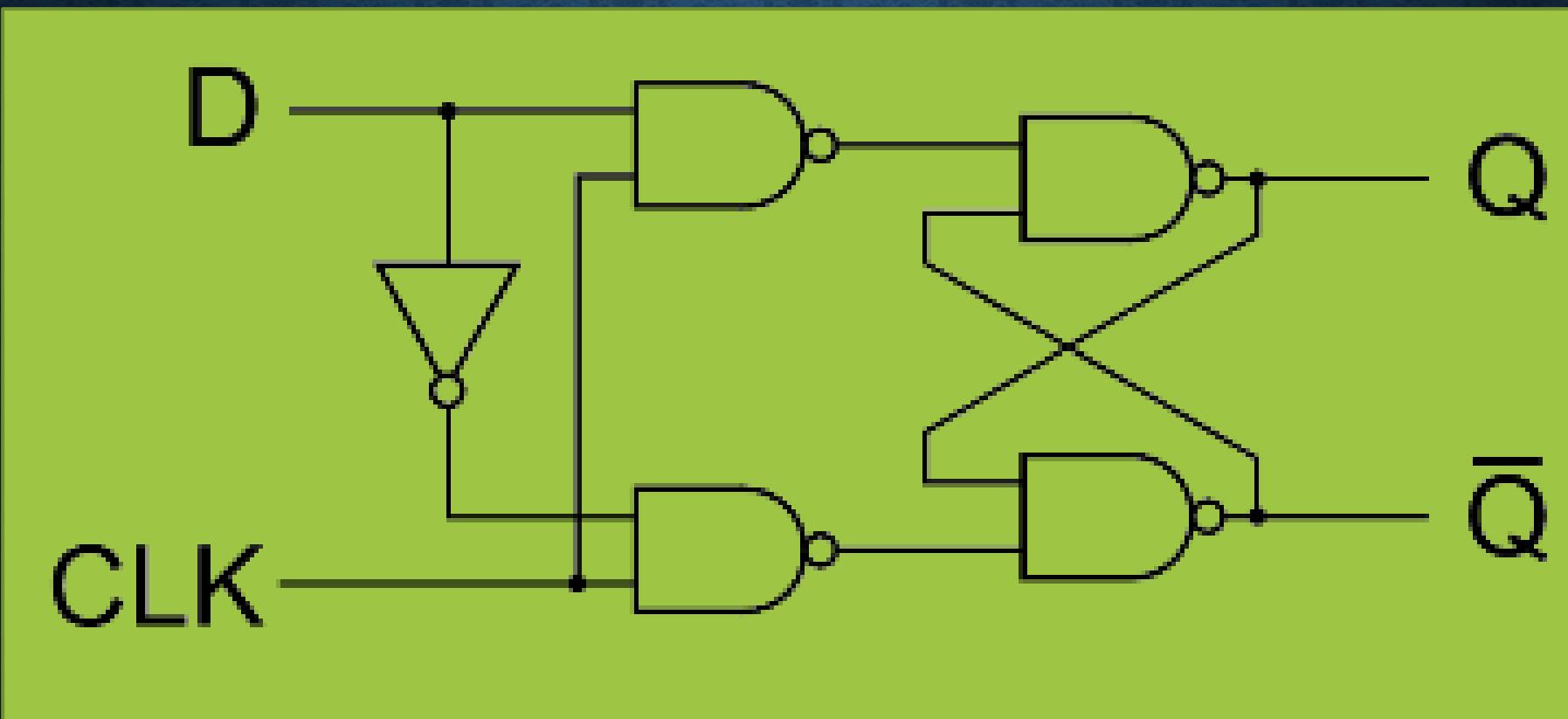
Q	S	R	Q_{t+1}	
0	0	0	0	Memory
0	0	1	0	RESET
0	1	0	1	SET
0	1	1	-	Indeterminate
1	0	0	1	Memory
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	-	Indeterminate

Characteristic Table

Disadvantage of R-S Flip Flop

* We need two control signals to store a binary data

D FLIP FLOP

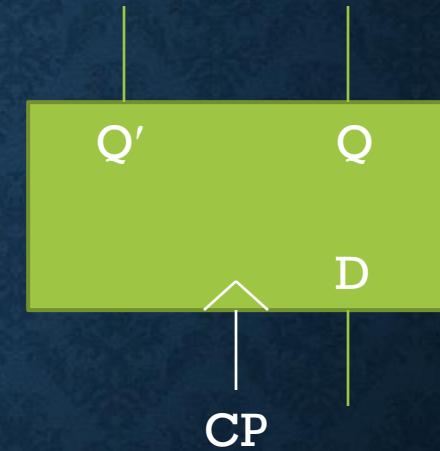


D FLIP FLOP

- D flip flop receives the designation from its ability to transfer “data” into a flipflop.
- It is basically an R-S Flip flop with an inverter in the R input.
- Also known as Gated D latch.

D FLIP FLOP

Q	D	Q_{t+1}	
0	0	0	Memory
0	1	1	Toggle
1	0	0	Memory
1	1	1	Toggle



Characteristic Equation

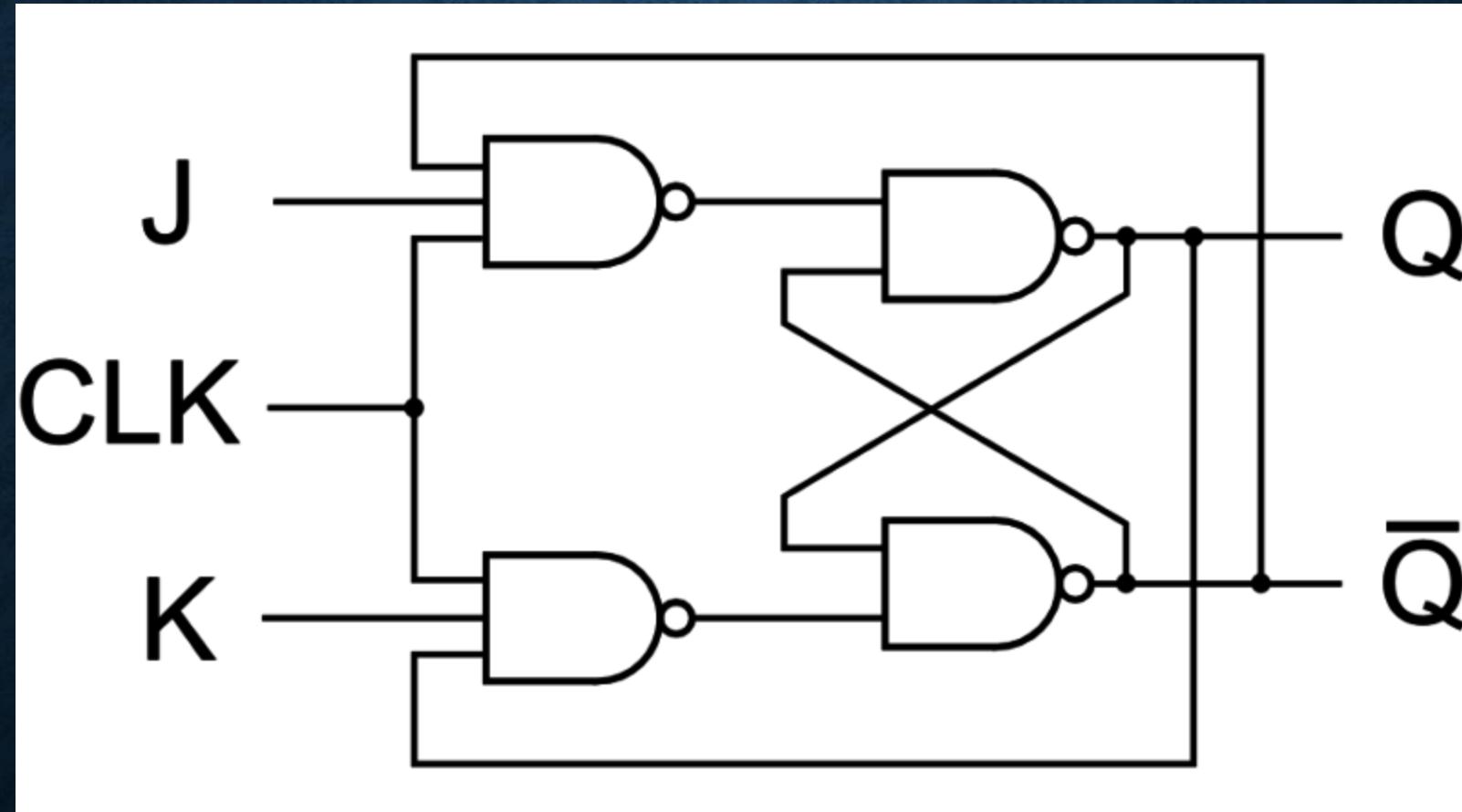
$$Q(t+1) = D$$

Logic Symbol
(Edge Triggered)

J-K FLIP FLOP

- A refinement of R-S Flip flop.
- The INDETERMINATE state of the R-S type is defined in the J-K type.
- Inputs J & K behave like i/ps S & R
 - J for SET, S and K for RESET, R.
- When $J=1$ & $K=1$, then the flip flop switches to its complement state whenever the clock signal is in HIGH state.

J-K FLIP FLOP



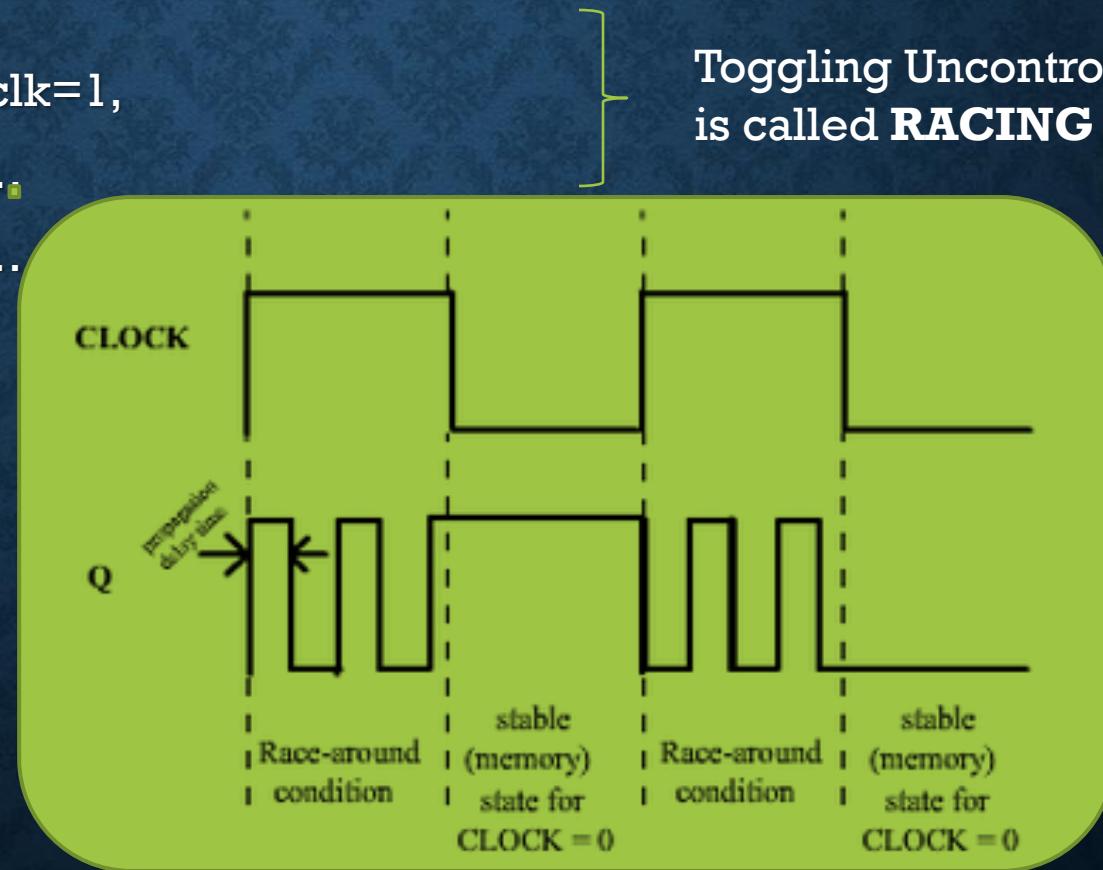
J-K FLIP FLOP

- Racing
 - When J=1 & K=1 and when clk=1,

$$Q(t+1) = 0, 1, 0, 1, 0 \dots$$

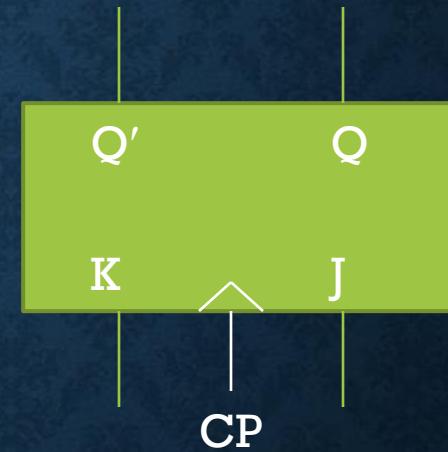
$$\overline{Q(t+1)} = 1, 0, 1, 0, 1 \dots$$

Toggling Uncontrollably
is called **RACING**



J-K FLIP FLOP

Q	J	K	Q_{t+1}	
0	0	0	0	Memory
0	0	1	0	RESET
0	1	0	1	SET
0	1	1	1	Toggle
1	0	0	1	Memory
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	0	Toggle



Logic Symbol
(Edge Triggered)

Characteristic Equation

$$Q(t+1) = JQ' + K'Q$$

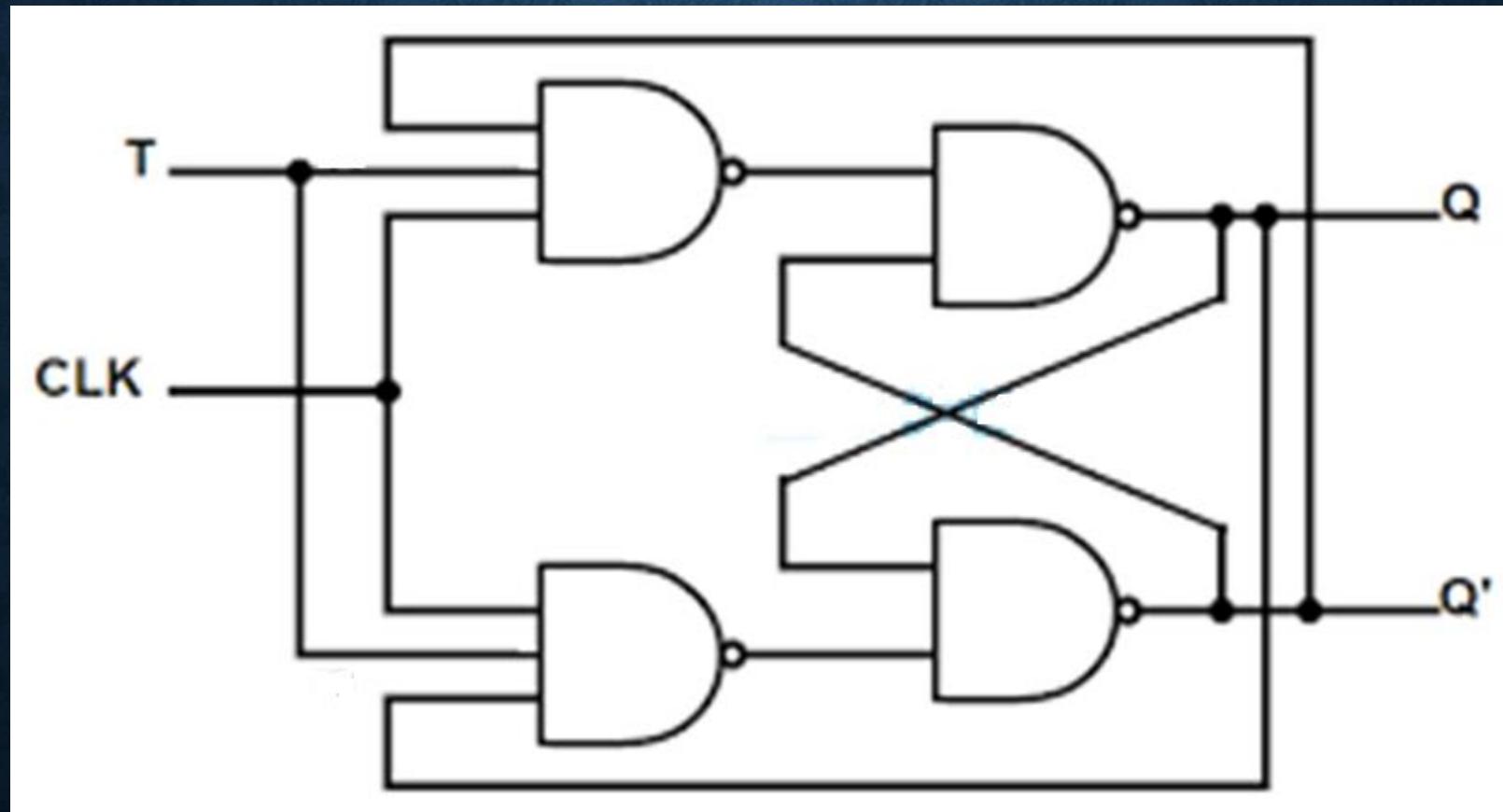
RACING/ RACE AROUND CONDITION

- Which o/p becomes 1/0 first depends on the difference in the propagation delay.
 - $Q(t+1)$ becomes 1/0 first if the gates correspond to it have less propagation delay than the gates correspond to $Q(t+1)$.
- Race Around Condition can be avoided if
 - Clock Period < Propagation delay of the flip flop
 - But it is impractical
 - Flip flop is made to toggle only once in a clock period
 - It is practically possible.

RACE AROUND CONDITION AND SOLUTION

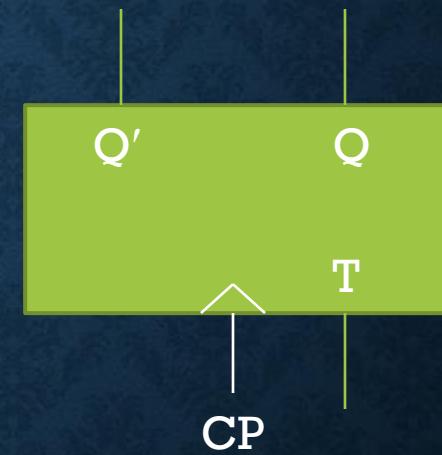
- The o/p of a J-K Flip flop is **uncertain** when **J** and **K** are **HIGH** and a clock signal is given. This situation is called **Race Around Condition**
- Race Around Condition can be solved using
 - **Master Slave J-K Flip flop**
 - **Edge Triggered construction of J-K Flip flop**

T FLIP FLOP



T FLIP FLOP

Q	T	Q_{t+1}	
0	0	0	Memory
0	1	1	Toggle
1	0	1	Memory
1	1	0	Toggle



Characteristic Equation

$$Q(t+1) = TQ' + T'Q$$

Logic Symbol
(Edge Triggered)

TRIGGERING OF FLIP FLOPS

- The process of applying the control signal to change the state of the flip flop is called **Triggering**.
- In Asynchronous flip flops(latches), the state of a flip flop is switched by a momentary change in the input signal. This momentary change is called a **Trigger**.
- The transition it causes is said to trigger the flip flop.
- Asynchronous flip flops require an input trigger defined by a change of signal level.
- In Asynchronous flip flops, if an unwanted signal comes to the i/ps, then there is a chance of changing the i/ps and hence the o/ps.

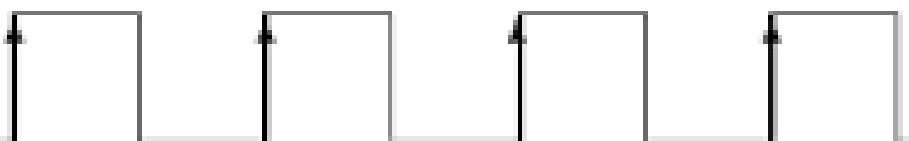
TRIGGERING OF FLIP FLOPS

- In Clocked flip flops, there is a triggering mechanism by clock pulses.
- There are two types of triggering
 - Level Triggering
 - The i/p signals affect the flip flop only when the clock is at logic-1 or logic 0.
 - Edge Triggering
 - The i/p signals affect the flip flop only if they are present at the rising edge or falling edge of the clock pulse.

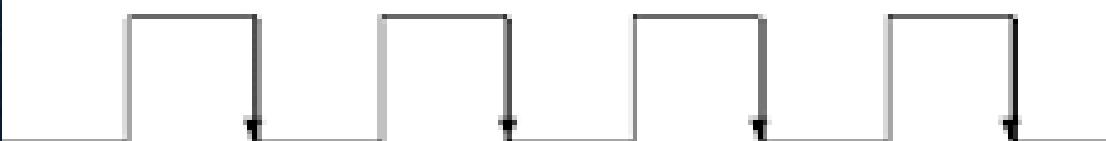
TRIGGERING OF FLIP FLOPS



(a) Level trigger.



(b) Positive-edge trigger.

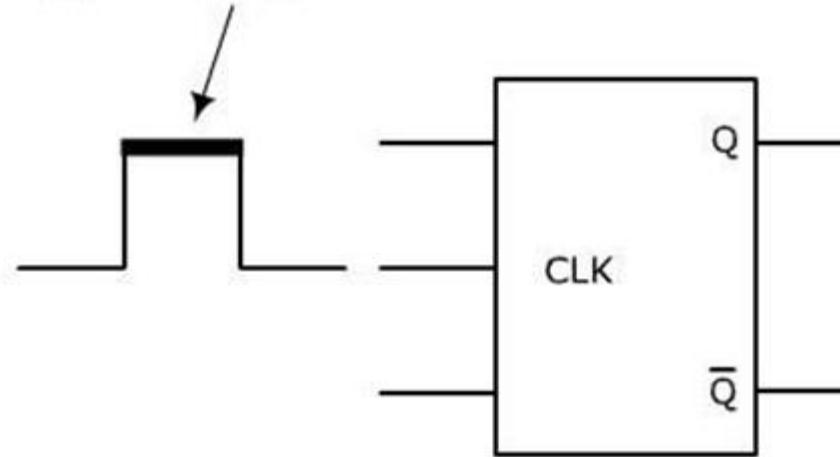


(c) Negative-edge trigger.

Time —

TRIGGERING OF FLIP FLOPS

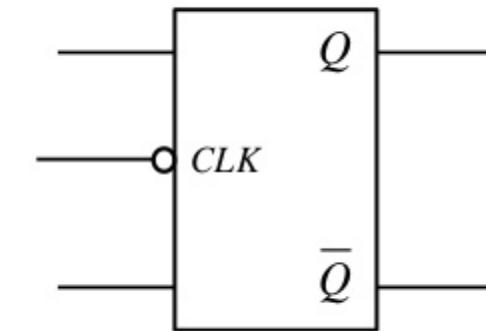
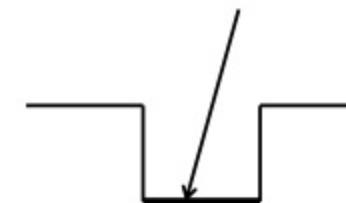
Triggers on high clock level



High Level Triggering

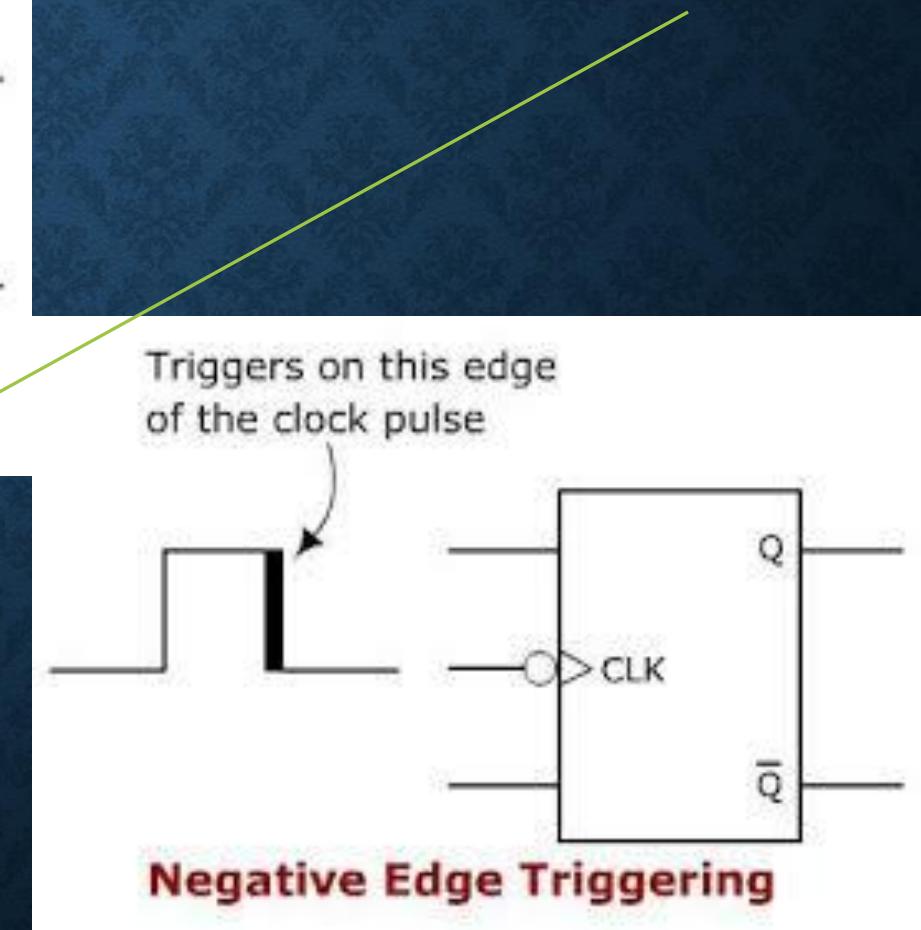
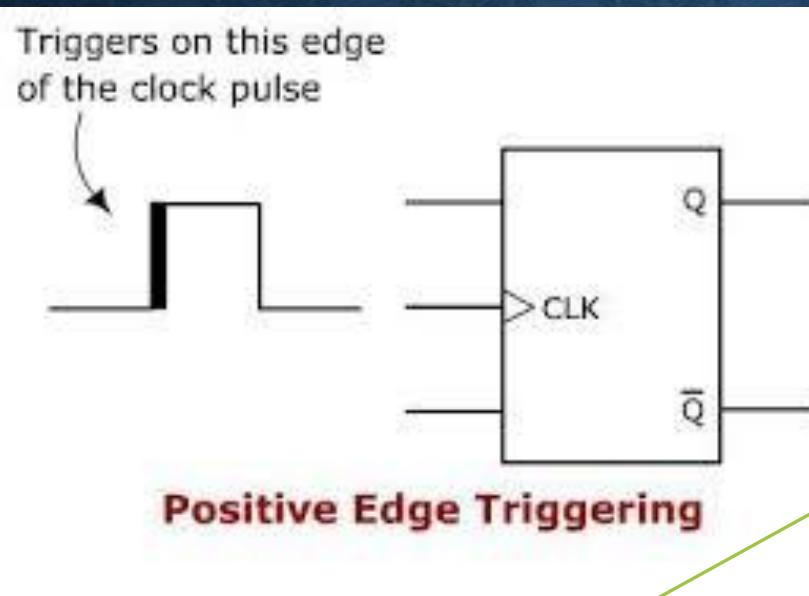
Low Level Triggering

Triggers on Low clock level



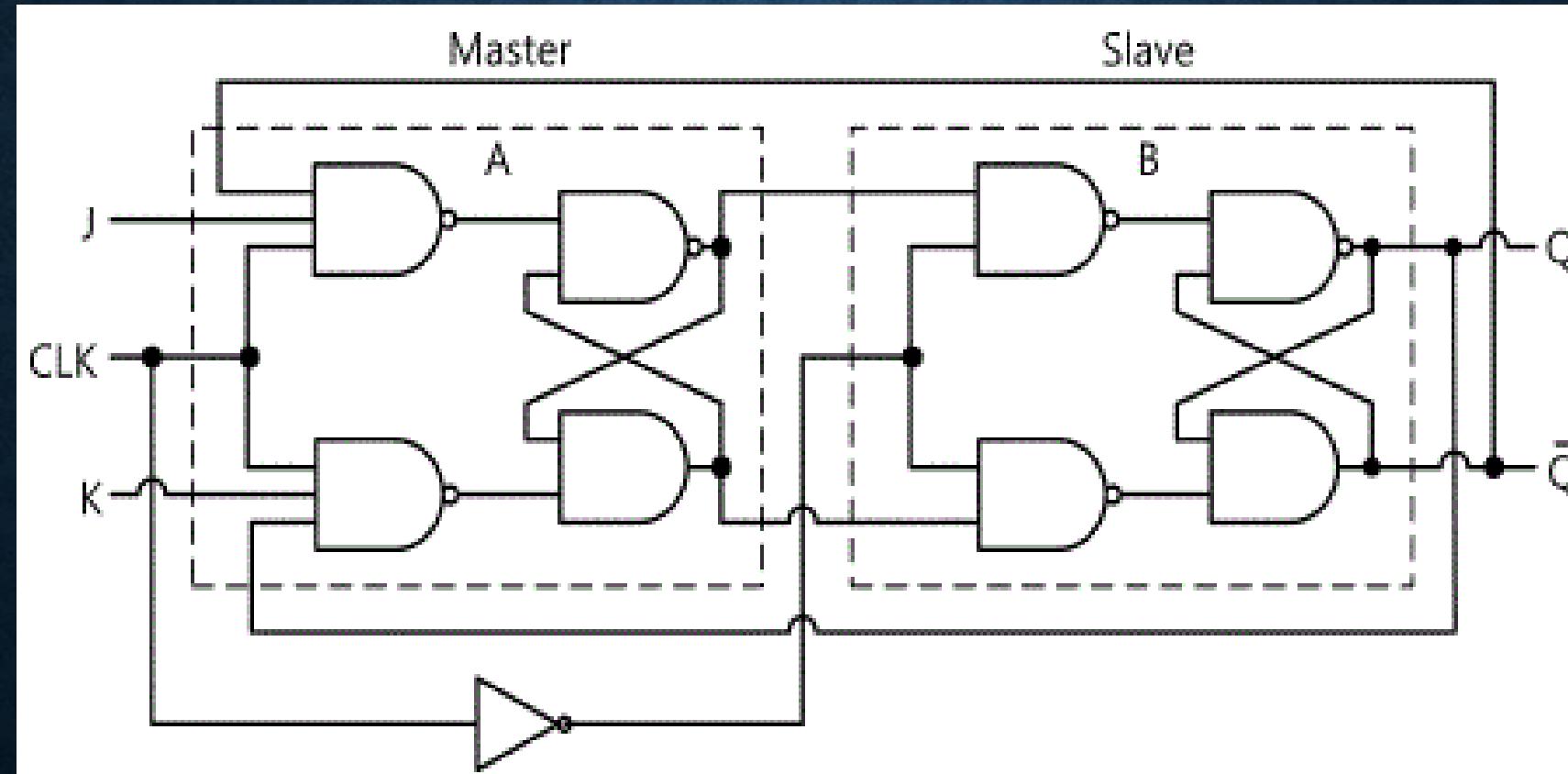
Symbol

TRIGGERING OF FLIP FLOPS



Edge Triggering is also known as
Dynamic Triggering

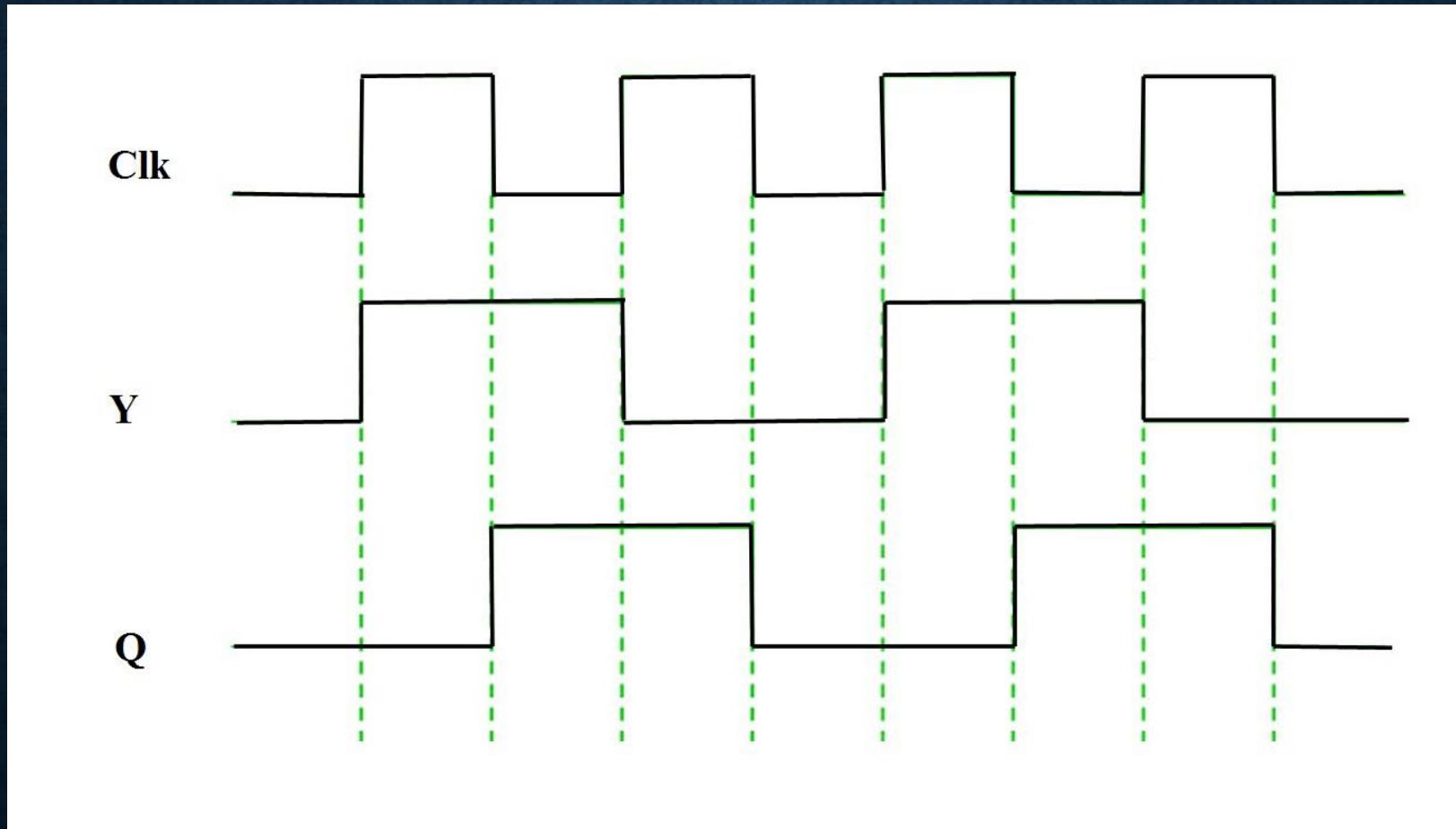
MASTER SLAVE J-K FLIP FLOP



MASTER SLAVE JK FLIP FLOP

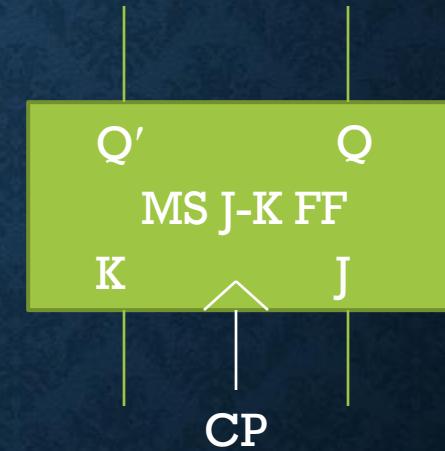
- Constructed from two separate flip flops
 - One is Master and the other is Slave.
- When $\text{clk}=1$,
 - the information at the external J & K i/p/s is transmitted to the master flip flop and
 - the slave flip flop is isolated from the master flip flop
- When $\text{clk}=0$,
 - The master flip flop is isolated, which prevents the external i/p/s from affecting it and
 - the slave flip flop then goes to the same state as the master flip flop

MASTER SLAVE J-K FLIP FLOP



MASTER SLAVE J-K FLIP FLOP

CL K	J	K	Q_{t+1}	
0	X	X	Q _t	Memory
1	0	0	Q _t	Memory
1	0	1	0	RESET
1	1	0	1	SET
1	1	1	Q _t	Toggle



Characteristic Equation

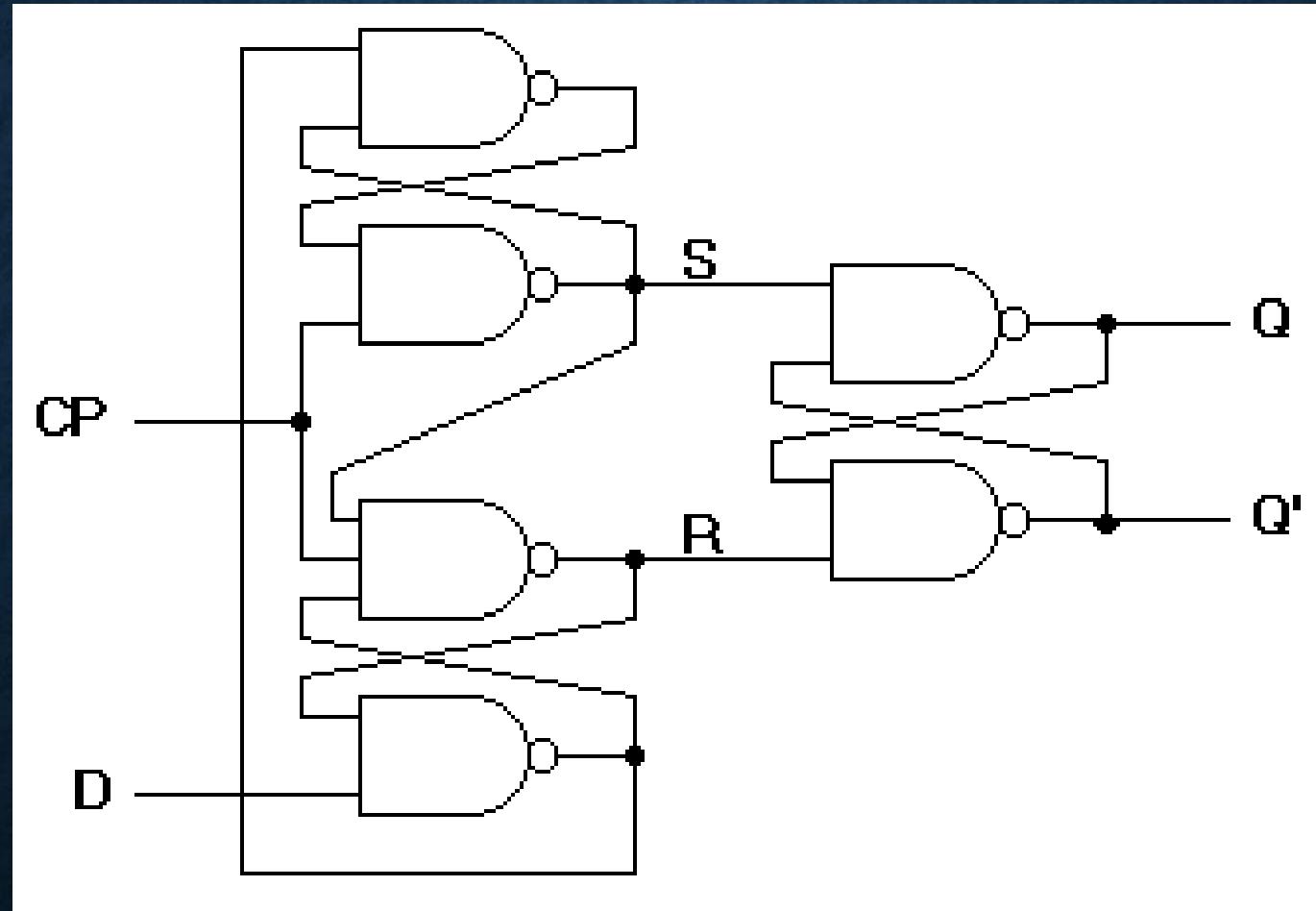
$$Q(t+1) = JQ' + K'Q$$

Logic Symbol
(Edge Triggered)

DISADVANTAGES OF MS J-K FF

- Two flip flops are needed.
- Slower due to two flip flop's delay.

EDGE TRIGGERED D FLIP FLOP



EDGE TRIGGERED D FLIP FLOP

- Consists of three basic latches.
 - NAND 1 & 2
 - NAND 3 & 4
 - NAND 5 & 6
- When $\text{clk}=0$, Q & Q' remains unchanged since $S=1$ & $R=1$ irrespective of the value of D .

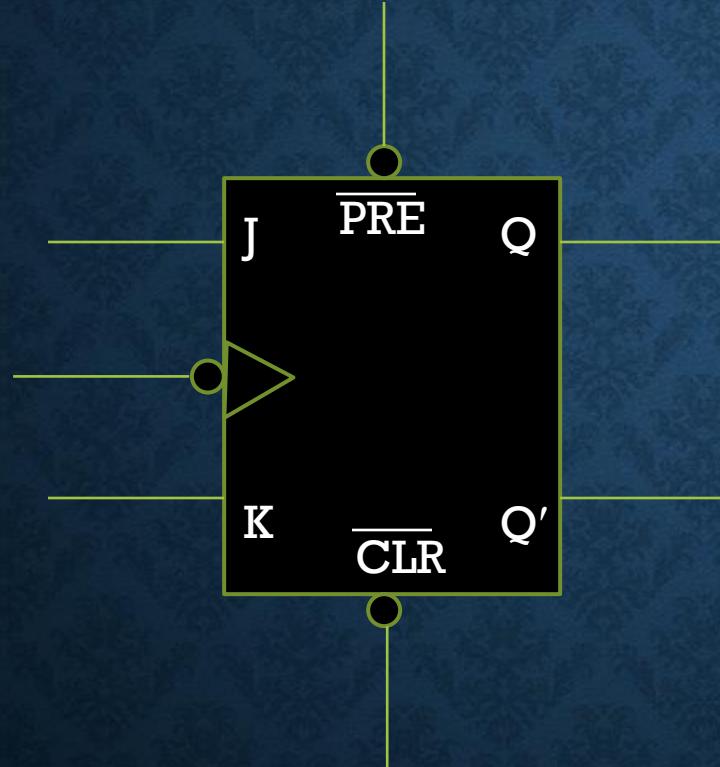
EDGE TRIGGERED D FLIP FLOP

- Setup time
 - Definite time in which the D i/p must be maintained at a constant value prior to the application of the pulse.
 - Setup time equals the propagation delay through the gates 4 & 1.
- Hold time
 - Definite time in which the D i/p must be maintained at a constant value after the application of the pulse.
 - Hold time equals the propagation delay through the gate 3.

ASYNCHRONOUS INPUTS (DIRECT INPUTS)

- Asynchronous inputs affect the o/p of the flip flop independently of the synchronous inputs and the clock.
- They are used to SET or RESET the flip flop at any time.
- Two Asynchronous inputs
 - PRESET(direct SET or DC SET)
 - This i/p will SET the flip flop.
 - CLEAR(direct RESET or DC CLEAR)
 - This i/p will RESET the flip flop.

PRE AND CLR



$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	FF Response
0	0	Not Used
0	1	$Q = 1$
1	0	$Q = 0$
1	1	Clocked Operation

ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS

- The behavior of a clocked sequential circuit is determined from the inputs, the outputs, and the state of its flip-flops.
- The outputs and the next state are both a function of the inputs and the present state.
- **The analysis of a sequential circuit consists of obtaining a table or a diagram for the time sequence of inputs, outputs, and internal states.**

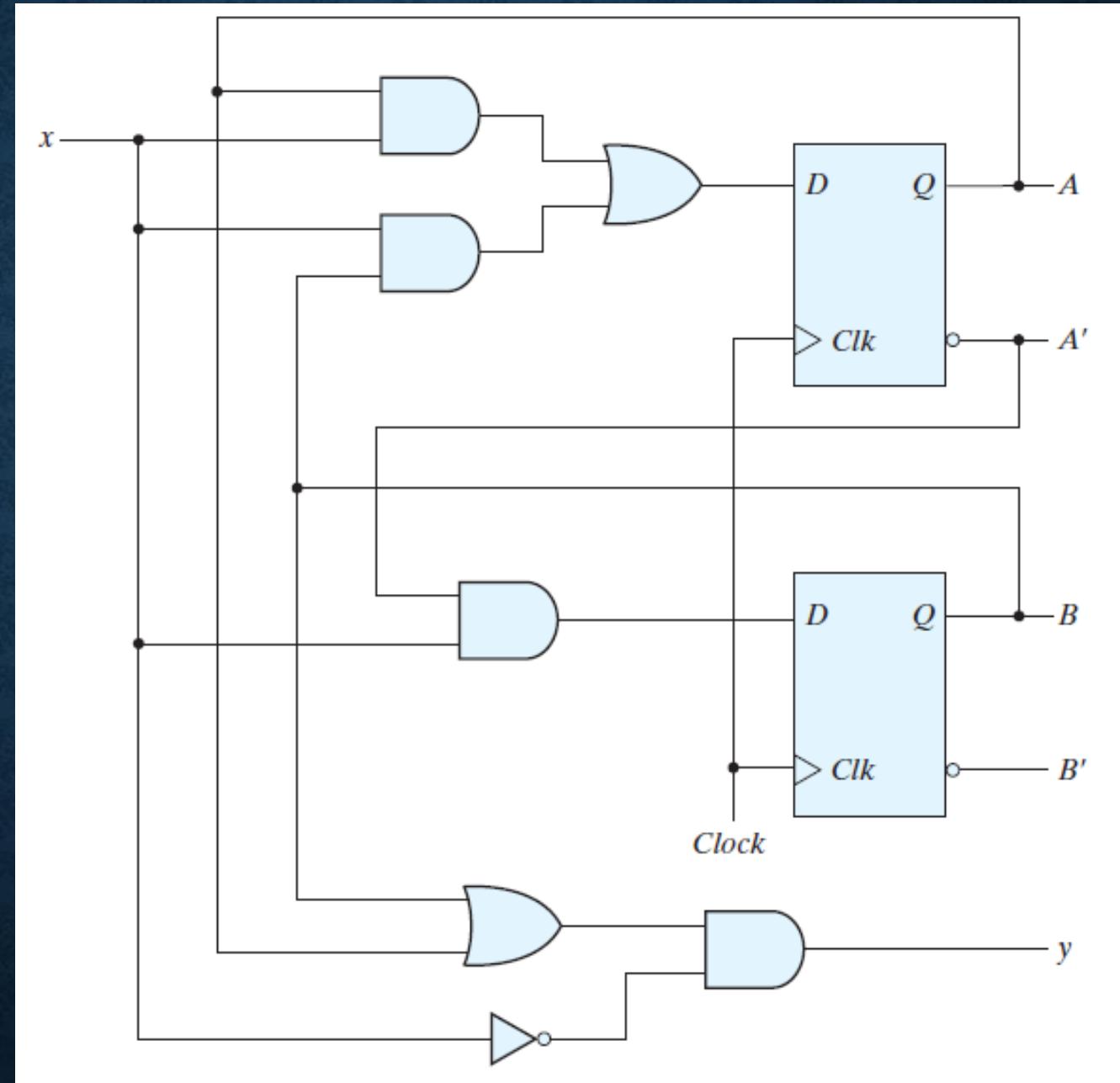
ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS

- The behavior of a clocked sequential circuit is determined from the inputs, the outputs, and the state of its flip-flops.
- The outputs and the next state are both a function of the inputs and the present state.
- The analysis of a sequential circuit starts from a circuit diagram and culminate in a state table or diagram.

STATE EQUATIONS

- The behavior of a clocked sequential circuit can be described algebraically by means of state equations.
- A state equation (also called a transition equation) specifies the next state as a function of the present state and inputs.

EXAMPLE OF A SEQUENTIAL CIRCUIT



STATE TABLE

- The time sequence of inputs, outputs, and flip-flop states can be enumerated in a state table (sometimes called a transition table).
- The table consists of four sections labeled present state, input, next state, and output.

STATE DIAGRAM

- The information available in a state table can be represented graphically in the form of a state diagram.
- In this type of diagram, a state is represented by a circle, and the (clock-triggered) transitions between states are indicated by directed lines connecting the circles.
- Each line originates at a present state and terminates at a next state, depending on the input applied when the circuit is in the present state.

FLIP FLOP INPUT FUNCTIONS

- The logic diagram of a sequential circuit consists of flip-flops and gates.
- The interconnections among the gates form a combinational circuit and may be specified algebraically with Boolean expressions.
- The part of the combinational circuit that generates external outputs is described algebraically by a set of Boolean functions called **output equations**.
- The part of the circuit that generates the inputs to flip-flops is described algebraically by a set of Boolean functions called **flip-flop input equations** (or, sometimes, **excitation equations**).

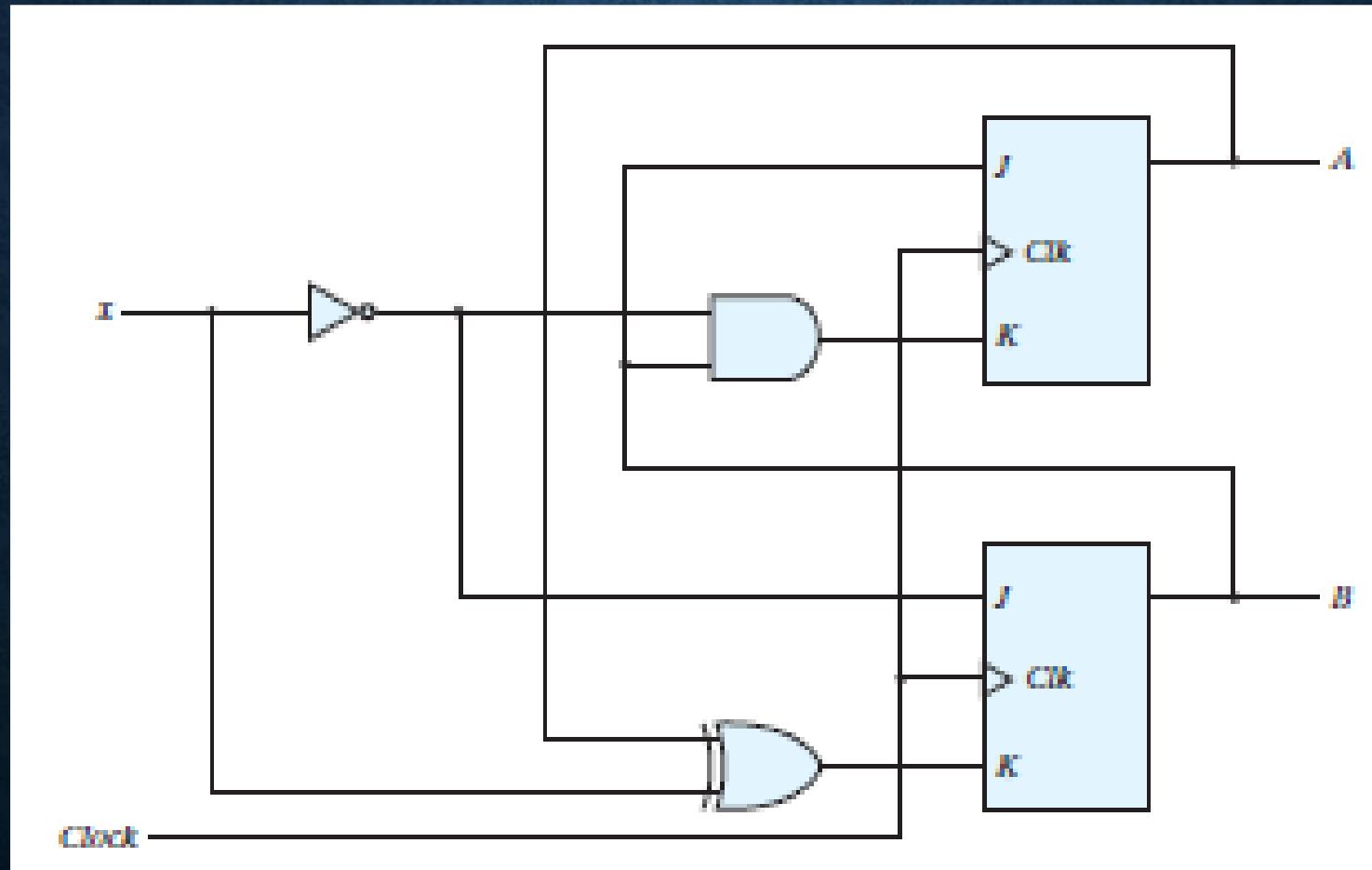
ANALYSIS OF SEQUENTIAL CIRCUITS

- When a flip-flop other than the D type is used, such as JK or T, it is necessary to refer to the corresponding characteristic table or characteristic equation to obtain the next-state values.
- The next-state values of a sequential circuit that uses JK- or T-type flip-flops can be derived as follows:
 - Determine the flip-flop input equations in terms of the present state and input variables.
 - List the binary values of each input equation.
 - Use the corresponding flip-flop characteristic table to determine the next-state values in the state table.

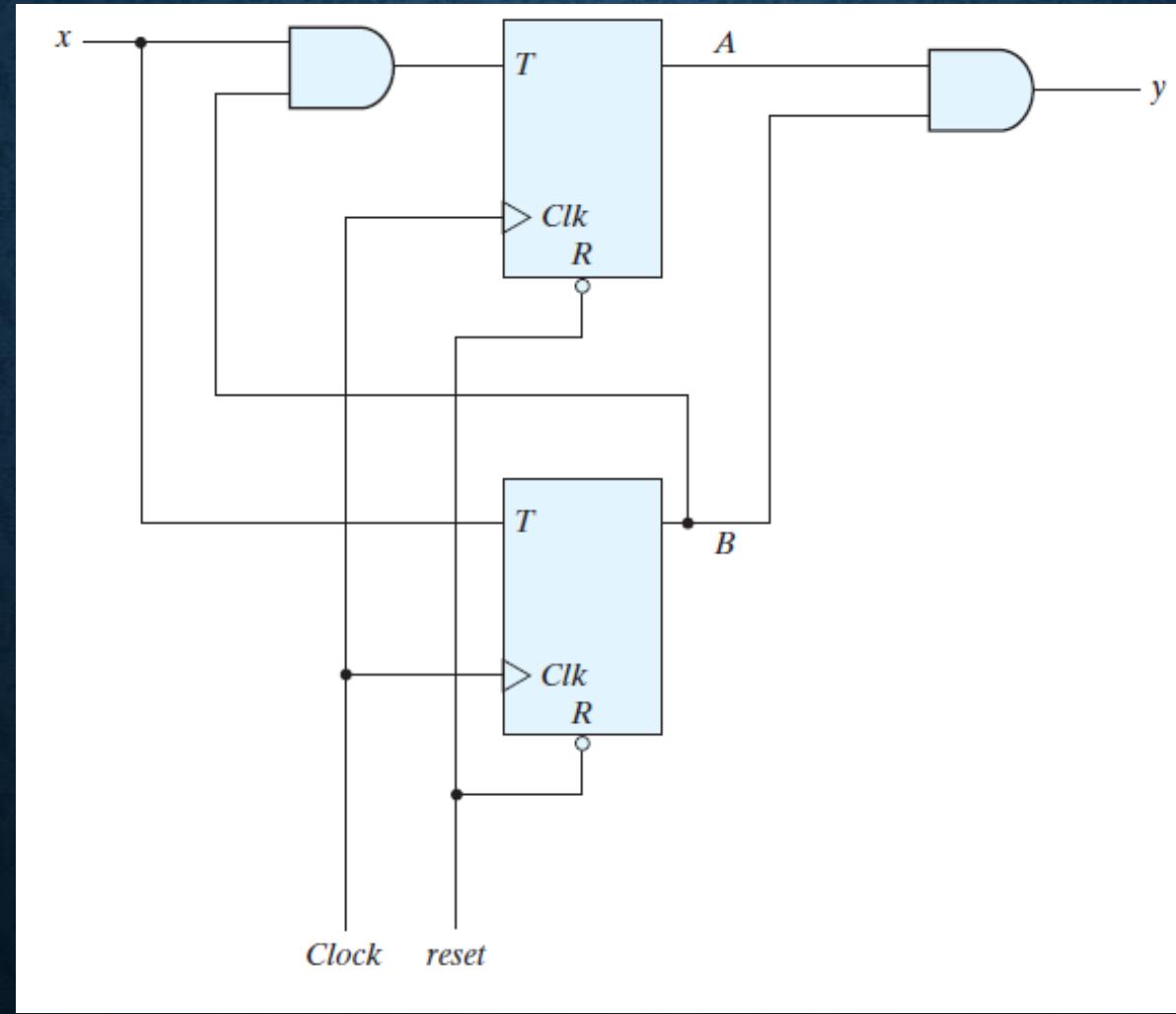
ANALYSIS OF SEQUENTIAL CIRCUITS

- The next-state values of a sequential circuit that uses JK- or T-type flip-flops can also be obtained by evaluating the state equations from the characteristic equation. This is done by using the following procedure:
 - Determine the flip-flop input equations in terms of the present state and input variables.
 - Substitute the input equations into the flip-flop characteristic equation to obtain the state equations.
 - Use the corresponding state equations to determine the next-state values in the state table.

ANALYSIS WITH JK FLIP FLOP



ANALYSIS WITH T FLIP FLOP

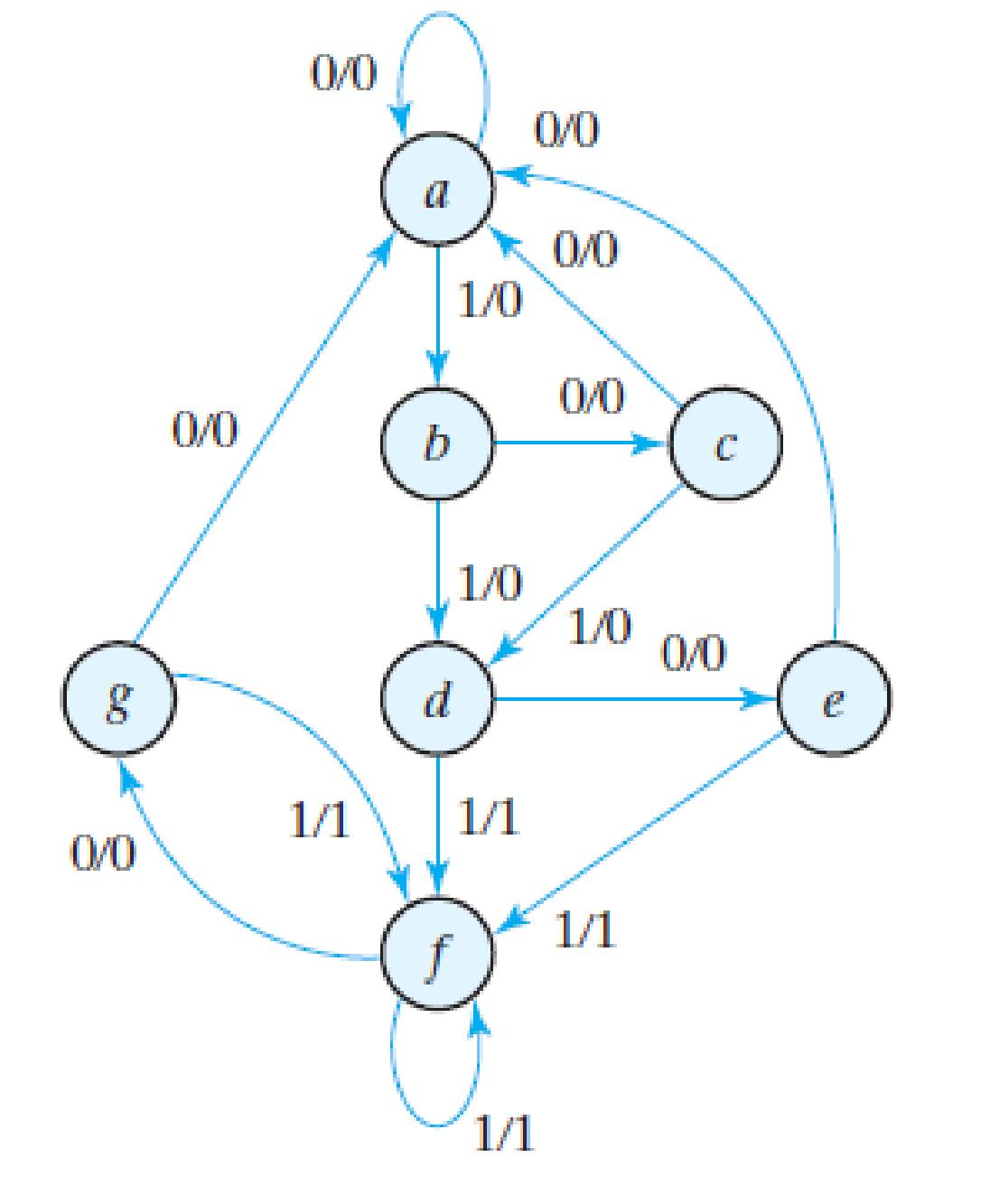


STATE REDUCTION AND ASSIGNMENT

- Cost reductions -> by reduction in the number of flip flops and the number of gates.
- Reduction in the number of flip flops in a sequential circuit referred to as the **State reduction problem**.
- **State-reduction algorithms** are concerned with procedures for reducing the number of states in a state table, while keeping the external input–output requirements unchanged.
- Unpredictable effect: sometimes the equivalent circuit may require more combinational circuits.

EXAMPLE

INPUT SEQUENCE:
01010110100



EQUIVALENT CIRCUITS

- If identical input sequences are applied to the two circuits and identical outputs occur for all input sequences, then the two circuits are said to be equivalent; and one may be replaced by the other.

EQUIVALENT STATES

- Two states are said to be equivalent if, for each member of the set of inputs, they give exactly the same output and send the circuit either to the same state or to an equivalent state.

STATE ASSIGNMENT

Three Possible Binary State Assignments

State	Assignment 1, Binary	Assignment 2, Gray Code	Assignment 3, One-Hot
a	000	000	00001
b	001	001	00010
c	010	011	00100
d	011	010	01000
e	100	110	10000

Reduced State Table with Binary Assignment 1

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
000	000	001	0	0
001	010	011	0	0
010	000	011	0	0
011	100	011	0	1
100	000	011	0	1

DESIGN PROCEDURE

- The design of a clocked sequential circuit starts from a set of specifications and culminates in a logic diagram or a list of Boolean functions from which the logic diagram can be obtained.

DESIGN PROCEDURE

- The procedure for designing synchronous sequential circuits can be summarized by a list of recommended steps:
 - From the word description and specifications of the desired operation, derive a state diagram for the circuit.
 - Reduce the number of states if necessary.
 - Assign binary values to the states.
 - Obtain the binary-coded state table.
 - Determine the number of flip flops needed and assign a letter to each.
 - Choose the type of flip-flops to be used.
 - Derive the circuit excitation and output tables
 - Derive the simplified flip-flop input equations and output equations.
 - Draw the logic diagram.

REFERENCES

- M. Morris Mano - Digital Logic and Computer Design

THANK YOU

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GECPKD