1. Design a accumulator.

* An accumulator is a register for short term, intermediate storage of arithmetic and logic data in a computers CPU.

* The term "accumulator" is used in reference to contemporary CPU's, having been replaced around the turn of the millennium by the term "register"

Circuits associated with AC.

Register A

Combinational circuit ← Control variables

B Data inputs
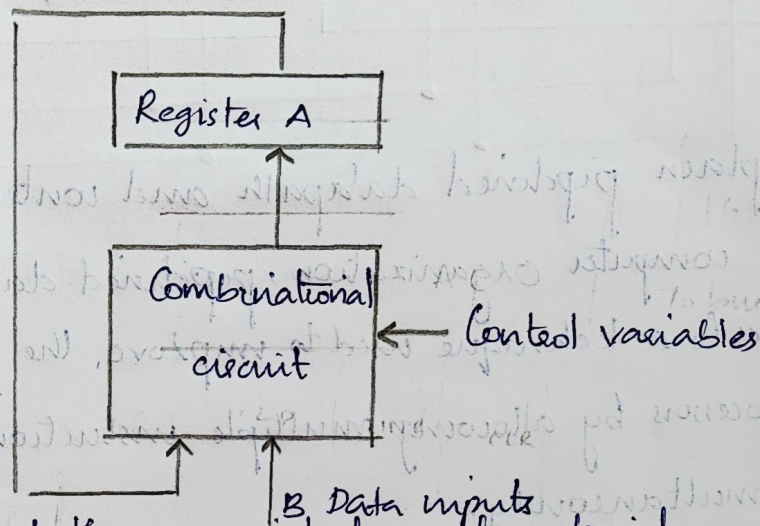
* A register and the associated combinational circuit constitutes a sequential circuit. The combinational circuit replaces the ALU but cannot be seperated from the register, since it is only the combinational-circuit part of a sequential circuit. The A register is referred to as the accumulator register and is sometimes denoted by the symbol AC. Here, accumulator defers to both the A Register and its associated combinational circuit.

* The external inputs to the accumulator are the data inputs from B and the control variables that determine

the micro operations for the register. The next stage of register A is a function of its present state and of the external inputs.
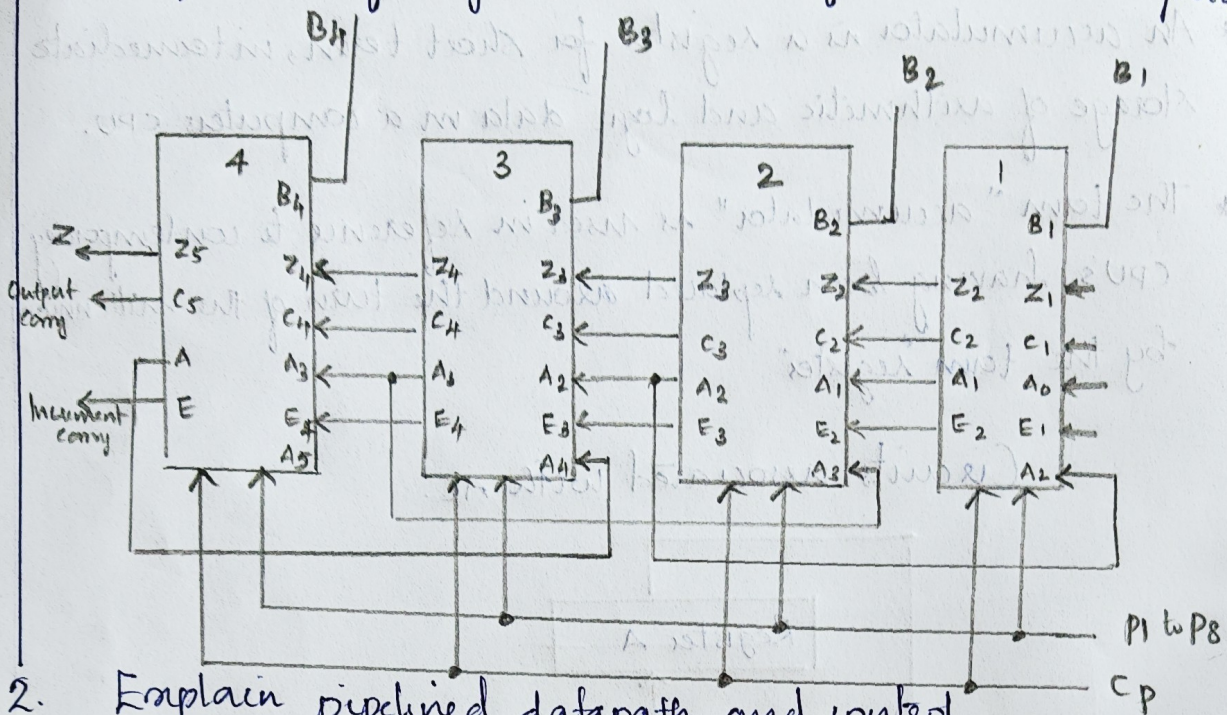
2. Explain pipelined datapath and control

ans: In computer organization, pipelined datapath and control refer to a technique used to improve the performance of processors by allowing multiple instructions to be executed simultaneously.

The pipelined datapath consists of a series of stages, each of which performs a specific operation on the data. For example, the stages might include instruction fetch, ex instruction decode, register fetch, execute, and write back. Each stage operates on a different part of the instruction, allowing multiple instructions to be processed simultaneously.

The control unit manages the flow of data through the pipeline, ensuring that each stage is executed in the correct order and that all dependencies between instructions are

The control logic is responsible for managing the flow of data through the pipeline and ensuring that each stage operates correctly. It must also handle issues such as data hazards, which can occur when an instruction requires data that is still being processed in an earlier stage of the pipeline. To prevent data hazards, the control logic may insert stall cycles, which temporarily halt the pipeline until the necessary data is available.

The control logic also manages the flow of instructions through the pipeline. It must ensure that instructions are fetched in the correct order, decoded and executed in the correct sequence, and that the results of each instruction are written back to memory in the proper location.

Overall, the pipelined datapath and control enable the efficient execution of multiple instructions simultaneously, which can result in improved performance and throughout in computer systems.