LIST OF FIGURES

EIOT OF FIGURES	
Figure 1: Block Diagram	3
Figure 2: FPGA - ADC DAC Interface	5
Figure 3: Input Channels of ADC	6
Figure 4 : Anti- Aliasing Filter	
Figure 5: Reconstruction Filter	
Figure 6: Stereo Jack	
Figure 7: Frequency Range Set	
Figure 8: FPGA - RS232 Interface	
Figure 9: Seven Segment Display	
Figure 10: Stepper Motor Interface	
Figure 11: Relay Interface	
Figure 12: DC Motor Interface	
Figure 13: LCD Interface to SPARTAN-3 FPGA	
Figure 14: ASCII Code for 5 x 7 LCD display	
Figure 15: positional Details of On Board Connectors	
Figure 16: JTAG Mode Selection	
Figure 17: JTAG Mode Selection	
rigure 17. JTAG Conffector Details	50
LIST OF TABLES	
Table 1: Analog Inputs	-
Table 2: ADC Interface to SPARTAN 3 FPGA	
Table 3: Control Inputs to ADC	
Table 4: Analog Outputs	
Table 5: DAC Interface to FPGA	
Table 6: Potentiometer adjustments	
Table 7: Jumper Setting for ADC Input	
Table 8: Jumper setting for Anti Aliasing Filter	
Table 9: Jumper Setting for Analog Output	
Table 10: Jumper Setting for Reconstruction Filter	
Table 11: RS232 Interface to SPARTAN -3 FPGA	
Table 12: Seven Segment Display Interface to SPARTAN-3 FPGA	
Table 13: Stepper motor Connector: J14	
Table 14: Stepper Motor and Relay Interface to FPGA	
Table 15: DC motor Connector: J14	
Table 16: Data Line Interface to SPARTAN-3 FPGA	
Table 17: Control Line Interface to SPARTAN-3 FPGA	
Table 18: DIP switch Interface to SPARTAN-3 FPGA	
Table 19: KEY switch Interface to SPARTAN-3 FPGA	
Table 20: LED Interface to SPARTAN-3 FPGA	
Table 21: IO Clock-Reset Interface to FPGA	27
Table 22: Mode Selection Jumper Settings	28
Table 23: Mode Selection Table	
Table 24: Configuration Selection	29
Table 25: Power Supply Details	
• • •	

TABLE OF CONTENTS

PREFACE	
About This Manual	
Manual Contents	
CHAPTER 1	
Introduction	
Features	2
CHAPTER 2	_
ADC - DAC Interface	
2.2 Analog Input Connector:	
2.3 ANALOG OUTPUT	
2.4 Analog Output Connector:	
2.6 Stereo Jack Connector:	
2.7 Function Generator	
2.8 Potentiometer Adjustments	
2.9 Jumper Settings of ADC- DAC Interface	10
OHARTER O	40
CHAPTER 3	
Serial Interface	
3.1 K3- 232 IIIleHace	12
CHAPTER 4	13
Seven Segment LED Display	
Octor ocginent LLD Display	
CHAPTER 5	15
Stepper Motor And Relay Interface	
5.1 Stepper Motor Interface	
5.2 Relay Interface	15
CHAPTER 6	
DC Motor	
6.1 DC Motor Interface	
CHAPTER 7	18
LCD Interface	
7.1 Data Lines Connection	
7.2 Control Line Interface:	
7.3 ASCII CODE	
CHAPTER 8	
Switches And LEDs	
8.1 DIP Switches	
8.2 Key Switches	
8.3 LEDS	22
CHAPTER 9	24
Connector Details	
	24
CHAPTER 10	27
Clock and Reset Sources	

CHAPTER 11	28
SPARTAN-3 Configuration Details	
11.1 Boundary Scan mode:	28
11.2 Master Serial Mode	
11.3 Jumper Setting	
13.4 JTAG Header:	
CHAPTER 12	31
Power Supplies	
12.1 Voltage Regulators	
APPENDIX A	32
Consolidated UCF For The Complete Board	
APPENDIX B	37
Operating Instructions To Start A New Design	
B.1 Starting The ISE Software:	
B.2 Design Flow	
B.3 Design Description	
B.4 Truin Table of Hall adder:	
B.4 Truth Table of Half adder: B.5 VHDL Code for Half adder	
B.4 Truth Table of Half adder: B.5 VHDL Code for Half adder. B.6 Steps to implement the Half adder in the FPGA using Xilinx ISE(8.1i)	38
B.5 VHDL Code for Half adderB.6 Steps to implement the Half adder in the FPGA using Xilinx ISE(8.1i)	38 39
B.5 VHDL Code for Half adder	38 39