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EE371
February 9, 2025
Lab 3 Report

Section 1: Procedure

This lab asked to modify and implement and draw various lines from arbitrary points on a VGA display. This system used VGA output to display the animation, movement, and drawing of a line. I divided the assignment into the following tasks, based on the major components:

1. Drawing any arbitrary line
2. Move and Animate arbitrary lines

Task #1: Drawing any arbitrary lines

Task one we implemented Bresenham's line algorithm to be able to draw any line from arbitrary points on a VGA display. To do this I created a line_drawer module from the pseudo-code provided by the lab document which helped me format/understand how to implement this algorithm. I also added to the already given DE1_SoC module and kept the VGA_framebuffer module the same.

1. The first module is called "DE1_SoC" This is the top-level module that connects/instantiates the line_drawer and VGA_frambuffer modules. It also instantiates the draw color by making the draw color black if SW[9] is off and white if SW[9] is on. The reset is also instantiated to KEY[3] (since active low it's ~KEY[3]) so when KEY[3] is pressed it resets the board by coloring whatever arbitrary points are given to white.
2. The second module was the "line_drawer" module that dealt with each case of arbitrary points, whether it was gradual or steep as well as dealing with where the points start and end. This module also uses these arbitrary points and cycles through each point between the end and beginning by incrementing the x and y coordinates based on whether the line was steep, gradual, neg slop, pos slop, etc.
3. The "VGA_framebuffer" module is the last module and it is taken from the skeleton provided by the lab manual for lab 3. This is the driver module that connects the VGA display to show visible output to the user.

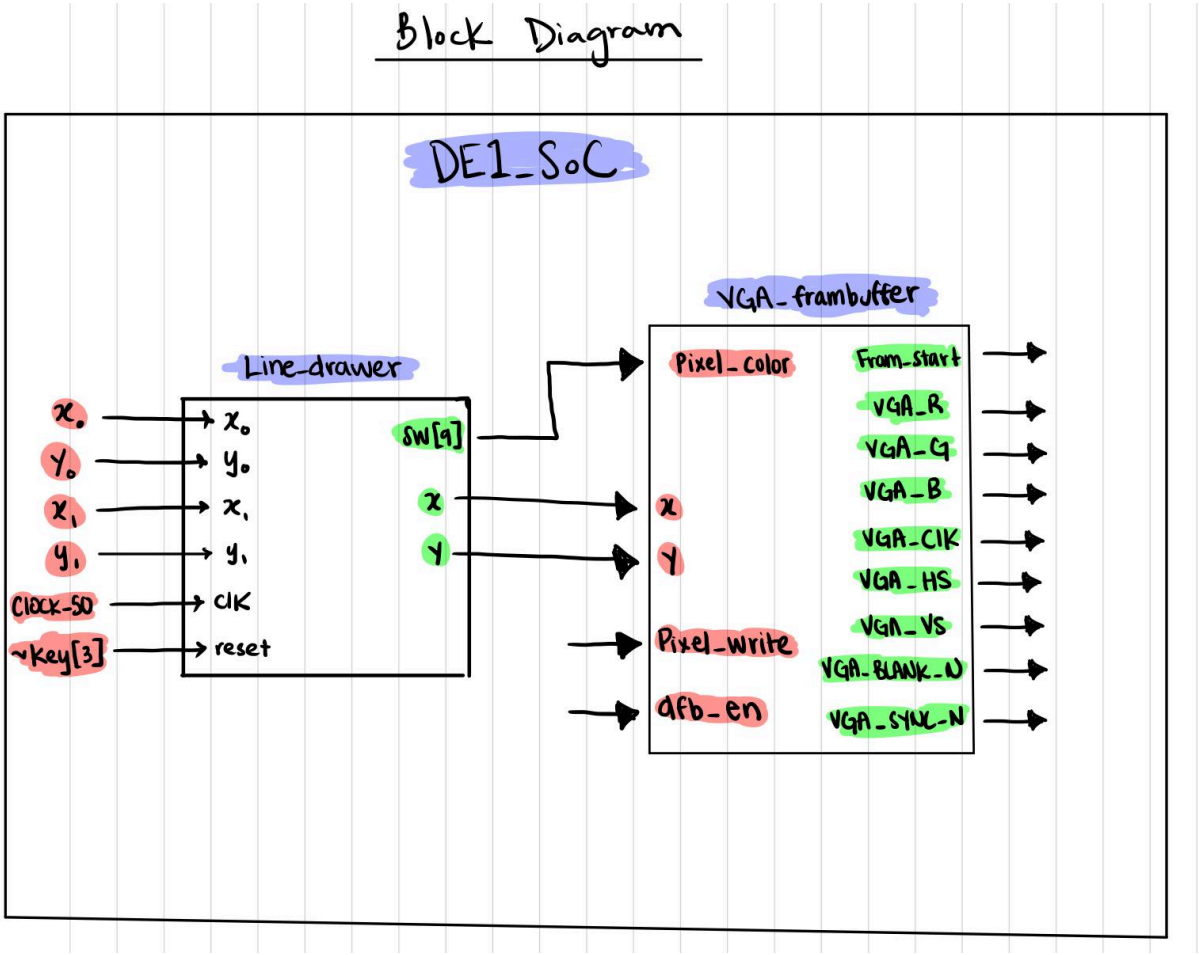

Figure 1: Block diagram of Task 1 - Draw Arbitary Lines

Task #2: Moving/Animating Arbitrary Lines

The second task was to create dual-port RAM by implementing an existing 32x4 RAM. We used 4 modules (3 modules in block diagram, as they were all initialized following this format on the 4th DE1_SoC module)

1. The “line_drawer” module stays the same where the module deals with each case of arbitrary points and cycles through each point between the end and beginning by incrementing the x and y coordinates based on whether the line was steep, gradual, neg slop, pos slop, etc.
2. The “VGP_framebuffer” module stays the same as the last task and it is taken from the skeleton provided by the lab manual for lab 3.
3. The “line_animation” module uses the x0, x1, y1, and y2 start and ending coordinates and increases their values periodically to show the line moving. This module uses a counter to slow down the time each variable is updated (and the line moves) so that the user can see the movement. It takes in the reset and clock signal and outputs 4 new x0, x1, y1, and y2 values.

4. The “DE1_SoC” module initlizations all of these modules and also creates an inProgress singal that serves as a signal that is true when a drawing is in progress so that it can’t be reset when the switch is on. It also uses a RAM to store the coordinates of the lines that are being animated and uses a state machine to go between each set of coordinates in a loop.
5. The “clear_display” module clears the display on two different occasions, it first clears the display after key3 is pressed or when SW9 turns off. It clears the display after a certain amount of time to show the animation recurring over and over again when key 3 is pressed.
6. The “button_press” module uses a FSM to make sure that any press of the button is captured and not overlooked incase it is pressed and finished pressing during the neg edge of a clock.

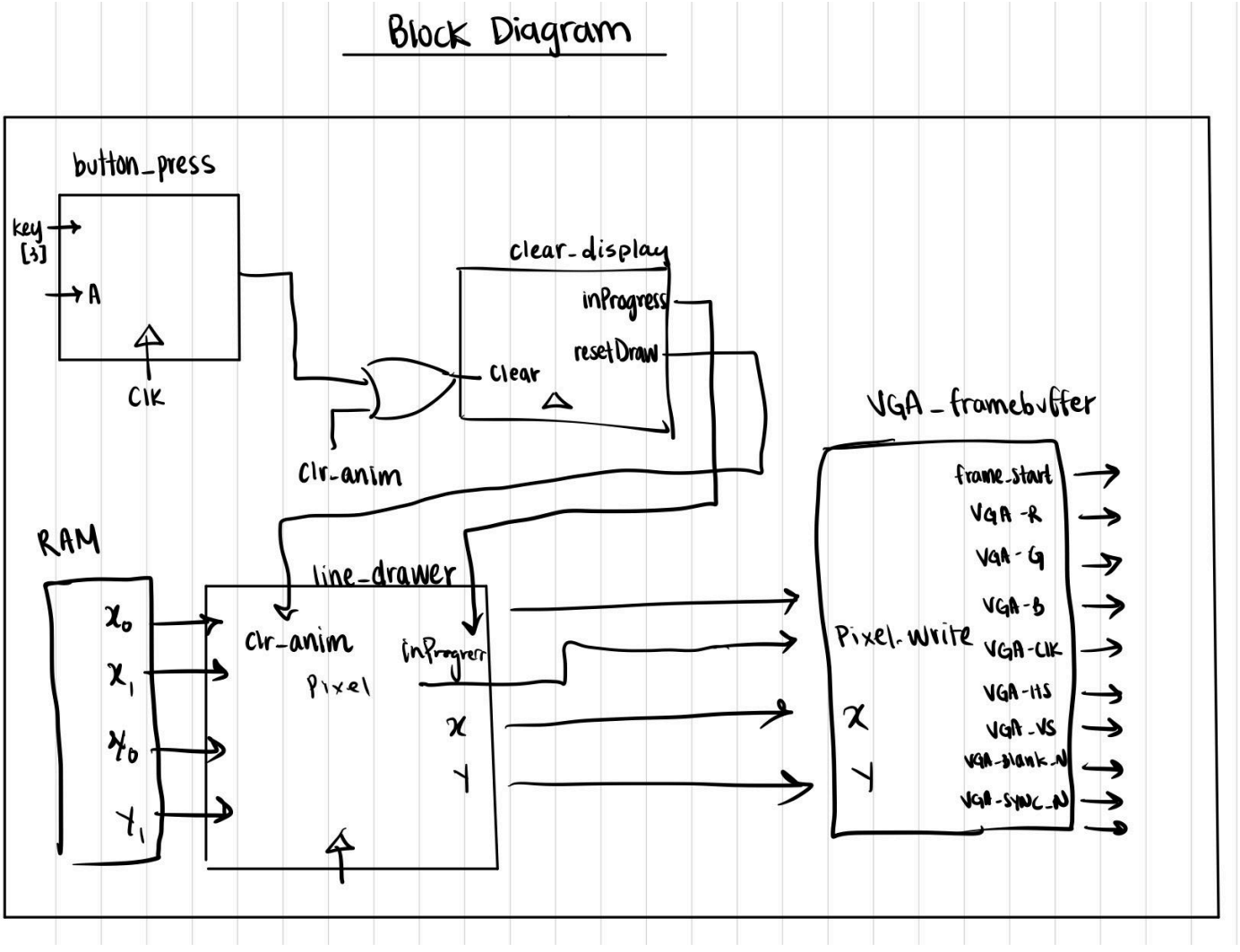

Figure 2: Block Diagram of Task 2 - Animation of Arbitrary Lines

Section 2: Results

Task #1: Drawing Arbitaray Lines

Each of the testbench simulations tested the following situations:

1. **Line_drawer_testbench**: This testbench simulates 7 different types of line drawings, each of which are described below with figures that go along with the description.

Simulation waveforms of line_drawer_testbench:

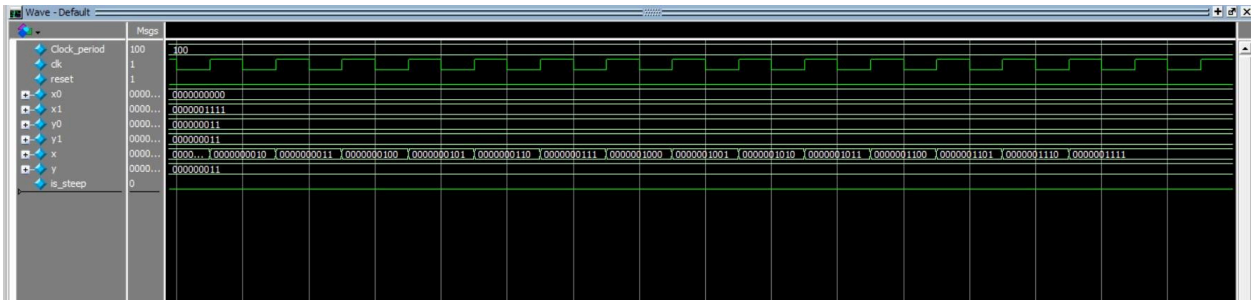

Figure 3.1: ModelSim waveform of Horizontal Line

Shows Situation where a coordinates for x0, x1, y0, y1 are given such that a horizontal line is drawn. As you can see the x coordinates increase by one but the y coordinates stay the same which shows how the horizontal line is being drawn.

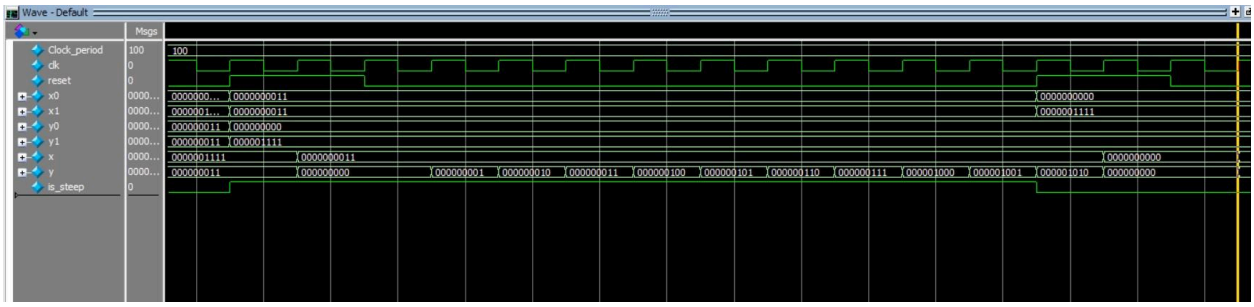

Figure 3.2: ModelSim waveform of Vertical Line

Shows Situation where a coordinates for x0, x1, y0, y1 are given such that a vertical line is drawn. As you can see the y coordinates increase by one but the x coordinates stay the same which shows how the vertical line is being drawn.

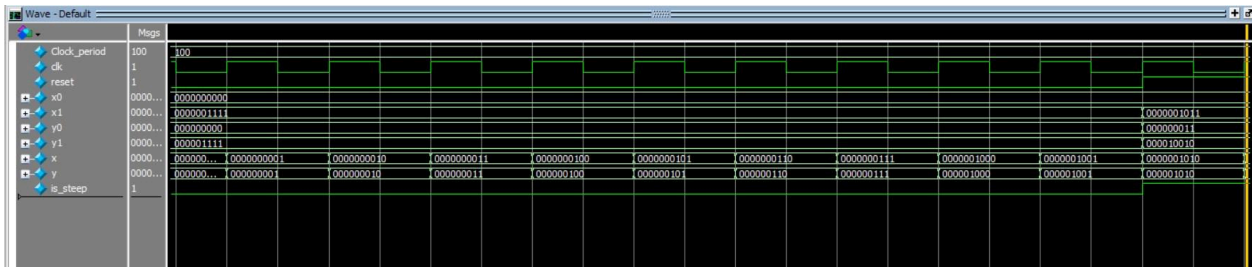

Figure 3.3: ModelSim waveform of diagonal from origin

Shows Situation where a coordinates for x0, x1, y0, y1 are given such that a perfectly diagonal line is drawn from the origin. As you can see the x coordinates and y coordinates increase at the same time/ratio-linearly.

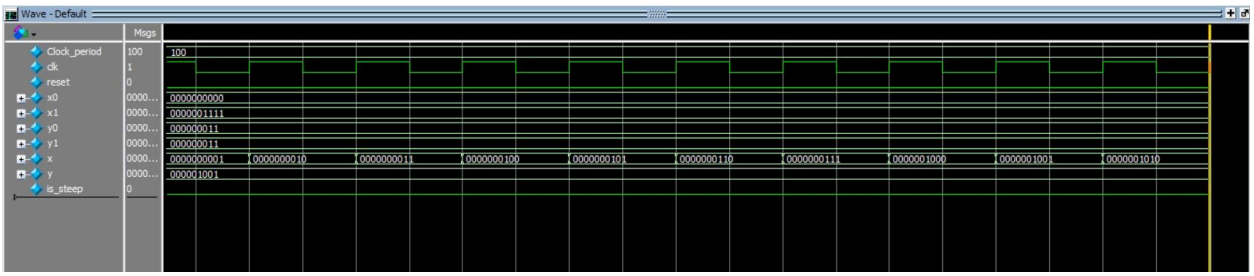

Figure 3.4: ModelSim waveform of gradual negative slope

Shows Situation where a coordinates for x0, x1, y0, y1 are given such that a gradual line with a negative slope is drawn not from the axis of the display. As you can see the x coordinates increase ever so often but the y coordinates increase steadily(a slope that is not the same for rise and run).

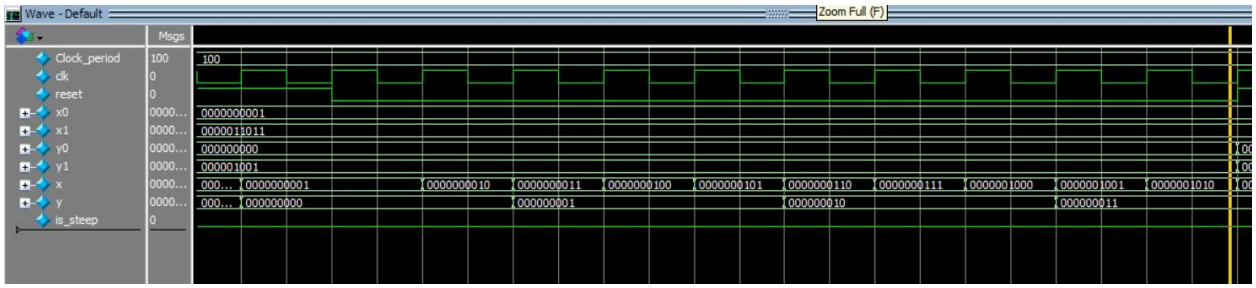

Figure 3.5: ModelSim waveform of gradual positive slope

Shows Situation where a coordinates for x0, x1, y0, y1 are given such that a gradual line with a positive slope is drawn not from the axis of the display. As you can see the y coordinates increase ever so often but the x coordinates increase steadily(a slope that is not the same for rise and run).

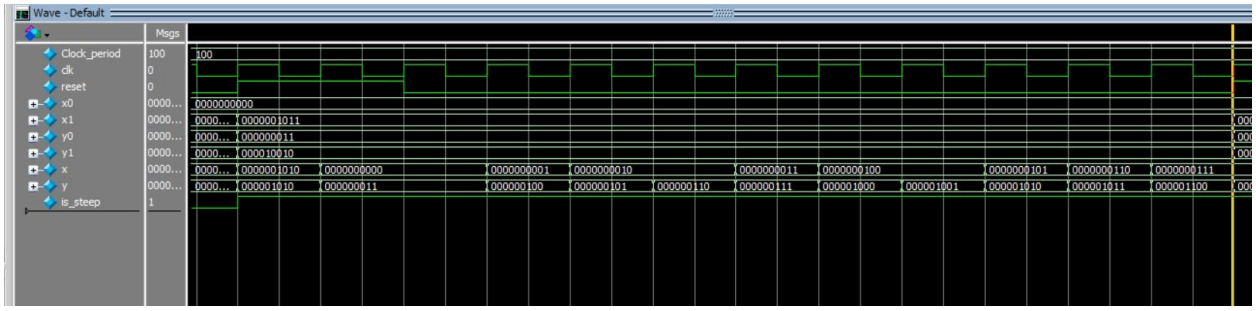

Figure 3.6: ModelSim waveform of steep positive slope

Shows Situation where a coordinates for x0, x1, y0, y1 are given such that a steep line with a positive slope is drawn not from the axis of the display. As you can see the y coordinates increase ever so often but the x coordinates increase steadily(a slope that is not the same for rise and run).

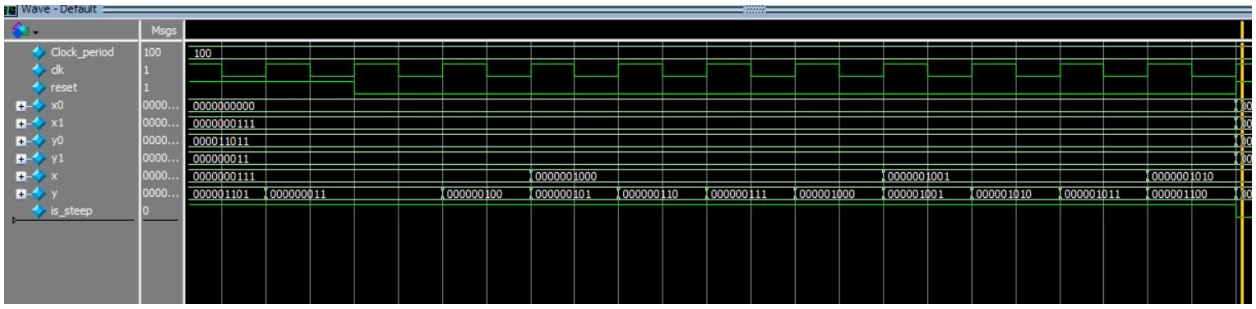

Figure 3.7: ModelSim waveform of steep negative slope

Shows Situation where a coordinates for x0, x1, y0, y1 are given such that a steep line with a negative slope is drawn not from the axis of the display. As you can see the x coordinates increase ever so often but the y coordinates increase steadily(a slope that is not the same for rise and run).

2. **DE1_SoC_testbench**: This testbench simulates 7 different types of line drawings, each of which are described below with figures that go along with the description.

Task #2: Moving/Animating Arbitrary Lines

Each of the testbench simulations tested the following situations:

1. **DE1_SoC_testbench**: This testbench simulates
2. **button_press_testbench**: This testbench simulates
3. **clear_display_testbench**: This testbench simulates

Simulation waveforms of DE1_SoC_testbench:

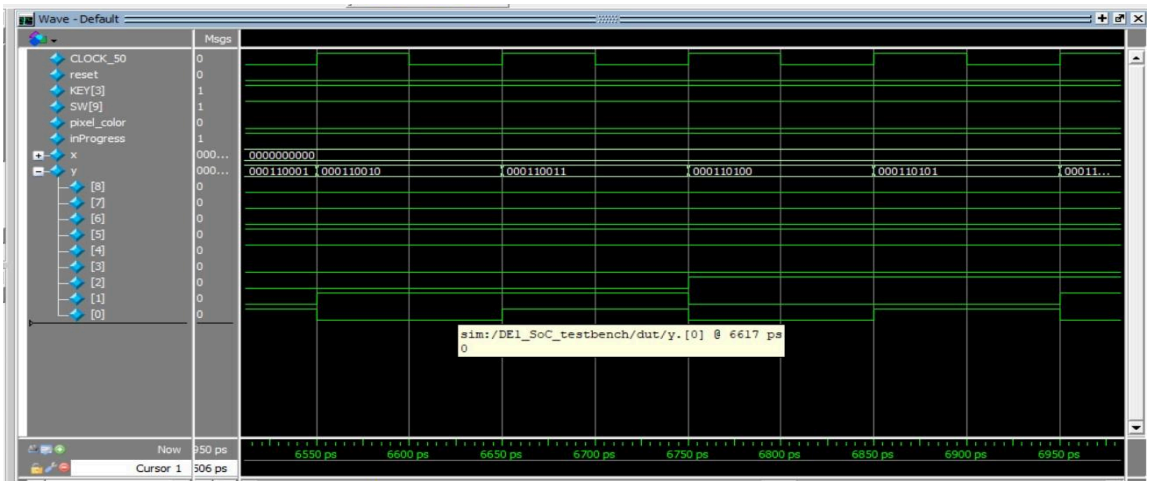

Figure 4: ModelSim waveform of DE1_SoC_testbench

Shows Situation where SW[9] is off and reset is on so there would be no drawing, a blank screen. It also shows where reset is off and SW[9] is on for 100 repeats of a posedge which shows how the display will draw the coordinates stored in the RAM.

Simulation waveforms of buton_press_testbench:

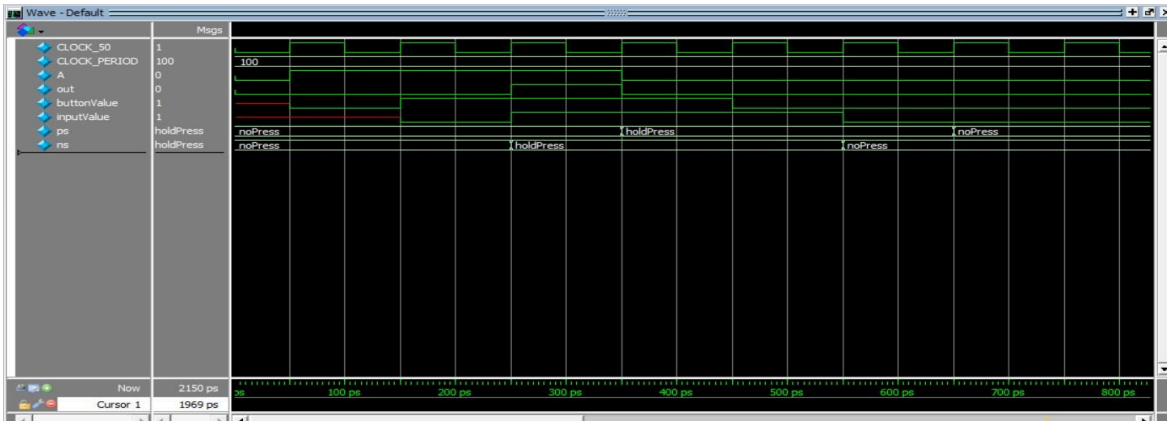

Figure 4: ModelSim waveform of button_press_testbench

Shows Situation where random button presses, A being on and off, are simulated for different amounts of time. When there is a button press you can see that the ps state goes from noPress to holdPress and continues to stay in that state until A is turned off in which it transitions to state noPress again.

Simulation waveforms of clear_display_testbench:

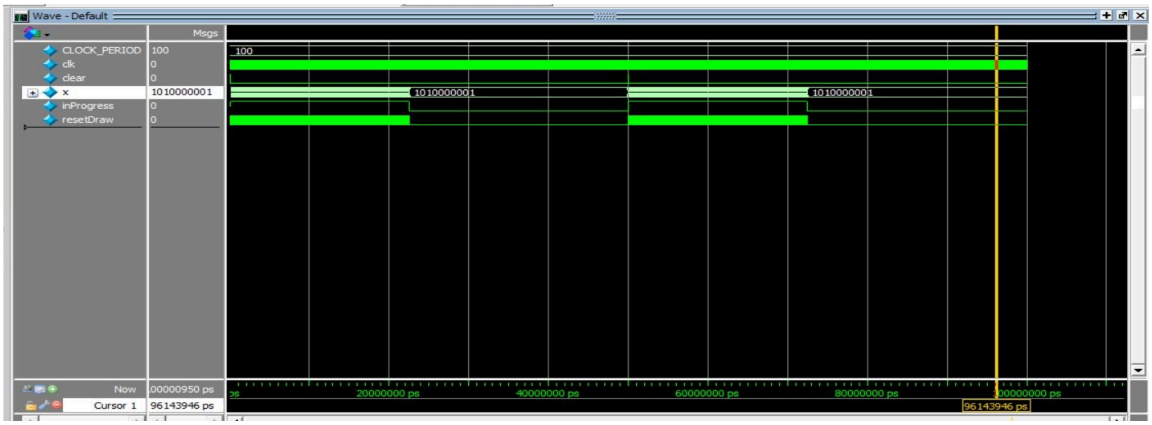

Figure 4: ModelSim waveform of clear_display_testbench

Shows Situation that if a clear signal is high and it is run for many clock cycles it cycles through each x coordinate it draws it/colors it in black. The above diagram shows that the clear signal is being used properly as the very close together green lines show the increase in x every 350 clock cycles.

Section 3: Final Product

The final product includes a system that can draw a line from any two arbitrary coordinates/points given by implementing the Bresenham's line algorithm. This system is able to also animate these lines by using a FSM and a RAM to hold the coordinates of multiple points and cycle through them to create a repeating design that clears each time its asked to draw the design again. This system also has clear and reset capabilities where the clear makes the display all black and counties drawing from the beginging if the system is still in progress of drawing or it completely creates a blank display and keeps it that way until the system is said to draw again.

Section 4: Appendix

TASK 1:

1) DE1_SoC

Date: February 11, 2025 DE1_SoC.sv Project: DE1_SoC

```
1   //Nithya Subramanian
2   //Feburary 9th 2025
3   //EE 371
4   //Lab 3, Task 1
5
6   //DE1_SoC is the top level module of this project and it initilizes
7   //VGA_frambuffer and line_drawer module to draw any line from point x
8   //to point y on a VGA display.
9   module DE1_SoC (HEX0, HEX1, HEX2, HEX3, HEX4, HEX5, KEY, LEDR, SW, CLOCK_50,
10     VGA_R, VGA_G, VGA_B, VGA_BLANK_N, VGA_CLK, VGA_HS, VGA_SYNC_N, VGA_VS);
11
12     output logic [6:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
13     output logic [9:0] LEDR;
14     input logic [3:0] KEY;
15     input logic [9:0] SW;
16
17     input CLOCK_50;
18     output [7:0] VGA_R;
19     output [7:0] VGA_G;
20     output [7:0] VGA_B;
21     output VGA_BLANK_N;
22     output VGA_CLK;
23     output VGA_HS;
24     output VGA_SYNC_N;
25     output VGA_VS;
26
27     assign HEX0 = '1;
28     assign HEX1 = '1;
29     assign HEX2 = '1;
30     assign HEX3 = '1;
31     assign HEX4 = '1;
32     assign HEX5 = '1;
33     assign LEDR = SW;
34
35     logic [9:0] x0, x1, x;
36     logic [8:0] y0, y1, y;
37     logic frame_start;
38     logic pixel_color;
39
40
41     //////// DOUBLE_FRAME_BUFFER ////////
42     logic dfb_en;
43     assign dfb_en = 1'b0;
44     ////////////////////////////////////////
45
46     VGA_framebuffer fb(.clk(CLOCK_50), .rst(1'b0), .x, .y,
47             .pixel_color, .pixel_write(1'b1), .dfb_en, .frame_start,
48             .VGA_R, .VGA_G, .VGA_B, .VGA_CLK, .VGA_HS, .VGA_VS,
49             .VGA_BLANK_N, .VGA_SYNC_N);
50
51     // draw lines between (x0, y0) and (x1, y1)
52     line_drawer lines (.clk(CLOCK_50), .reset(~KEY[3]),
53             .x0, .y0, .x1, .y1, .x, .y);
54
55     //draw an arbitrary line
56     assign x0 = 0;
57     assign y0 = 0;
58     assign x1 = 240;
59     assign y1 = 240;
60
61
62     /*// draw horz
63     assign x0 = 100;
64     assign y0 = 500;
65     assign x1 = 300;
66     assign y1 = 500;*/
67
68     /*draw vertical
69     assign x0 = 0;
70     assign y0 = 50;
71     assign x1 = 240;
72     assign y1 = 50;*/
73
```

```
74      /*draw arbitrary pos slop
75      assign x0 = 50;
76      assign y0 = 100;
77      assign x1 = 240;
78      assign y1 = 50;*/
79
80      /*draw arbitrary neg slop
81      assign x0 = 50;
82      assign y0 = 25;
83      assign x1 = 100;
84      assign y1 = 240;*/
85
86
87      // draw an arbitrary line for testbench- much smaller
88      //assign x0 = 0;
89      //assign y0 = 3;
90      //assign x1 = 15;
91      //assign y1 = 25;
92
93      //assigns write in black if SW[9] off and white if SW[9] on
94      assign pixel_color = SW[9] ? 1'b1 : 1'b0;
95      //assign pixel_color = 1'b1;
96
97  endmodule
98
99  //a testbench for DE1_SoC that simulates/test all situations in that testbench
100 module DE1_SoC_testbench();
101     logic [6:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
102     logic [9:0] LEDR;
103     logic [3:0] KEY;
104     logic [9:0] SW;
105
106     logic CLOCK_50;
107     logic [7:0] VGA_R;
108     logic [7:0] VGA_G;
109     logic [7:0] VGA_B;
110     logic VGA_BLANK_N;
111     logic VGA_CLK;
112     logic VGA_HS;
113     logic VGA_SYNC_N;
114     logic VGA_VS;
115
116
117     DE1_SoC dut (.HEX0, .HEX1, .HEX2, .HEX3, .HEX4, .HEX5, .KEY, .LEDR, .SW, .CLOCK_50,
118     .VGA_R, .VGA_G, .VGA_B, .VGA_BLANK_N, .VGA_CLK, .VGA_HS, .VGA_SYNC_N, .VGA_VS);
119
120     logic reset;
121     assign KEY[3] = ~reset;
122
123     parameter CLOCK_PERIOD = 100;
124
125     initial begin
126        CLOCK_50 <= 100;
127        forever #(CLOCK_PERIOD / 2) CLOCK_50 <= ~CLOCK_50;
128     end
129
130     initial begin
131        //check line when reset is on and SW[9] is 0 (black)
132        reset <= 1; SW[9] <= 0; repeat (10) @(posedge CLOCK_50);
133
134        //check line drawing when reset off and SW[9] is 1 (white)
135        reset <= 0; SW[9] <= 1; repeat (100) @(posedge CLOCK_50);
136
137        $stop;
138     end
139 endmodule
140
141
```

2) line_drawer

```
1   //Nithya Subramanian
2   //Feburary 9th 2025
3   //EE 371
4   //Lab 3, Task 1 and 2
5
6   //This module line_drawer has input signals clk and reset which are 1-bit inputs
7   //as well as two coordinates x and y that are 10 and 9 bit inputs(respectivley)
8   //x0, x1, y0, y1 are the start and end coordinates of the line. This module
9   //outputs 2 signals- x (10 bit) and y (9 bit) which correspond to the coordinate
10  //pair (x, y). This module given these inputs will use the Bresenham's line algo
11  //to draw a line between the two sets of input coordinates given (x0, x1, y0, y1).
12  //The module will use a certain amount of clock cyles(dependednt on length of line)
13  //as each clock cyle as one pixel is drawn.
14  module line_drawer(
15     input logic clk, reset,
16
17     // x and y coordinates for the start and end points of the line
18     input logic [9:0] x0, x1,
19     input logic [8:0] y0, y1,
20
21     //outputs cooresponding to the coordinate pair (x, y)
22     output logic [9:0] x,
23     output logic [8:0] y
24     );
25
26     //internal registers
27     logic is_steep;
28     logic signed [10:0] delta_x;
29     logic signed [9:0] delta_y;
30     logic signed [11:0] error;
31     logic signed [10:0] x_start, x_end;
32     logic signed [9:0] y_start, y_end;
33     integer x_step, y_step;
34
35     //Registers that help with iteration
36     logic [9:0] x_curr;
37     logic [8:0] y_curr;
38
39     //finds the gap between the x and y coordinates and
40     //uses that to find if the line is steep
41     assign delta_x = (x0 > x1) ? (x0 - x1) : (x1 - x0);
42     assign delta_y = (y0 > y1) ? (y0 - y1) : (y1 - y0);
43     assign is_steep = (delta_y > delta_x) ? 1'b1 : 1'b0;
44
45     always_comb begin
46
47        //if steep start with moving from the smaller y value
48        if(is_steep) begin
49           x_start = (y0 <= y1) ? x0 : x1;
50           y_start = (y0 <= y1) ? y0 : y1;
51           x_end = (y0 > y1) ? x0 : x1;
52           y_end = (y0 > y1) ? y0 : y1;
53        end
54
55        //if not steep start on smaller x
56        else begin
57           x_start = (x0 <= x1) ? x0 : x1;
58           y_start = (x0 <= x1) ? y0 : y1;
59           x_end = (x0 > x1) ? x0 : x1;
60           y_end = (x0 > x1) ? y0 : y1;
61        end
62     end
63
64     //to see if the line has positive or negative slope
65     assign y_step = (y_end > y_start) ? 1 : -1;
66     assign x_step = (x_end > x_start) ? 1 : -1;
67
68     //logic for how the line is drawn depending on if the line is steep
69     //or gradual. If the line is steep it is drawn by increasing the y
70     //coordinate by one and the x by x_step, if it is not it is drawn by
71     //increasing the x by one and y by y_step
72     always_ff @(posedge clk) begin
73
```

```
74          if(reset) begin
75             x <= x_start;
76             y <= y_start;
77
78             error <= (is_steep) ? -delta_y / 2 : -delta_x / 2;
79          end
80
81          //if line is step it increases y by one
82          else if ((is_steep == 1) & (y != y_end)) begin
83             y <= y + 1;
84
85             if((error + delta_x) >= 0) begin
86                x <= x + x_step;
87                error <= error + (delta_x - delta_y);
88             end
89
90             else
91                error <= error + delta_x;
92          end
93
94          //if line is gradual it increases x by one
95          else if (x != x_end) begin
96             x <= x + 1;
97
98             if((error + delta_y) >= 0) begin
99                y <= y + y_step;
100               error <= error + (delta_y - delta_x);
101            end
102
103            else
104               error <= error + delta_y;
105         end
106      end
107   endmodule
108
109   //testbench of line_drawer module that simulates/tests all scenarios for this module
110   module line_drawer_testbench();
111      logic clk, reset;
112      logic [9:0] x0, x1;
113      logic [8:0] y0, y1;
114      logic [9:0] x;
115      logic [8:0] y;
116
117      line_drawer dut (.clk(clk), .reset(reset), .x0(x0), .x1(x1), .y0(y0), .y1(y1), .x(x), .y(
      y));
118
119      parameter CLOCK_PERIOD = 100;
120
121      initial begin
122         clk <= 0;
123         forever #(CLOCK_PERIOD / 2) clk <= ~clk;
124      end
125
126      initial begin
127         //draws a horizontal line from x = 0 to x = 15
128         reset <= 1; x0 <= 0; y0 <= 3; x1 <= 15; y1 <= 3; repeat(2) @(posedge clk);
129         reset <= 0; repeat(20) @(posedge clk);
130
131         //draws a vertical line from y = 0 to y = 15
132         reset <= 1; x0 <= 3; y0 <= 0; x1 <= 3; y1 <= 15; repeat(2) @(posedge clk);
133         reset <= 0; x0 <= 3; y0 <= 0; x1 <= 3; y1 <= 15; repeat(10) @(posedge clk);
134
135         //draws a diagonal line starting from origin with positive slope
136         reset <= 1; x0 <= 0; y0 <= 0; x1 <= 15; y1 <= 15; repeat(2) @(posedge clk);
137         reset <= 0; x0 <= 0; y0 <= 0; x1 <= 15; y1 <= 15; repeat(10) @(posedge clk);
138
139         //draws a diagonal line starting from y axis with positive steep slope
140         reset <= 1; x0 <= 0; y0 <= 3; x1 <= 11; y1 <= 18; repeat(2) @(posedge clk);
141         reset <= 0; x0 <= 0; y0 <= 3; x1 <= 11; y1 <= 18; repeat(10) @(posedge clk);
142
143         //draws a diagonal starting from y axis with negative steep slope
144         reset <= 1; x0 <= 0; y0 <= 27; x1 <= 7; y1 <= 3; repeat(2) @(posedge clk);
145         reset <= 0; x0 <= 0; y0 <= 27; x1 <= 7; y1 <= 3; repeat(10) @(posedge clk);
```

```
146
147         //draws a line with a positive gradual slope
148         reset <= 1; x0 <= 1; y0 <= 0; x1 <= 27; y1 <= 9; repeat(2) @(posedge clk);
149         reset <= 0; x0 <= 1; y0 <= 0; x1 <= 27; y1 <= 9; repeat(10) @(posedge clk);
150
151         //draws a line with a negative gradual slope
152         reset <= 1; x0 <= 1; y0 <= 9; x1 <= 27; y1 <= 0; repeat(2) @(posedge clk);
153         reset <= 0; x0 <= 0; y0 <= 3; x1 <= 15; y1 <= 3; repeat(10) @(posedge clk);
154         $stop;
155       end
156   endmodule
```

3) VGA_framebuffer

```
1   //Nithya Subramanian
2   //Feburary 9th 2025
3   //EE 371
4   //Lab 3, Task 1
5   // VGA driver: provides I/O timing and double-buffering for the VGA port.
6
7   module VGA_framebuffer(
8      input logic clk, rst,
9      input logic [9:0] x, // The x coordinate to write to the buffer.
10     input logic [8:0] y, // The y coordinate to write to the buffer.
11     input logic pixel_color, pixel_write, // The data to write (color) and write-enable.
12
13     input logic dfb_en, // Double-Frame Buffer Enable
14
15     output logic frame_start,   // Pulse is fired at the start of a frame.
16
17     // Outputs to the VGA port.
18     output logic [7:0] VGA_R, VGA_G, VGA_B,
19     output logic VGA_CLK, VGA_HS, VGA_VS, VGA_BLANK_N, VGA_SYNC_N
20  );
21
22     /*
23     *
24     * HCOUNT 1599 0             1279       1599 0
25     *             _______________           ________
26     * ___________|    Video      |_____________|  Video
27     *
28     *
29     * |SYNC| BP |<-- HACTIVE -->|FP|SYNC| BP |<-- HACTIVE
30     *       _____________________  _____________
31     * |____|       VGA_HS          |____|
32     *
33     */
34
35     // Constants for VGA timing.
36     localparam HPX = 11'd640*2, HFP = 11'd16*2, HSP = 11'd96*2, HBP = 11'd48*2;
37     localparam VLN = 11'd480,   VFP = 10'd11,   VSP = 10'd2,    VBP = 10'd31;
38     localparam HTOTAL = HPX + HFP + HSP + HBP; // 800*2=1600
39     localparam VTOTAL = VLN + VFP + VSP + VBP; // 524
40
41     // Horizontal counter.
42     logic [10:0] h_count;
43     logic end_of_line;
44
45     assign end_of_line = h_count == HTOTAL - 1;
46
47     always_ff @(posedge clk)
48        if (rst) h_count <= 0;
49        else if (end_of_line) h_count <= 0;
50        else h_count <= h_count + 11'd1;
51
52     // Vertical counter & buffer swapping.
53     logic [9:0] v_count;
54     logic end_of_field;
55     logic front_odd; // whether odd address is the front buffer.
56
57     assign end_of_field = v_count == VTOTAL - 1;
58     assign frame_start = !h_count && !v_count;
59
60     always_ff @(posedge clk)
61        if (rst) begin
62           v_count <= 0;
63           front_odd <= 0;
64        end else if (end_of_line)
65           if (end_of_field) begin
66              v_count <= 0;
67              front_odd <= !front_odd;
68           end else
69              v_count <= v_count + 10'd1;
70
71     // Sync signals.
72     assign VGA_CLK = h_count[0]; // 25 MHz clock: pixel latched on rising edge.
73     assign VGA_HS = !(h_count - (HPX + HFP) < HSP);
```

```
74      assign VGA_VS = !(v_count - (VLN + VFP) < VSP);
75      assign VGA_SYNC_N = 1; // Unused by VGA
76
77      // Blank area signal.
78      logic blank;
79      assign blank = h_count >= HPX || v_count >= VLN;
80
81      // Double-buffering.
82      logic buffer[640*480*2-1:0];
83      logic [19:0] wr_addr, rd_addr;
84      logic rd_data;
85
86      assign wr_addr = {y * 19'd640 + x, (!front_odd & dfb_en)};
87      assign rd_addr = {v_count * 19'd640 + (h_count / 19'd2), (front_odd & dfb_en)};
88
89      always_ff @(posedge clk) begin
90         if (pixel_write) buffer[wr_addr] <= pixel_color;
91         if (VGA_CLK) begin
92            rd_data <= buffer[rd_addr];
93            VGA_BLANK_N <= ~blank;
94         end
95      end
96
97      // Color output.
98      assign {VGA_R, VGA_G, VGA_B} = rd_data ? 24'hFFFFFF : 24'h000000;
99   endmodule
100
```

TASK 2:

1) DE1_SoC

```
1   //Nithya Subramanian
2   //Feburary 9th 2025
3   //EE 371
4   //Lab 3, Task 2
5
6   //DE1_SoC is the top level module of this project and it initilizes
7   //VGA_frambuffer and line_drawer module to draw any line from point x
8   //to point y on a VGA display.
9   module DE1_SoC (HEX0, HEX1, HEX2, HEX3, HEX4, HEX5, KEY, LEDR, SW, CLOCK_50,
10     VGA_R, VGA_G, VGA_B, VGA_BLANK_N, VGA_CLK, VGA_HS, VGA_SYNC_N, VGA_VS);
11
12     output logic [6:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
13     output logic [9:0] LEDR;
14     input logic [3:0] KEY;
15     input logic [9:0] SW;
16
17     input CLOCK_50;
18     output [7:0] VGA_R;
19     output [7:0] VGA_G;
20     output [7:0] VGA_B;
21     output VGA_BLANK_N;
22     output VGA_CLK;
23     output VGA_HS;
24     output VGA_SYNC_N;
25     output VGA_VS;
26
27     assign HEX0 = '1;
28     assign HEX1 = '1;
29     assign HEX2 = '1;
30     assign HEX3 = '1;
31     assign HEX4 = '1;
32     assign HEX5 = '1;
33     assign LEDR = SW;
34
35     logic [9:0] x0, x1, x, clear_all;
36     logic [8:0] y0, y1, y;
37     logic frame_start;
38     logic pixel_color;
39
40     logic drawNow;
41     assign drawNow = SW[9];
42
43
44
45     //////// DOUBLE_FRAME_BUFFER ////////
46     logic dfb_en;
47     assign dfb_en = 1'b0;
48     ////////////////////////////////////////
49
50
51     logic rst_clear, rst_animate;
52     logic inProgress, clr_draw;
53
54     button_press button (.A(~KEY[3]), .out(clr_draw), .clk(CLOCK_50));
55
56     clear_display clearDraw (.clear(clr_draw), .clk(CLOCK_50), .inProgress(inProgress), .
    resetDraw(rst_clear), .x(clear_all));
57
58     //A bus that holds all coordinates for each variable
59     logic [9:0] x0_base, x1_base;
60     logic [8:0] y0_base, y1_base;
61
62
63      // Assigns what action should be completed based on the values
64     assign x0_base = inProgress ? clear_all : x0;
65     assign y0_base = inProgress ? 0 : y0;
66     assign x1_base = inProgress ? clear_all : x1;
67     assign y1_base = inProgress ? 480 : y1;
68
69     assign pixel_color = inProgress ? 1'b0 : 1'b1;
70
71     //creates a RAM that holds points needed to draw
72     logic [9:0] x0_points [0:5];
```

```
73        logic [8:0] y0_points [0:5];
74        logic [9:0] x1_points [0:5];
75        logic [8:0] y1_points [0:5];
76
77        assign x0_points[0] = 240;
78        assign x0_points[1] = 340;
79        assign x0_points[2] = 340;
80        assign x0_points[3] = 240;
81        assign x0_points[4] = 240;
82        assign x0_points[5] = 290;
83
84        assign y0_points[0] = 340;
85        assign y0_points[1] = 340;
86        assign y0_points[2] = 240;
87        assign y0_points[3] = 240;
88        assign y0_points[4] = 290;
89        assign y0_points[5] = 340;
90
91        assign x1_points[0] = 240;
92        assign x1_points[1] = 240;
93        assign x1_points[2] = 180;
94        assign x1_points[3] = 180;
95        assign x1_points[4] = 240;
96        assign x1_points[5] = 350;
97
98        assign y1_points[0] = 240;
99        assign y1_points[1] = 180;
100       assign y1_points[2] = 180;
101       assign y1_points[3] = 240;
102       assign y1_points[4] = 350;
103       assign y1_points[5] = 240;
104
105       //initilizes VGA_framebuffer
106       VGA_framebuffer fb(
107         .clk(CLOCK_50), .rst(1'b0), .x, .y,
108         .pixel_color, .pixel_write(1'b1), .dfb_en(), .frame_start,
109         .VGA_R, .VGA_G, .VGA_B, .VGA_CLK, .VGA_HS, .VGA_VS,
110         .VGA_BLANK_N, .VGA_SYNC_N);
111
112       //initilizes line_drawer
113       line_drawer lines (
114         .clk(CLOCK_50),
115         .reset(rst_clear | rst_animate),
116         .x0(x0_base), .y0(y0_base), .x1(x1_base), .y1(y1_base), .x, .y);
117
118       integer counter, index;
119
120       //uses different signals to find whether the machine should draw, clear ect. it also uses
121       //a counter to slow down the time taken to update the machine
122       always_ff @(posedge CLOCK_50) begin
123          if (clr_draw) begin
124             counter <= 0;
125             index <= 0;
126             x0 <= 0;
127             y0 <= 0;
128             x1 <= 0;
129             y1 <= 0;
130          end
131
132          else if (counter == 1) begin
133             counter <= counter + 1;
134             rst_animate <= 1'b1;
135          end
136
137          else if (counter == 5) begin
138             counter <= counter + 1;
139             rst_animate <= 1'b0;
140          end
141
142          else if (counter == (50000000 / 2)) begin
143             counter <= 0;
144
145             if (index < 5) begin
```

```
146                index <= index + 1;
147             end
148
149             else begin
150                index <= 0;
151             end
152
153                x0 <= x0_points[index];
154                y0 <= y0_points[index];
155                x1 <= x1_points[index];
156                y1 <= y1_points[index];
157          end
158
159          else if (drawNow) begin
160             counter <= counter + 1;
161          end
162       end
163    endmodule
164
165
166    //a testbench for DE1_SoC that simulates/test all situations in that testbench
167    module DE1_SoC_testbench();
168       logic [6:0] HEX0, HEX1, HEX2, HEX3, HEX4, HEX5;
169       logic [9:0] LEDR;
170       logic [3:0] KEY;
171       logic [9:0] SW;
172
173       logic CLOCK_50;
174       logic [7:0] VGA_R;
175       logic [7:0] VGA_G;
176       logic [7:0] VGA_B;
177       logic VGA_BLANK_N;
178       logic VGA_CLK;
179       logic VGA_HS;
180       logic VGA_SYNC_N;
181       logic VGA_VS;
182
183
184       DE1_SoC dut (.HEX0, .HEX1, .HEX2, .HEX3, .HEX4, .HEX5, .KEY, .LEDR, .SW, .CLOCK_50,
185       .VGA_R, .VGA_G, .VGA_B, .VGA_BLANK_N, .VGA_CLK, .VGA_HS, .VGA_SYNC_N, .VGA_VS);
186
187       logic reset;
188       assign KEY[3] = ~reset;
189
190       parameter CLOCK_PERIOD = 100;
191
192       initial begin
193          CLOCK_50 <= 100;
194          forever #(CLOCK_PERIOD / 2) CLOCK_50 <= ~CLOCK_50;
195       end
196
197       initial begin
198          //check line when reset is on and SW[9] is 0 (black)
199          reset <= 1; SW[9] <= 0; repeat (10) @(posedge CLOCK_50);
200
201          //check line drawing when reset off and SW[9] is 1 (white)
202          reset <= 0; SW[9] <= 1; repeat (100) @(posedge CLOCK_50);
203
204          $stop;
205       end
206    endmodule
207
208
```

2) button_press

```
1   //Nithya Subramanian
2   //Feburary 9th 2025
3   //EE 371
4   //Lab 3, Task 2
5
6   //button_press is to ensure that a users button value is
7   //not overlooked or missed. Takes in button input value A
8   // and clk and outputs with 1-bit signal out.
9   module button_press (A, out, clk);
10     input logic A, clk;
11     output logic out;
12
13     logic buttonValue, inputValue;
14
15     // put the input logic through 2 D_FFs to clean up
16     always_ff @(posedge clk) begin
17        buttonValue <= A;
18        inputValue <= buttonValue;
19     end
20
21     enum {noPress, holdPress} ps, ns;
22
23     //if a button is pressed the value is held until the
24     //the button is realeased
25     always_comb begin
26        case(ps)
27           noPress:
28              if (inputValue)
29                 ns = holdPress;
30
31              else
32                 ns = noPress;
33
34           holdPress:
35              if (inputValue)
36                 ns = holdPress;
37              else
38                 ns = noPress;
39        endcase
40     end
41
42     // Combinatinal logic that figures out what the output value
43     //should be based on the state it is in
44     always_comb begin
45        case (ps)
46           noPress:
47              if (inputValue)
48                 out = 1'b1;
49
50              else
51                 out = 1'b0;
52
53           holdPress:
54              out = 1'b0;
55        endcase
56     end
57
58     // Tells the machine what state to go to after present
59     always_ff @(posedge clk) begin
60           ps <= ns;
61     end
62  endmodule
63
64  //a testbench for button_press that simulates/test all situations in that testbench
65  module button_press_testbench();
66     logic A, clk, out;
67     logic CLOCK_50;
68
69     button_press dut (.A(A), .clk(CLOCK_50), .out(out));
70
71     parameter CLOCK_PERIOD = 100;
72     initial begin
73        CLOCK_50 <= 0;
```

```
74          forever #(CLOCK_PERIOD/2) CLOCK_50 <= ~CLOCK_50;
75      end
76
77      initial begin
78
79          //simulate random times of button presses
80          A <= 0; repeat(7); @(posedge CLOCK_50);
81          A <= 1; repeat(3) @(posedge CLOCK_50);
82          A <= 0; repeat(5) @(posedge CLOCK_50);
83          A <= 1; repeat(1) @(posedge CLOCK_50);
84          A <= 0; repeat(6) @(posedge CLOCK_50);
85          A <= 1; repeat(4) @(posedge CLOCK_50);
86          A <= 0; repeat(2) @(posedge CLOCK_50);
87          $stop;
88      end
89  endmodule
```

3) Clear_display

```
Date: February 14, 2025        clear_display.sv        Project: DE1_SoC
```

```
1   //Nithya Subramanian
2   //Feburary 9th 2025
3   //EE 371
4   //Lab 3, Task 2
5
6   //clear_display takes in 1-bit valyes clear, clk. inProgress output
7   // tells the mdoule if the display needs to be cleared inProgress
8   //tells the module if a draw is still in progress and so the clear
9   //needs to happen and then a cycle of the same coordinates occur
10  //which is the output value resetDraw, the x output ist the coordinate
11  //that the dispaly is on.
12  module clear_display (clear, clk, inProgress, resetDraw, x);
13      input logic clear, clk;
14      output logic [9:0] x;
15      output logic inProgress;
16      output logic resetDraw;
17
18      integer counter;
19      logic enable;
20
21      //uses the enable and counter signals to decide what action
22      //the user wants us to take. counter is used to slow down the
23      //actions and increments occuring
24      always_ff @(posedge clk) begin
25        if (inProgress) begin
26           if (clear) begin
27              counter <= 0;
28              enable <= 1'b0;
29              resetDraw <= 1'b1;
30            end
31
32            else if (counter == 5) begin
33                  counter <= counter + 1;
34                  resetDraw <= 1'b0;
35            end
36
37            else if (counter == 350) begin
38                  counter <= 0;
39                  enable <= 1'b1;
40                  resetDraw <= 1'b1;
41            end
42
43            else begin
44                  counter <= counter + 1;
45                  enable <= 1'b0;
46            end
47        end
48
49        else begin
50           resetDraw <= 1'b0;  // End drawing when x reaches 641
51        end
52     end
53
54        //if the clear is on the x coordinate should reset to 0 while
55        //the inProgress coordinate should be 1 since a reset is happneing
56        //but if not the x should increment by 1 unless it gets to the last
57        //index then the clear has completed.
58        always_ff @(posedge clk) begin
59           if(clear) begin
60              x <= 0;
61              inProgress <= 1'b1;
62           end
63
64           else if (enable & x < 641) begin
65              x <= x + 1;
66           end
67
68           else if (x == 641) begin
69              inProgress <= 1'b0;
70           end
71        end
72  endmodule
73
```

```
74  //a testbench for clear_display that simulates/test all situations in that testbench
75  module clear_display_testbench();
76     logic clear, clk;
77     logic [9:0] x;
78     logic inProgress;
79     logic resetDraw;
80
81     clear_display dut (.*);
82
83     parameter CLOCK_PERIOD = 100;
84
85     initial begin
86        clk <= 0;
87        forever #(CLOCK_PERIOD / 2) clk <= ~clk;
88     end
89
90     initial begin
91        clear <= 1;       repeat(5)      @(posedge clk);
92        clear <= 0;       repeat(500000) @(posedge clk);
93        clear <= 1;       repeat(5)      @(posedge clk);
94        clear <= 0;       repeat(500000) @(posedge clk);
95        $stop;
96     end
97  endmodule
98
```