the value of memory location 2000 is?

Instruction (Assembly)	operations
MOV R1, 15	R1 ← 15
MOV R2, (2000)	R2 ← M[2000]
SUB R2, R1	R2 ← R2 − R1
MOV (2000), R2	M[2000] ← R2
HALT	Stop

R1 = 15	R2 = 32 − 15	M[2000] = R2
R2 = 32	R2 = 17	M[2000] = 17

Ans : 17

* Instruction — Lecture 7

- The commands to CPU for performing operation.

* Digital computer

input (Binary) → Digital Computer (CPU) → output (binary)

Program + data

#code
int main()
{
return 0;
}
(High level program)

→ Compiler / Langyge translator

0 0 1 ...
1 0 1 0 1 ...
machine code (Binary) code
Low level language program
bytecode

Programing Statement

Instruction

Instruction

A group of bit which instructs computer to perform some operation

instruction code

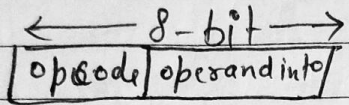
operation/ operand info

or

op-code

* Example: A cpu supports 8 bits instructions

Assume:



opcode ⇒ 000
001
010
011
100
101
110
111

* The type of instruction in CPU is identified by its operation/opcode.

op code

000	→	addition
001	→	Subtration
010	→	AND
011	→	OR
100	→	MOV
101	→	Load
110	→	Store
111	→	Increment

max opcode combinations = $2^3 = 8$

* The cpu can support maximum 8 disticnct operation.

MY CHOICE
Date:
Page No.:

* The cpu can support maximum 8 distinct instructions.

* Instruction set Architecture (ISA)
  ↳ Collection of all instruction supported by CPU

* Type of Instruction
  ↳ Based of operation
  ↳ Based on operand

* 3- Address Instruction
  ↳ Maximum 3 address can be specified within an instruction

Opcode	Add-1	Add-2	Add-3

Supports – 2 address
1 address
0 address

ADD R0, R1, R3
R0 ← R1 + R3

* 2 Address Instruction

ADD R1, R3
R1 ← R1 + R3

* 1 Address Instruction
  ⇓
  ADD R3
  ⇓
  AC ← AC + R3

one of the two operand is used as source and destination both
* The old value of the common operand is overwritten by the result.

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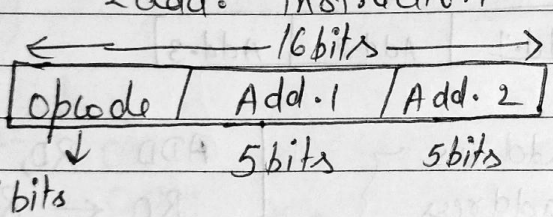
If need 2nd operand is taken from Accumulator.
- Such type of instruction supported in Accumulator based architecture.

* 0 address Instruction
No address within an instruction
↳ Supported in stack based architecture

opcode

Ques ① Consider a digital which only supports only 2 address instruction each with 16-bit if address length is 5 bits then maximum and minimum how many instruction supported by the system

Sol :- 2 add. instruction



max opcode $\Rightarrow 2^6 = 64$
max number of instruction = 64
min " " = 1

Ques ② Consider a digital computer which supports 16 bit 2 add. instruction. If address length is 6 bit then the length of instruction is ?

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Sol No. of instruction supported = 16 ⇒ operation ⇒ 4bits
Code

2 add.

opcode	Add.1	Add.2
4bits	6 bits	bits = 16 bits Ans

$\log_2 16 \Longrightarrow 4$

Que 3 gate – 2016

A processor has 40 distinct instruction and 24 general purpose registers. A 32 bit instruction word has an opcode, two registers operands and an immidiet operand. The number of bit available for the immediate operand field is

Sol No. of instruction = 40 — opcode bit
= $\log_2 40$ — bits = 6 bits

No. of Registers = 24 ⇒ registers = $\lceil \log_2 24 \rceil$ - bits
= 5-bits

← 32 bits →

opcode	Reg1 ~~Add~~	Reg2	immediate operand
6	5	5	16

Ans → 16-bits

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