MY CHOICE
Date:
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Questions on addressing modes Lecture 11

* Computable Modes :-

7 * Auto increment / Autodcrement mode
varient of register indicrect mode, in which the content of register is automatically increment or decrement to access the sequential data. → Table of data

Example : loops

200
Register

opcode	Mode	Add.

↓
Auto increment / decrement

Memory

Operand	200
Operand	201

Register will auto increment the add. to access the sequential data.
for excessing in rev we will use auto derement.

Auto inc => Post increment
Auto dec. => Pre drement
→ old / some particular microprocessor's architecture.

8 * Indexed or Indexd Register mode
→ used for access the element of an array

* Add. of operand is effective address

int a[5]

loc(A[i]) = Base + w * i

Memory

base add. ←	300
	302
	304
	306
	308

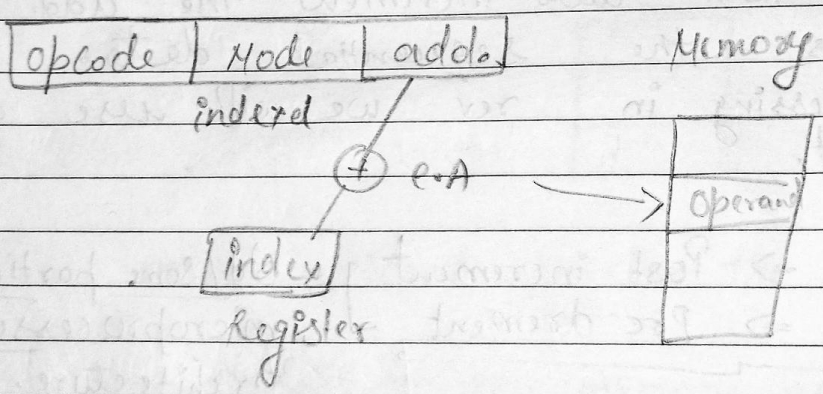
i = 3, w = size of each element

Compiler generates instruction

index Reg. = w * i

M[Base + index reg.]

we calculated the effective add. using = Base add. + index reg



effective add. = {Add. part of inst.} + {index Reg value}

{Add. part of inst.} → base add.

{index Reg value} → index

* One memory access required to get the operand.

* This addr. mode does not support relocation because of relocation then the base ~~add~~ addr. should be update in instruction

implementation of index reg

index reg

→ Special purpose reg

| opcode | mode | addr. |

→ g.p.r

| opcode | index reg identifier | mode | addr. |

* 9. PC - Relative mode

→ used for branch instruction

Memory

Assume, CPU is executing i2 instruction.

(PC) Program Counter = 202

Program

i2 is branch instruction

200	i1
201	i2
202	i3
203	i4
204	i5
205	i6
206	i7
207	i8
208	i9

True
Branch taken
Target instruction executed
PC = 207 (target addr.)

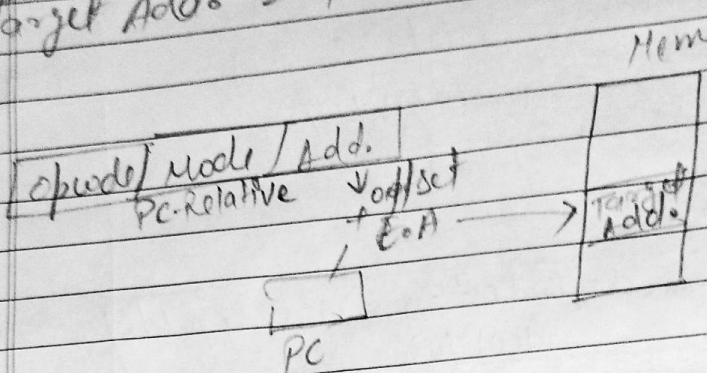
False
next in the sequence instruction
i2 executes
(Branch not taken)
x10 change in PC

i8 is target instruction

its add. is known as target add.

Target add. = P.C + no. of memory loc to skip

Target Add. = PC + 5 => 202 + 5 = 207



PC Relative mode

effective add = PC value + add. part value of instruction

PC

-> before fetch of i2 = 201
After fetch of i2 = 202

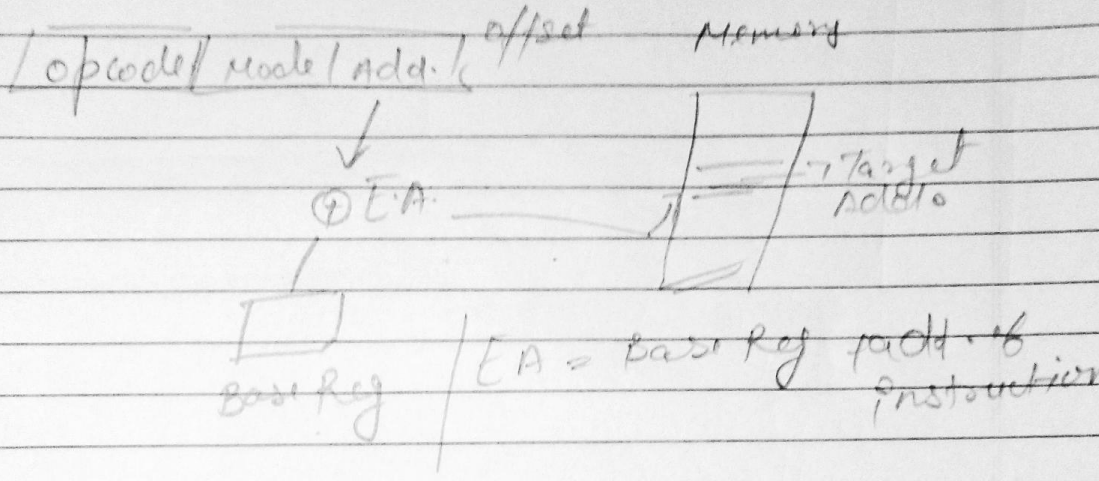
Decode => It's a branch instruction
E.A Calculation => E.A = 202 + 5 = 207

Execution => CPU check the Condition and updates the pc if Condition is true

* for forward jumpin offset +ve
for backword " -ve

* Intra-Segment branching

* Base Register Mode
used for inter-segment branching



PC-Relative mode is also know as position independent mode

PC Relative, Base Register mode → Supports Relocation

Both are used for Branching instruction
Rest are used to obtain operand or data