Aim ↬ To design and study the characteristics of CMOS NAND Gate.

Software Required ↬ Tanner EDA Tools [S-Edit, T-Spice].

Circuit Elements ↬ PMOS, NMOS, Voltage sources, connecting wires.

Theory ↬

A CMOS (Complementary Metal-Oxide-Semiconductor) NAND gate is a fundamental digital logic circuit composed of NMOS and PMOS transistors. It operates by combining the characteristics of a CMOS inverter with the logic functionality of a NAND gate. The output of a CMOS NAND gate is the complement of the AND operation on its inputs.

The circuit consists of:

1. **NMOS (N-type MOSFETs):** These transistors conduct when a positive voltage is applied to their gates. They are used parallel in the pull-down network to pull the output to logic '0'.
2. **PMOS (P-type MOSFETs):** These transistors conduct when their gates are at low voltage. They are used in series in the pull-up network to pull the output to logic '1'.

Operation:

1. **All Inputs High (Logic '1'):**
    - NMOS transistors are ON (conducting), forming a low-resistance path to the ground.
    - PMOS transistors are OFF (non-conducting), isolating the output from the power supply.
    - The output is pulled low (logic '0').
2. **At Least One Input Low (Logic '0'):**
    - At least one NMOS transistor is OFF, breaking the connection to the ground.
    - The PMOS transistors form a conducting path in series, pulling the output high (logic '1').

The complementary configuration ensures low static power dissipation, as only one network (pull-up or pull-down) conducts in a steady state. This efficiency,

combined with its reliability, makes CMOS NAND gates crucial in modern digital circuit design.

Circuit Diagram ↬

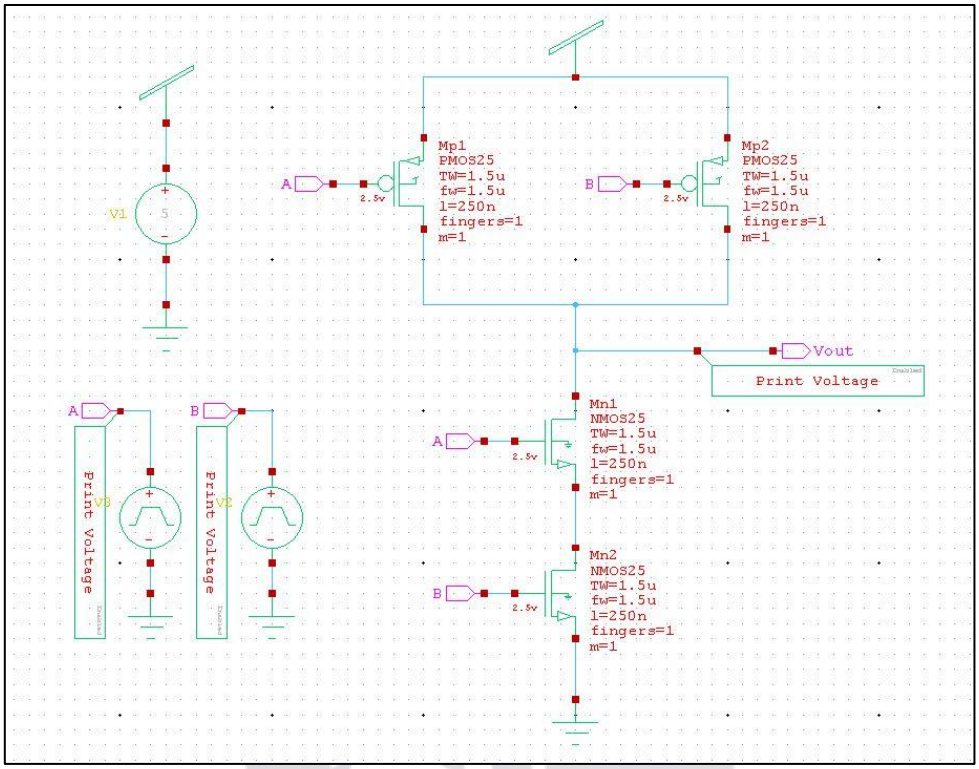

Fig. i) CMOS NAND Gate Circuit

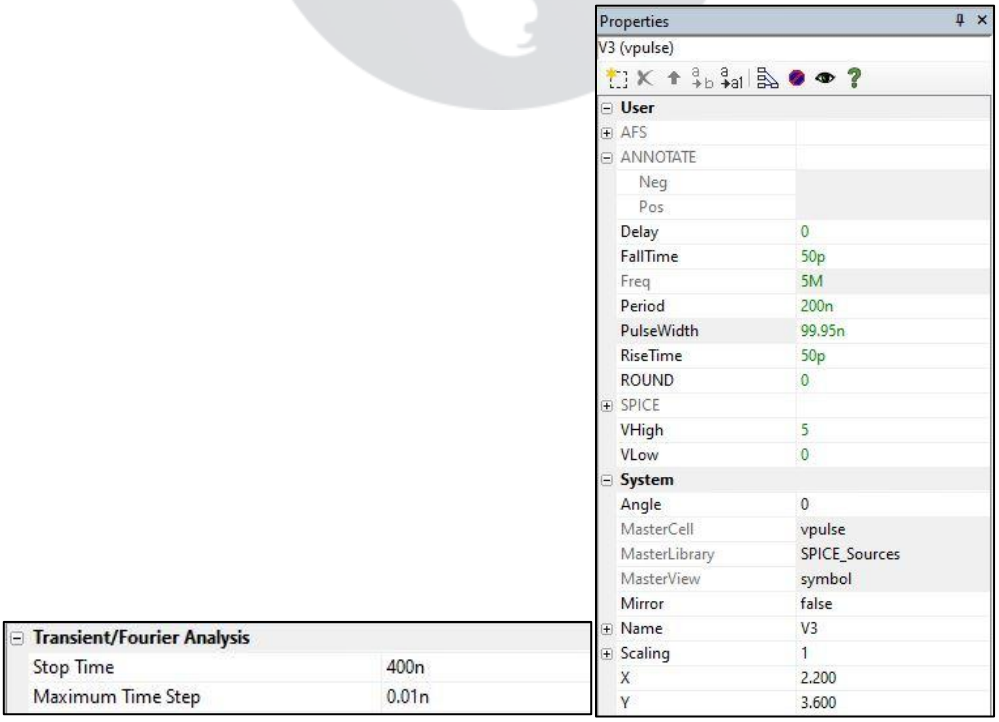

Fig. ii) Plot conditions and parameter setting

Graphs ↬

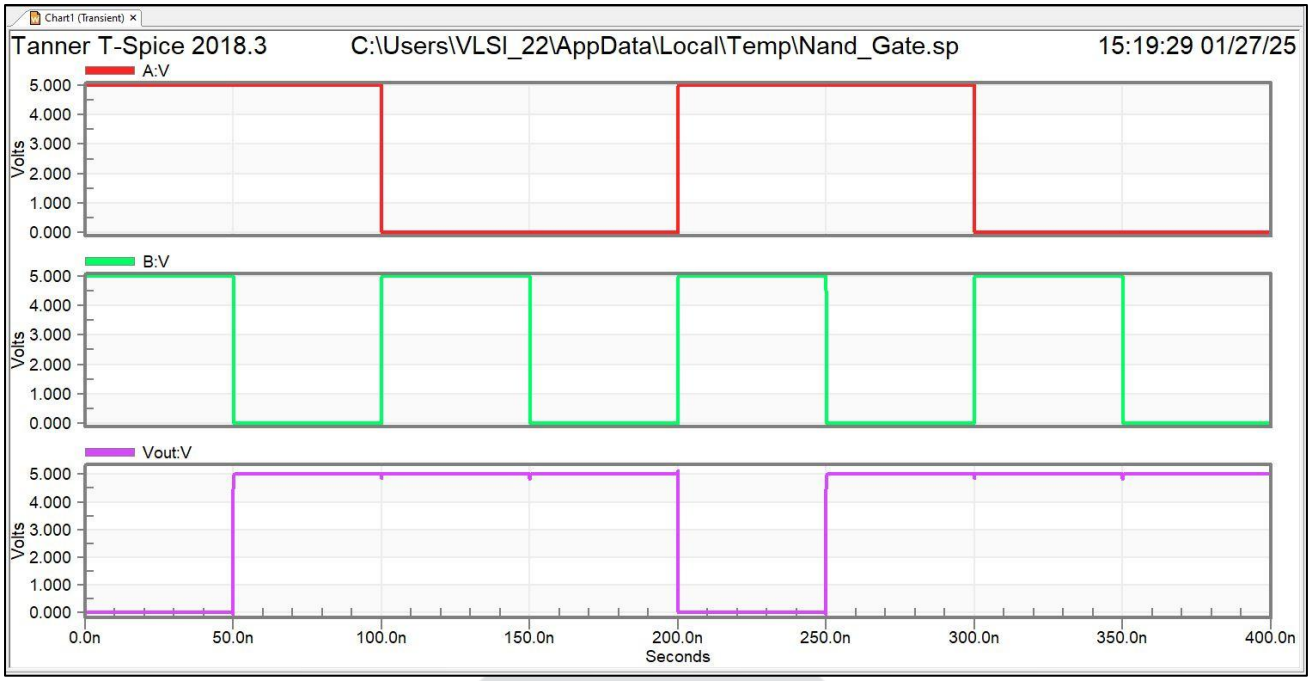

Fig. iii) Transient characteristics of CMOS NAND Gate

Result ↬

The experiment successfully demonstrated the characteristics of a CMOS NAND gate using Tanner EDA tools. The simulation confirmed proper NAND functionality, aligning with theoretical predictions.

Conclusion ↬

The CMOS NAND gate's transient behavior was analyzed, confirming efficient logic operation, minimal delay, and low static power dissipation. The experiment validated the NAND gate's theoretical design and practical significance in digital circuits.

Precautions ↬

- Double-check the orientation of NMOS and PMOS transistors in the circuit.
- Ensure all connections are correct and components are securely placed.
- Do not exceed the voltage ratings of components.