

Aim ⇨ To design and study the transient and DC characteristics of CMOS Inverter.

Software Required ⇨ Tanner EDA Tools [S-Edit, T-Spice].

Circuit Elements ⇨ PMOS, NMOS, Voltage sources, connecting wires.

Theory ⇨

A CMOS [Complementary Metal-Oxide-Semiconductor] inverter is a fundamental building block in digital circuit design. It is composed of an NMOS and a PMOS transistor. It operates as a logic inverter, producing an output voltage that is the complement of its input voltage. The operation of the CMOS inverter is based on the complementary switching of the NMOS and PMOS transistors.

- **NMOS (N-type MOSFET):** Conducts when a positive voltage is applied to its gate. It pulls the output to a logic '0' when active.
- **PMOS (P-type MOSFET):** Conducts when a negative voltage (or ground for typical designs) is applied to its gate. It pulls the output to a logic '1' when active.

In a CMOS inverter:

- When the input is low (logic '0'), the PMOS is ON, and the NMOS is OFF. The output is pulled high (logic '1').
- When the input is high (logic '1'), the NMOS is ON, and the PMOS is OFF. The output is pulled low (logic '0').

The operation regions of the NMOS and PMOS transistors play a crucial role in understanding the transient and DC characteristics of the CMOS inverter:

1. Cutoff Region:

- NMOS: $V_{GS} < V_{th} \rightarrow I_D = 0$
- PMOS: $V_{GS} < |V_{th}| \rightarrow I_D = 0$

Both transistors are off in this region.

2. Linear Region:

- NMOS: $V_{GS} > V_{th}$ and $V_{DS} < V_{GS} - V_{th}$
$$I_D = k_n [2(V_{GS} - V_{th})V_{DS} - V_{DS}^2]$$
- PMOS: $V_{GS} > |V_{th}|$ and $V_{SD} < V_{SG} - V_{th}$
$$I_D = k_p [2(V_{SG} - |V_{th}|)V_{SD} - V_{SD}^2]$$

3. Saturation Region:

- NMOS: $V_{DS} \geq V_{GS} - V_{th}$

$$I_D = k_n [V_{GS} - V_{th}]^2$$

- PMOS: $V_{SD} \geq V_{SG} - |V_{th}|$

$$I_D = k_p [V_{SG} - |V_{th}|]^2$$

Here, the transistors operate as constant current sources.

In the CMOS inverter, the transient response represents how quickly the circuit responds to changes in input, while the DC characteristics reveal the steady-state voltage transfer curve (VTC). The VTC defines the relationship between the input and output voltages, highlighting the switching threshold and noise margins.

The complementary structure ensures low static power dissipation, as only one transistor conducts during steady-state operation. This makes CMOS inverters highly efficient and suitable for modern digital circuits.

Circuit Diagram ↔

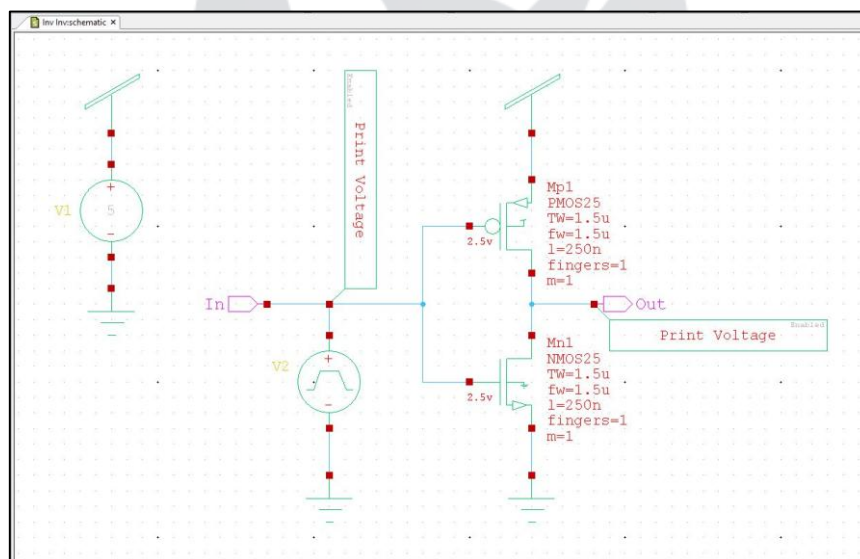


Fig. i) CMOS Inverter Circuit

DC Sweep Analysis		Transient/Fourier Analysis	
Source 1 (swept for each value of Source 2)		Stop Time	400n
Source or Parameter Name	VV2	Maximum Time Step	0.01n
Start Value/List of Points	-5	Print Start Time	0n
Stop Value	5	Print Time Step	
Step/Number of Points	0.01	Use Initial Conditions	False
Sweep Type	lin	Startup Mode	Op

Fig. ii) Plot conditions and parameter setting

Graphs ↔

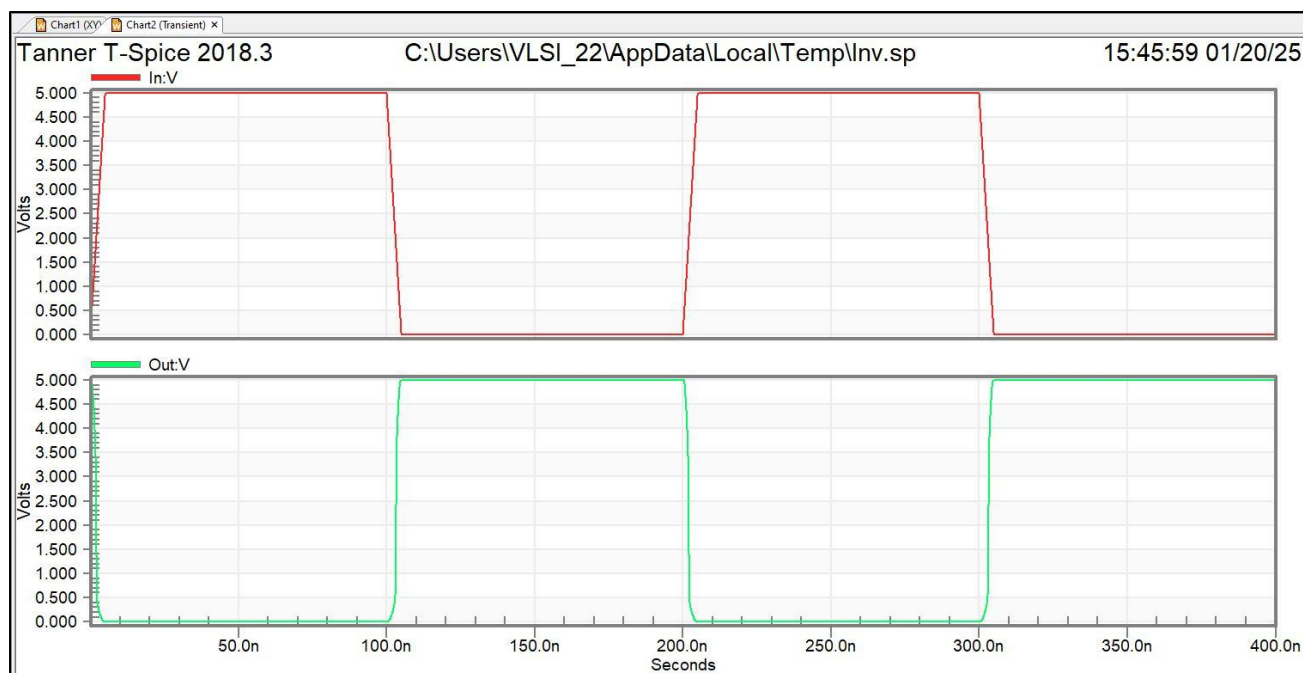


Fig. iii) Transient characteristics of CMOS Inverter

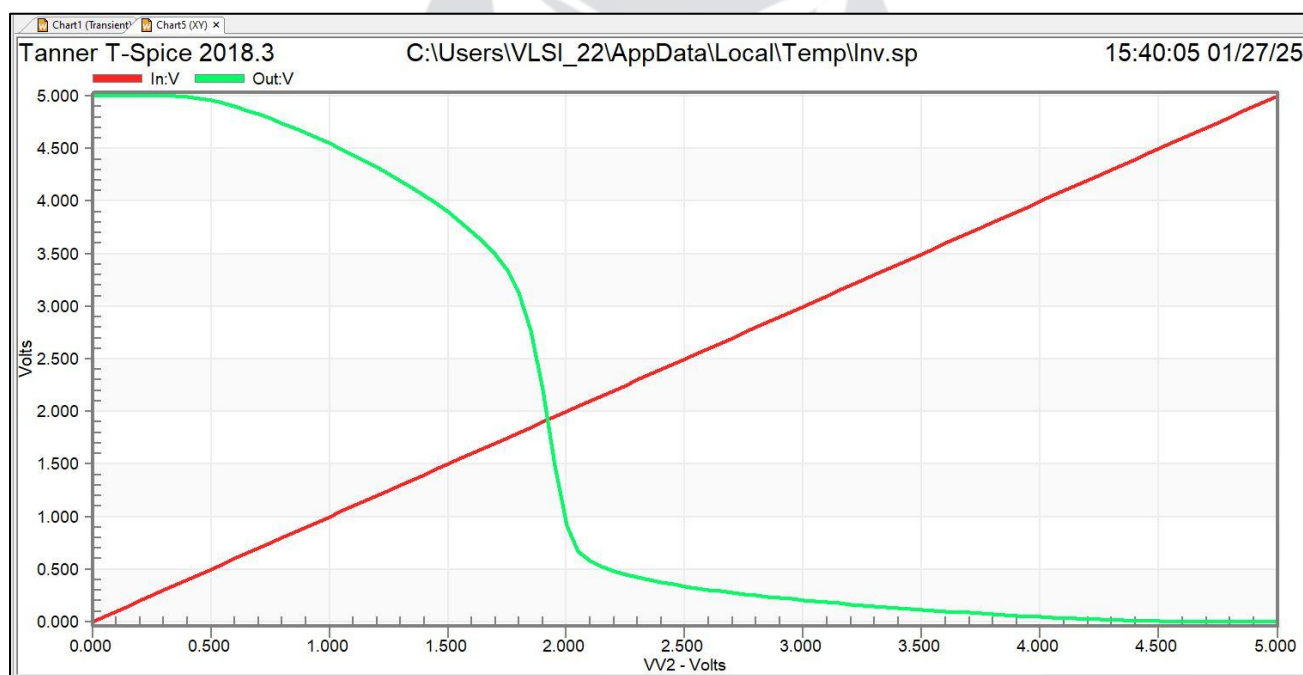


Fig. iv) DC characteristics of CMOS Inverter for $\frac{(W/L)_p}{(W/L)_n} = 1$

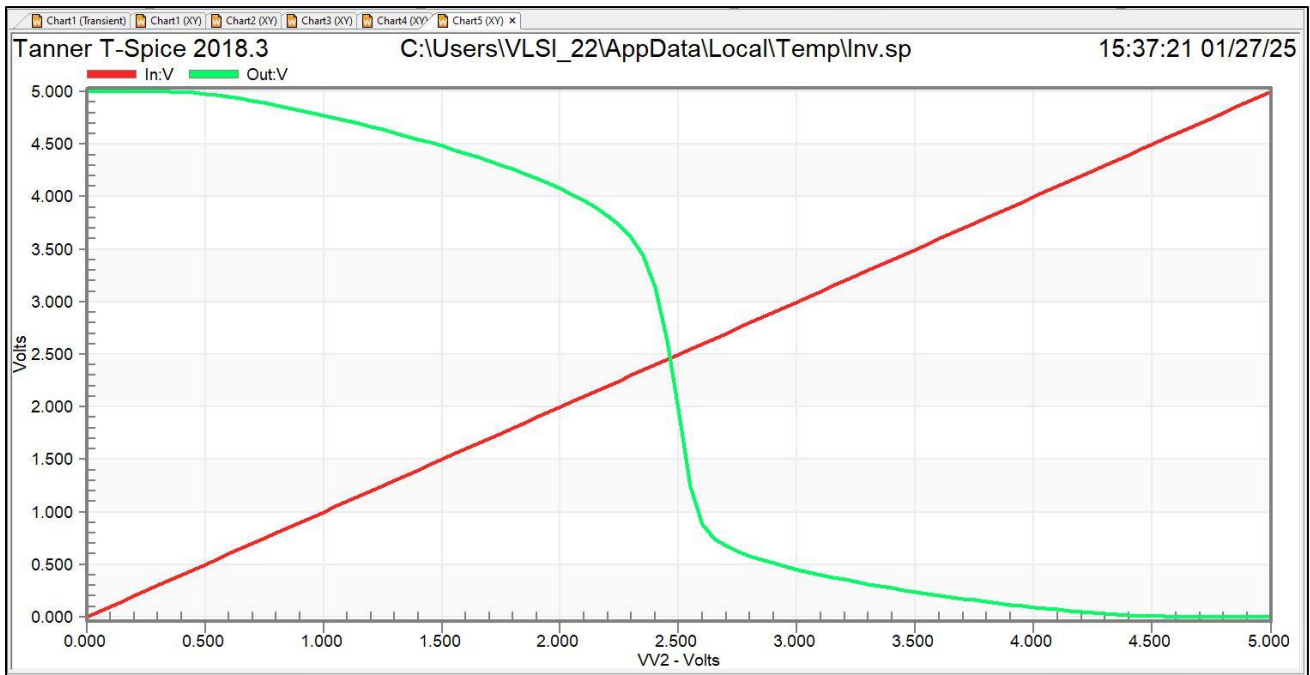


Fig. v) DC characteristics of CMOS Inverter for $\frac{(W/L)_p}{(W/L)_n} = 2$

Result ⇨

The experiment successfully demonstrated the transient and DC characteristics of a CMOS inverter using Tanner EDA tools. The simulation confirmed complementary switching, fast transitions, and the expected Voltage Transfer Characteristics (VTC), aligning with theoretical predictions.

Conclusion ⇨

The CMOS inverter's transient and DC behavior were analyzed, confirming efficient switching, minimal delay, and low static power dissipation. The experiment validated the inverter's theoretical design and practical significance in digital circuits.

Precautions ⇨

- Double-check the orientation of NMOS and PMOS transistors in the circuit.
- Ensure all connections are correct and components are securely placed.
- Do not exceed the voltage ratings of components.