**Aim ↬ To design and study the characteristics of CMOS XNOR Gate.**

**Software Required ↬** Tanner EDA Tools [S-Edit, T-Spice].

**Circuit Elements ↬** PMOS, NMOS, Voltage sources, connecting wires.

**Theory ↬**

A CMOS XNOR gate is a fundamental digital logic circuit composed of NMOS and PMOS transistors. Unlike simple logic gates such as NAND or NOR, an XOR gate requires a combination of multiple transistors to implement its function. The XNOR gate outputs a high signal (logic '1') when both inputs are the same (either both high or both low).

The circuit consists of:

- **NMOS (N-type MOSFETs):** These transistors conduct when a positive voltage is applied to gates. They are used in the PDN to pull the output to logic '0'.
- **PMOS (P-type MOSFETs):** These transistors conduct when their gates are at low voltage. They are used in the PUN to pull the output to logic '1'.

**Operation ↴**

1. **Both Inputs Low (Logic '0') or Both Inputs High (Logic '1'):**
    - NMOS transistors are OFF, isolating the output from the ground.
    - PMOS transistors conduct, forming a low-resistance path to VDD, pulling the output high (logic '1').
2. **One Input High (Logic '1'), One Input Low (Logic '0'):**
    - The transistor network forms a conducting path such that the output is pulled low (logic '0').

Unlike basic gates such as NAND and NOR, which require only four transistors, a CMOS XNOR gate typically requires more transistors due to its more complex function. Despite this, the CMOS configuration ensures low static power dissipation, as only one network (pull-up or pull-down) conducts in a steady state.

**Boolean Expression ↴**

$$A\ XNOR\ B = \overline{AB} + AB$$

## Truth Table ↴

| A | B | $V_0$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## Procedure ↬

i. Create a New Project in S-Edit and set up the workspace.

ii. Place the required PMOS and NMOS transistors in the XNOR configuration.

iii. Connect VDD to the PMOS source and GND to the NMOS source.

iv. Apply inputs (A, B) to transistor gates and connect drains for output ($V_0$).

v. Set Up Voltage Sources for power (VDD) and inputs (0V/VDD).

vi. Export Netlist from S-Edit and open it in T-Spice.

vii. Set up the transient analysis parameters.

viii. Run Simulation and view results in W-Edit.

## Circuit Diagram ↬

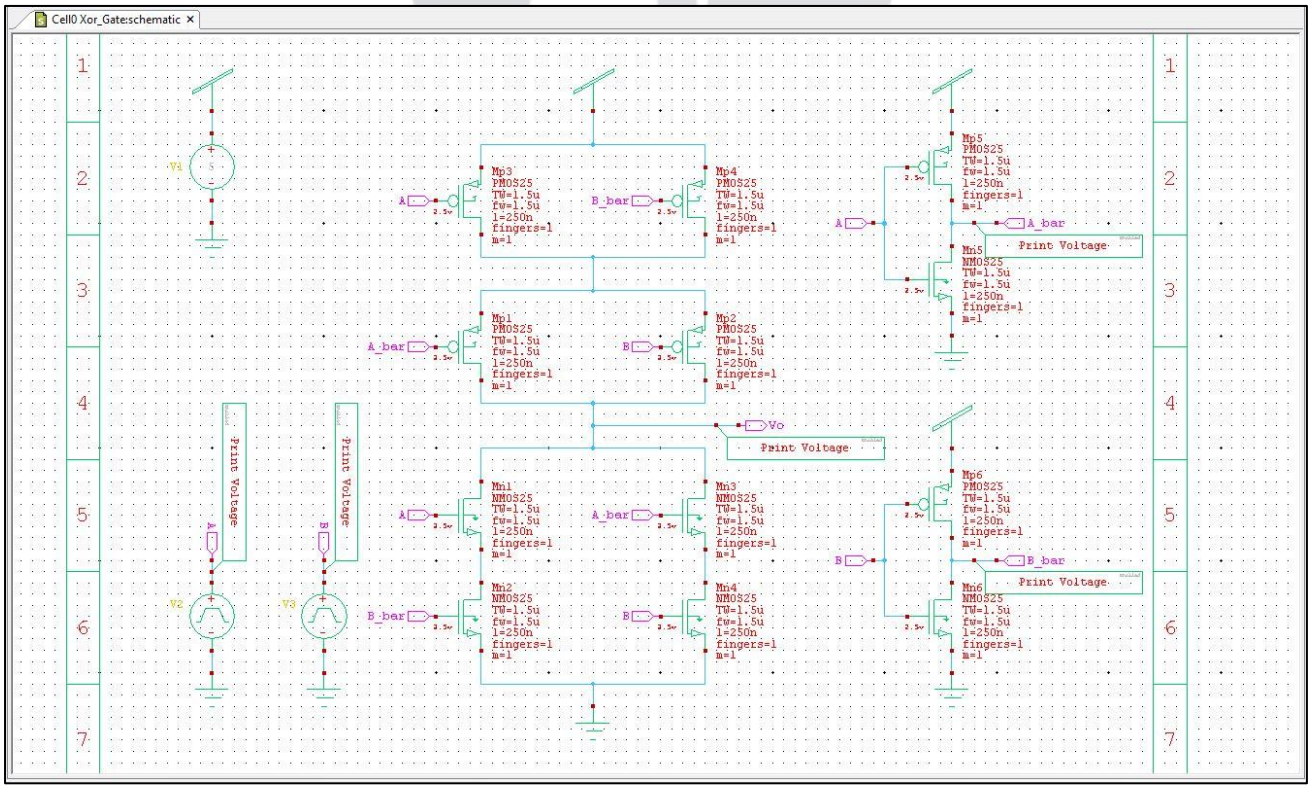


Fig. i) CMOS XNOR Gate Circuit

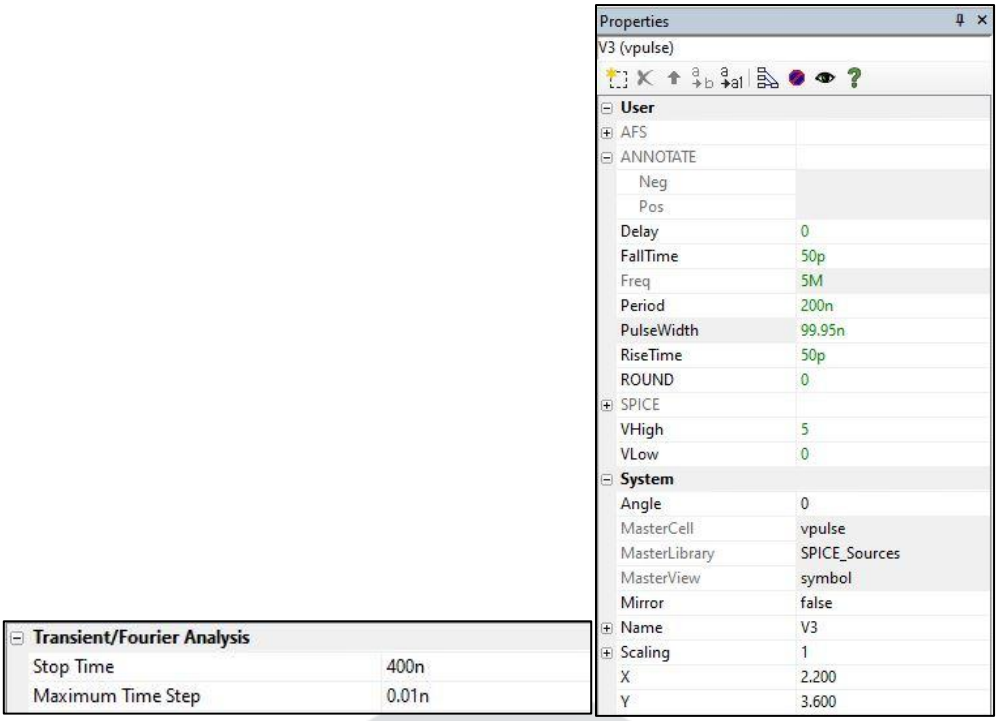


Fig. ii) Plot conditions and parameter setting

## Graphs ↬

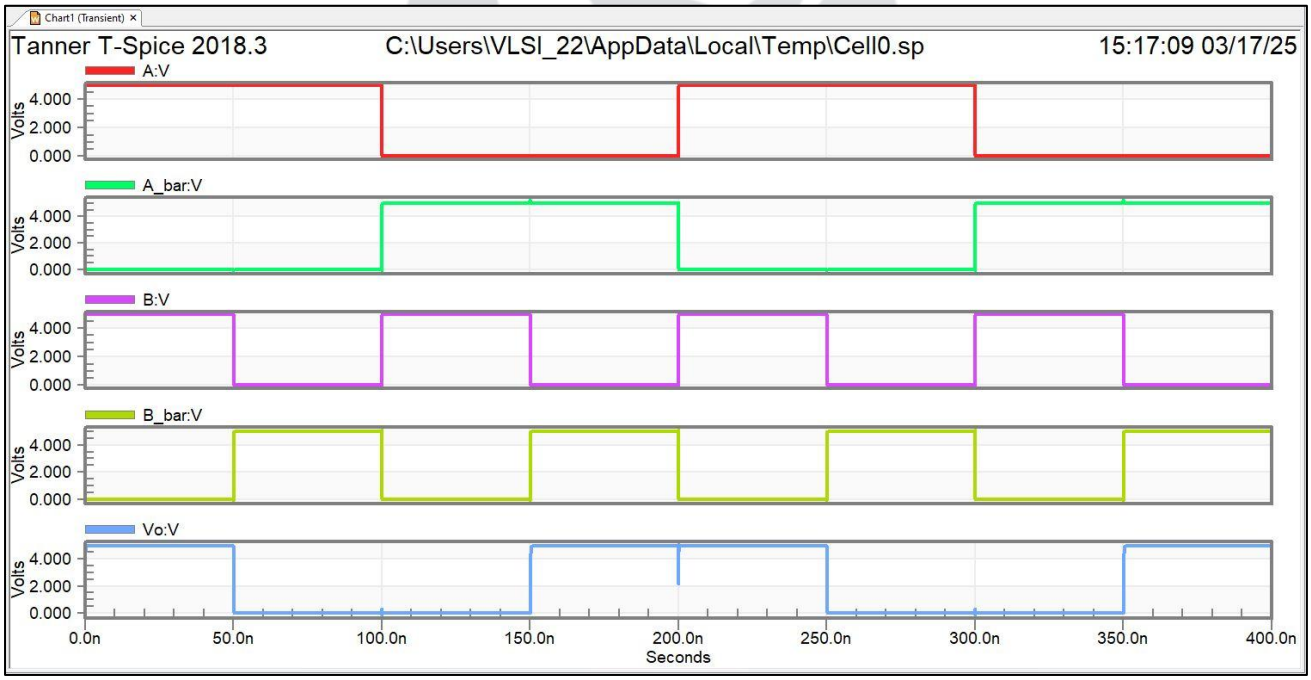


Fig. iii) Transient characteristics of CMOS XNOR Gate

## Result ↬

The experiment successfully demonstrated the characteristics of a CMOS XNOR gate using Tanner EDA tools. The simulation confirmed proper XNOR functionality, aligning with theoretical predictions.

## Conclusion ↬

The CMOS XNOR gate's transient behavior was analyzed, confirming efficient logic operation, minimal delay, and low static power dissipation. The experiment validated the XNOR gate's theoretical design and practical significance in digital circuits.

## Precautions ↬

- Double-check the orientation of NMOS and PMOS transistors in the circuit.
- Ensure all connections are correct and components are securely placed.
- Do not exceed the voltage ratings of components.