Aim ↬ To design and study the characteristics of CMOS NOR Gate.

Software Required ↬ Tanner EDA Tools [S-Edit, T-Spice].

Circuit Elements ↬ PMOS, NMOS, Voltage sources, connecting wires.

Theory ↬

A CMOS NOR gate is a fundamental digital logic circuit composed of NMOS and PMOS transistors. It operates by combining the characteristics of a CMOS inverter with the logic functionality of a NOR gate. The output of a CMOS NOR gate is the complement of the OR operation on its inputs.

The circuit consists of:

1. **NMOS (N-type MOSFETs)**: These transistors conduct when a positive voltage is applied to their gates. They are used in series in the pull-down network to pull the output to logic '0'.
2. **PMOS (P-type MOSFETs)**: These transistors conduct when their gates are at low voltage. They are used in parallel in the pull-up network to pull the output to logic '1'.

Operation ↴

1. **All Inputs Low (Logic '0'):**
    - NMOS transistors are OFF (non-conducting), isolating the output from the ground.
    - PMOS transistors are ON (conducting), forming a low-resistance path to the power supply pulling the output high (logic '1').
2. **At Least One Input High (Logic '1'):**
    - At least one NMOS transistor is ON, forming a conducting path to the ground pulling the output low (logic '0').
    - The PMOS transistors are OFF, breaking the connection to the power supply.

The complementary configuration ensures low static power dissipation, as only one network (pull-up or pull-down) conducts in a steady state. This efficiency, combined with its reliability, makes CMOS NOR gates crucial in modern digital circuit design.

Boolean Expression ↴

$$A\ NOR\ B = \overline{A + B} = \overline{A}.\overline{B}$$

Truth Table ↴

A	B	V_0
0	0	0
0	1	0
1	0	0
1	1	1

Procedure ↬

i. Create a New Project in S-Edit and set up the workspace.

ii. Place two PMOS (parallel) and two NMOS (series) transistors.

iii. Connect VDD to the PMOS source and GND to the NMOS source.

iv. Apply inputs (A, B) to transistor gates and connect drains for output (V_0).

v. Set Up Voltage Sources for power (VDD) and inputs (0V/VDD).

vi. Export Netlist from S-Edit and open it in T-Spice.

vii. Set up the transient analysis parameters.

viii. Run Simulation and view results in W-Edit.

Circuit Diagram ↬

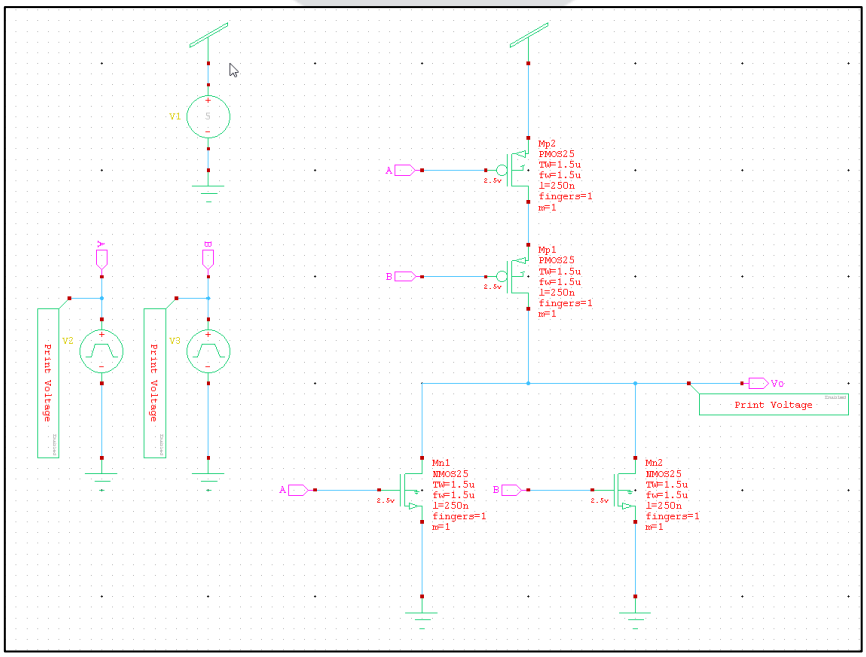

Fig. i) CMOS NOR Gate Circuit

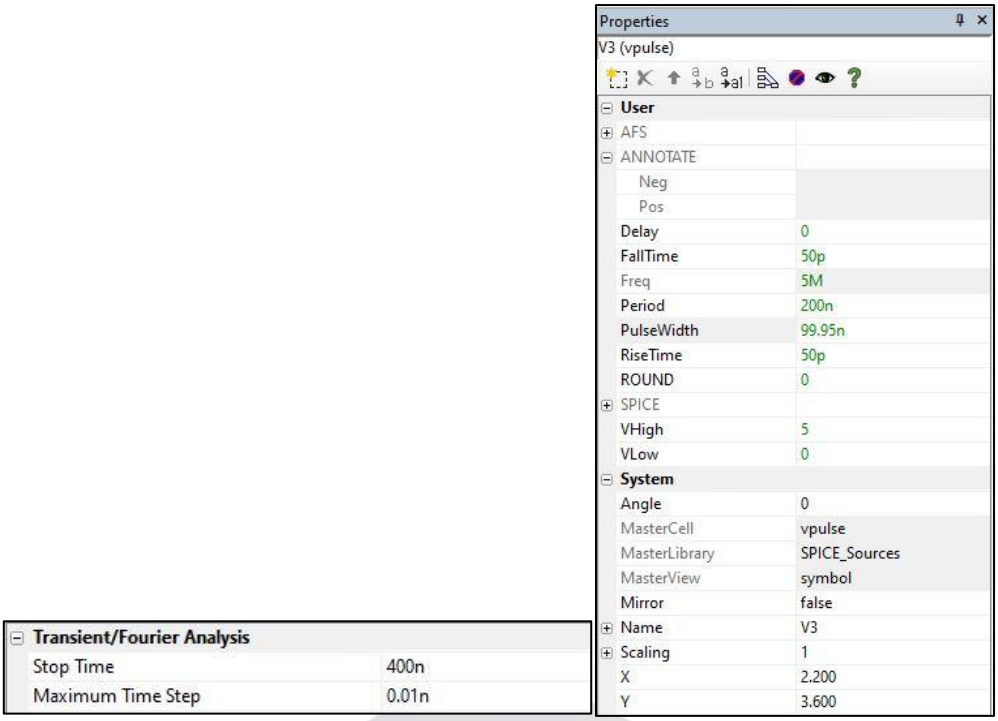

Fig. ii) Plot conditions and parameter setting

Graphs ↬

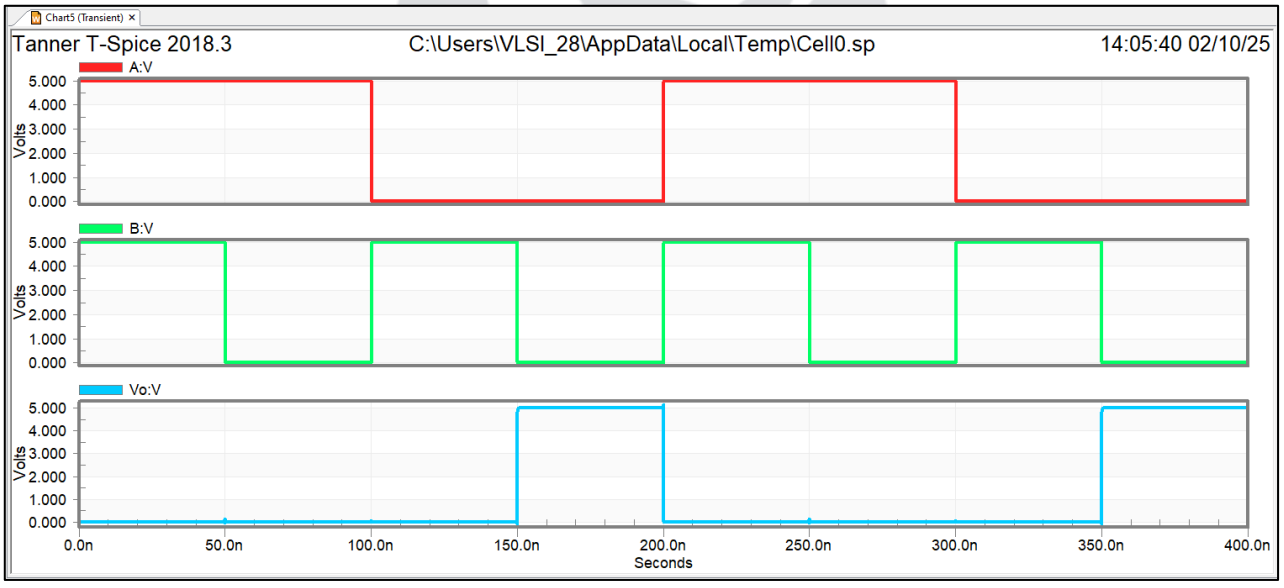

Fig. iii) Transient characteristics of CMOS NOR Gate

Result ↬

The experiment successfully demonstrated the characteristics of a CMOS NOR gate using Tanner EDA tools. The simulation confirmed proper NOR functionality, aligning with theoretical predictions.

Conclusion ↬

The CMOS NOR gate's transient behavior was analyzed, confirming efficient logic operation, minimal delay, and low static power dissipation. The experiment validated the NOR gate's theoretical design and practical significance in digital circuits.

Precautions ↬

- Double-check the orientation of NMOS and PMOS transistors in the circuit.
- Ensure all connections are correct and components are securely placed.
- Do not exceed the voltage ratings of components.