LAB PROGRAMS

LEVEL-0:

- Design and implement all basic gates in data-flow and behavioralmodeling.
- Design and implement F.A, HA in data-flow and structural modeling.
- Design and implement Multiplexer using conditional statement.
- Design and implement 3:8 decoders.
- Design and implement 4:2 encoders.
- Design and implement Even Parity & Odd parity generator.

LEVEL-1:

- Design and implement Priority Encoder.
- Design and implement Or, And, Xor gate using Multiplexer (2×1).
- Design and implement 4-bit adder/sub using structural.
- Design and implement 4-bit CLAA.
- Design and implement a Swap/Buffer circuit using multiplexer.
- Design and implement 8:3encoder.

LEVEL-2:

- Design and implement JK-FlipFlop,D-FlipFlopand T-FlipFlop.
- Design and implement a system which takes 4-bit data and shifts left,right, reverses, passes the data depending upon a control signal(Don't use any registers).
- Design and implement a 4-bit Counter
- Design and implement a system which takes 8-bit data and stores in memory and based on request it should send data ROM/ RAM.

LEVEL-3:

- 1. Write the hardware description of a 4-bit PRBS (pseudo-random Binary
- sequence) generator using a linear feedback shift register and test it.?
- 2. Write the hardware description of a 8-bit register with shift left and shift right
- modes of operation based on selection line and write its test operation?

- 3. Write a program for universal shift register?
- 4. write a program for universal synchronous counter which includes up , down and updown counter?
- 5. write a program for universal asynchronous counter which includes up , down and updown counter?
- 6. Write the hardware description of a 4-bit mod-13 counter and test it.?
- 7. write a program for synchronous fifo for 32 locations depth and 16 bit data size?
- 8. design and implement asynchronous fifo with write clock 512 mhz and read clock 64 mhz?(hint: calculate the fifo depth and proceed)