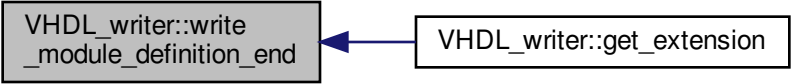


VHDL_writer::write
_module_definition_end



```
graph LR; A[VHDL_writer::get_extension] --> B[VHDL_writer::write_module_definition_end]
```

The diagram consists of two rectangular boxes. The box on the left is shaded gray and contains the text 'VHDL_writer::write' on the first line and '_module_definition_end' on the second line. The box on the right is white with a black border and contains the text 'VHDL_writer::get_extension'. A dark blue arrow points from the right side of the white box to the left side of the gray box.

VHDL_writer::get_extension