

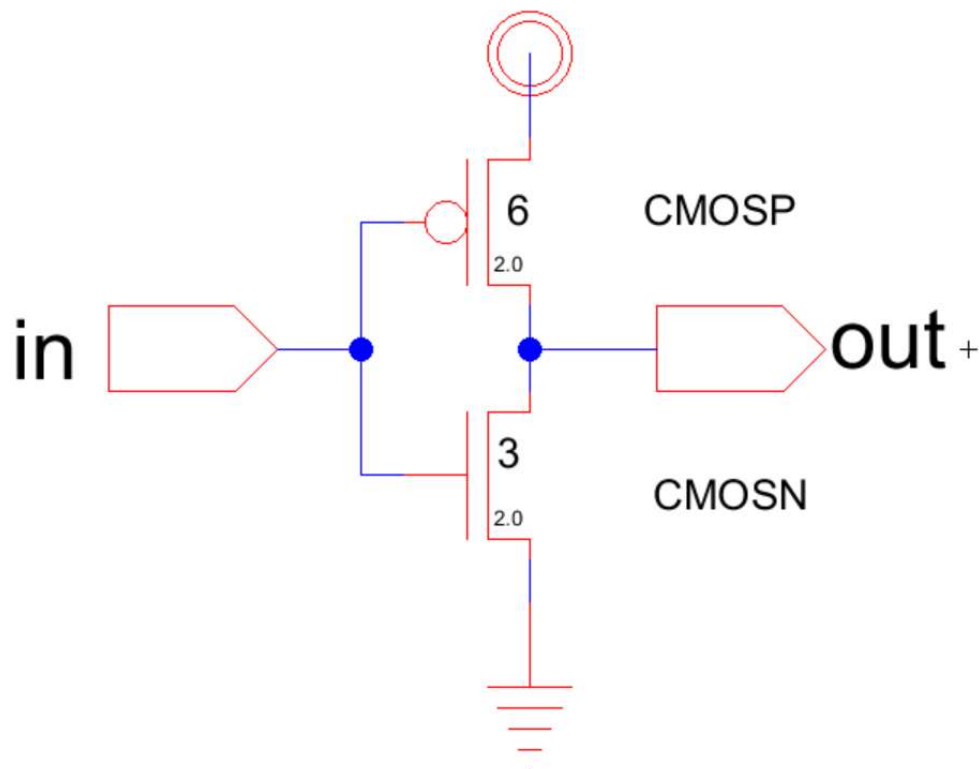
## ASSIGNMENT 2

29 September 2021 22:18

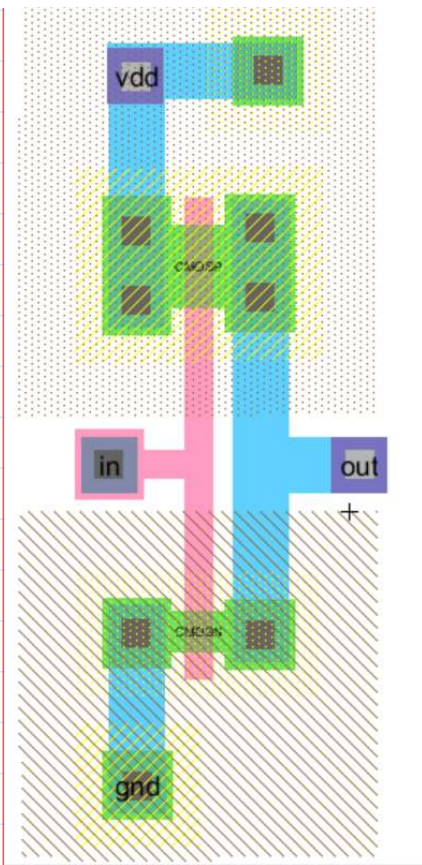
Technology taken for the below circuits is 180nm. ( $\lambda = 90\text{nm}$ )

### Inverter

#### Schematic:



#### Layout:



All the regions are at the best possible distance.

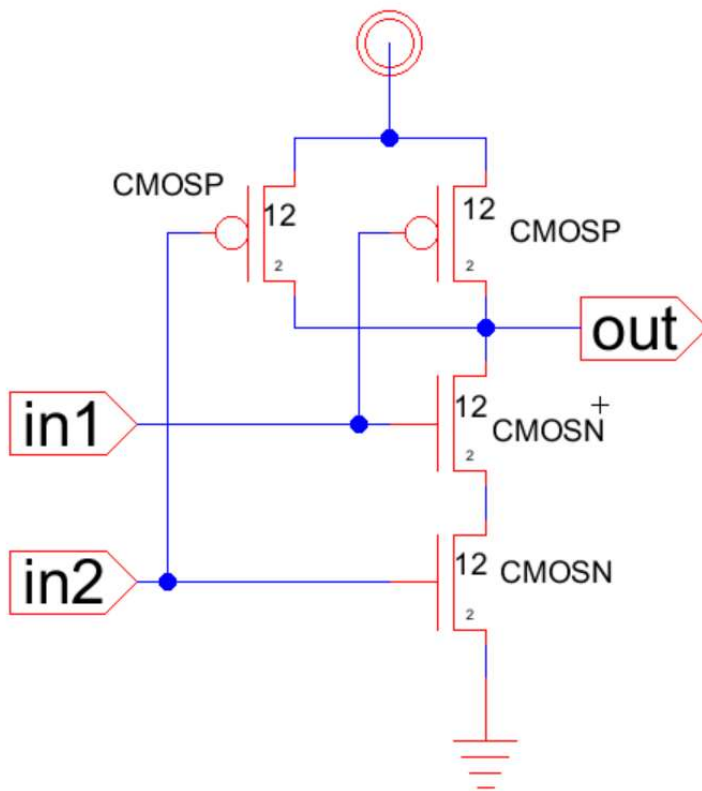
The above circuit is designed for minimum area as shown in the figure above. This minimum size has been used as reference to design all the other circuits below.

Results are shown below for inverter:

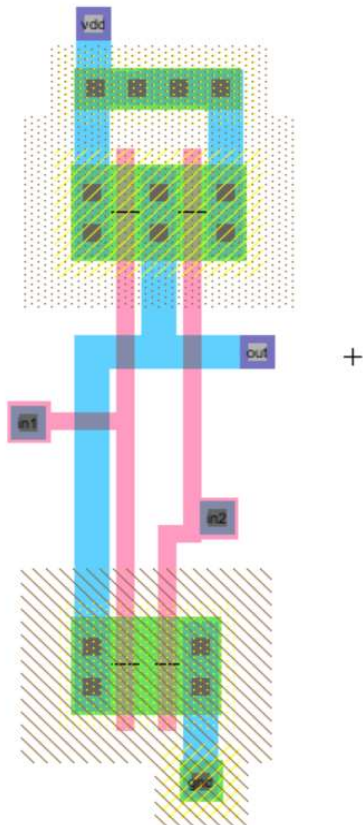
CIRCUIT	Td(seconds)
Inverter (sch)	7.01891e-010
Inverter (layout)	7.49893e-010

NAND 2 input

Schematic :



Layout:



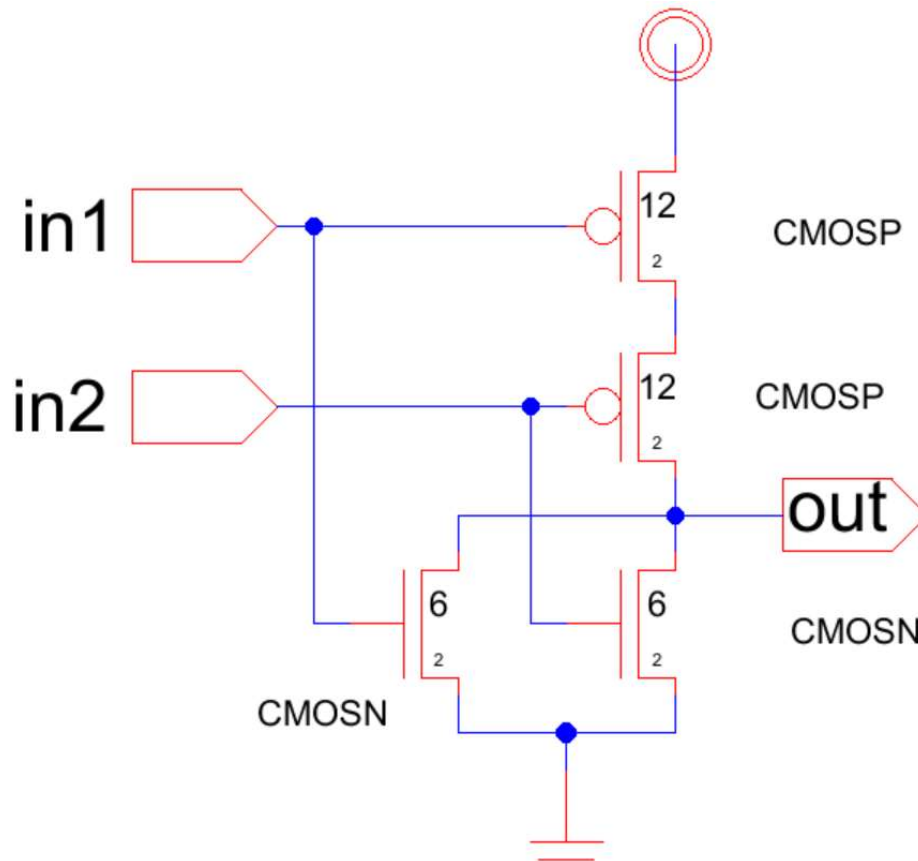
NOTE: Analysis using schematic for minimum length is taken (different from the schematic diagram)

CIRCUIT	I/P 1	I/P 2	Td(seconds)
NAND (sch)	0	0	1.54522e-010
	0	1	7.77857e-010
	1	0	7.60379e-010
	1	1	1.247e-010

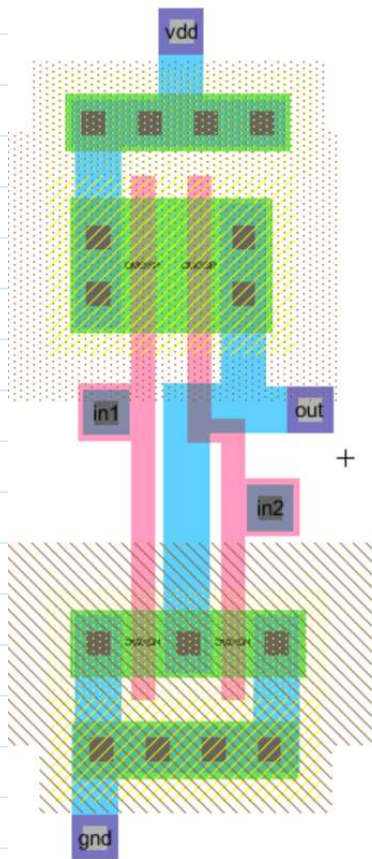
CIRCUIT	I/P 1	I/P 2	Td(seconds)
NAND (layout)	0	0	8.79535e-011
	0	1	7.21629e-010
	1	0	9.5027e-010
	1	1	2.66554e-010

## NOR 2 INPUT GATE

### SCHEMATIC



### LAYOUT:



NOTE: Analysis using schematic for minimum length is taken (different from the schematic diagram)

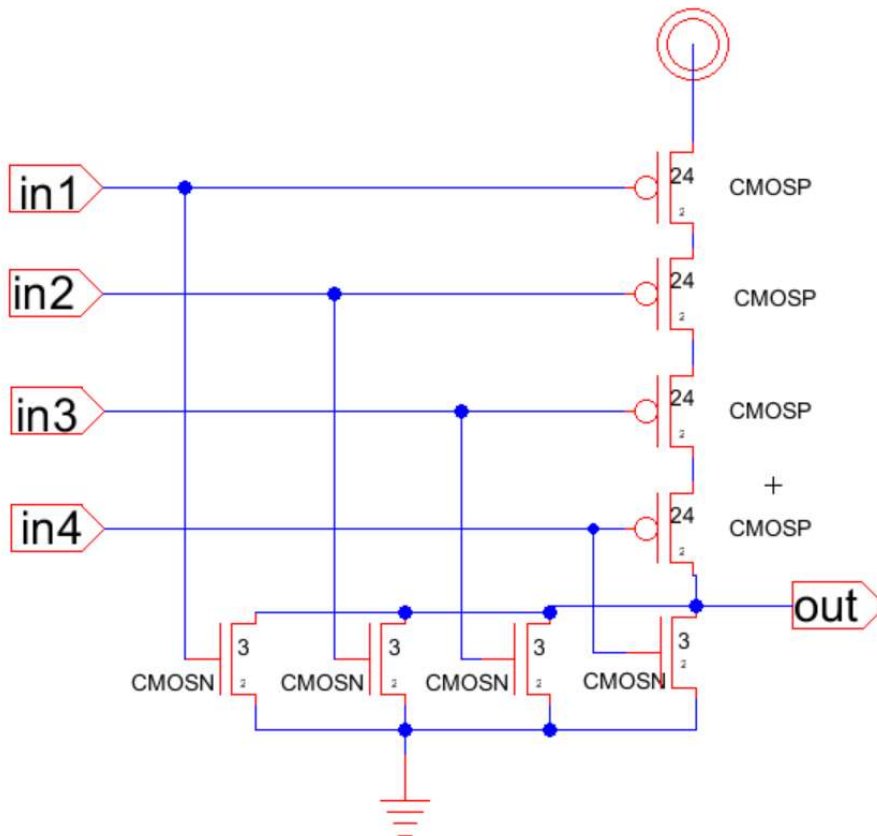
CIRCUIT	I/P 1	I/P 2	Td(seconds)
NOR (SCH)	0	0	1.40172e-009
	0	1	3.60906e-010
	1	0	1.6072e-010
	1	1	1.34256e-009

CIRCUIT	I/P 1	I/P 2	Td(seconds)
NOR (layout)	0	0	3.67139e-010
	0	1	4.01579e-010

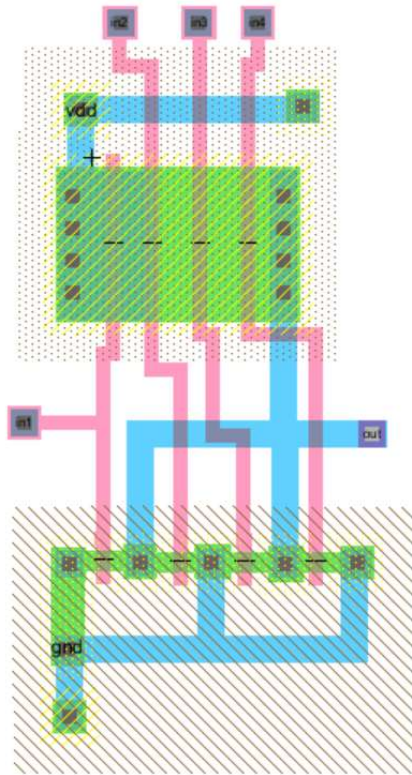
	1	0	9.10093e-011
	1	1	1.23129e-009

## NOR GATE 4 input

Schematic:



LAYOUT



Observation made for different inputs combination for LAYOUT configuration:

lp1	lp2	lp3	lp4	Td
0	0	0	0	1.48808e-010
1	1	1	1	1.48799e-009
1	1	0	0	5.77738e-010

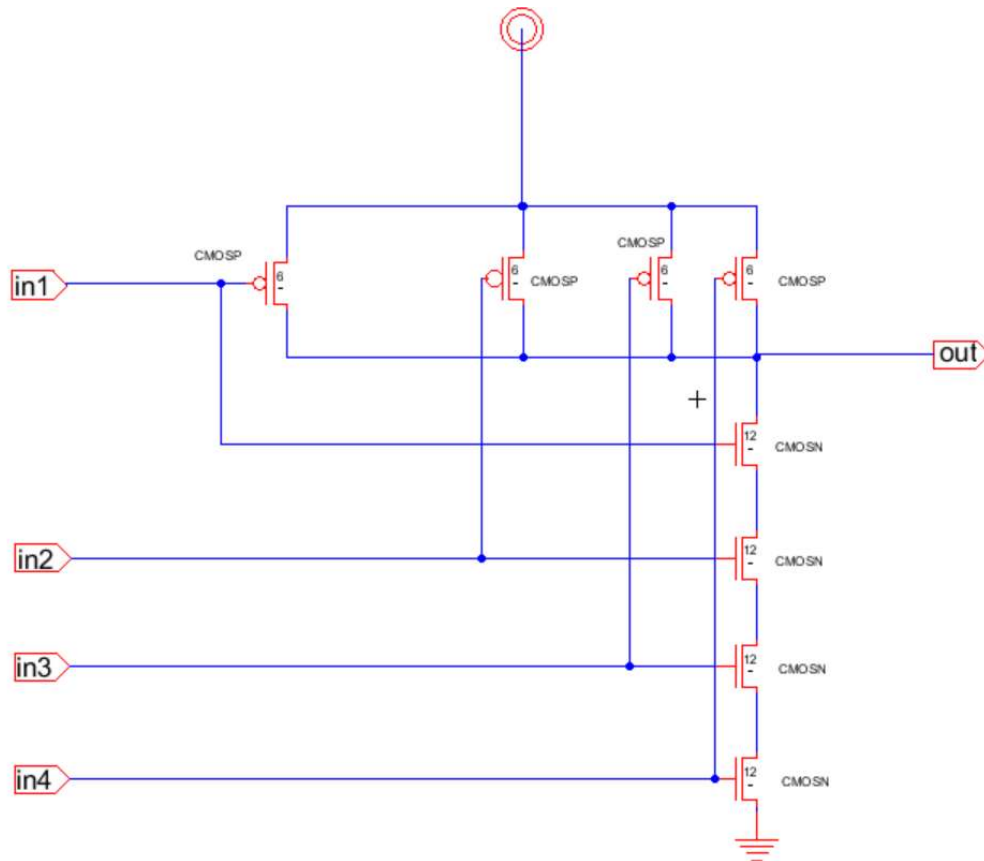
Observation made for different inputs combination for schematic configuration:

lp1	lp2	lp3	lp4	Td
0	0	0	0	1.07831e-009
1	1	1	1	1.48799e-009
1	1	0	0	7.07489e-010

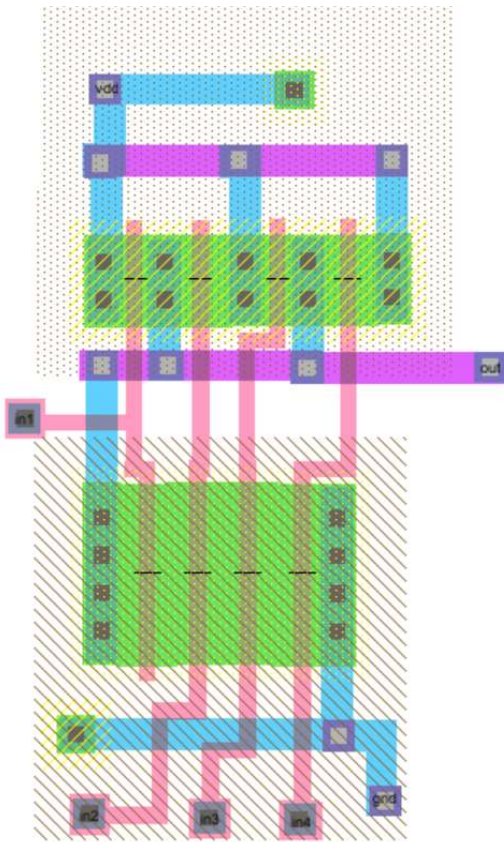


## NAND 4 INPUT

### SCHEMATIC:



### LAYOUT:



Observation made for different inputs combination for LAYOUT configuration:

lp1	lp2	lp3	lp4	Td
1	1	0	1	1.41346e-009
1	1	1	1	7.72191e-010
0	1	1	1	9.85027e-010

Observation made for different inputs combination for SCHEMATIC configuration:

lp1	lp2	lp3	lp4	Td
1	1	0	1	1.27739e-009
1	1	1	1	6.50626e-010
0	1	1	1	9.41722e-010

