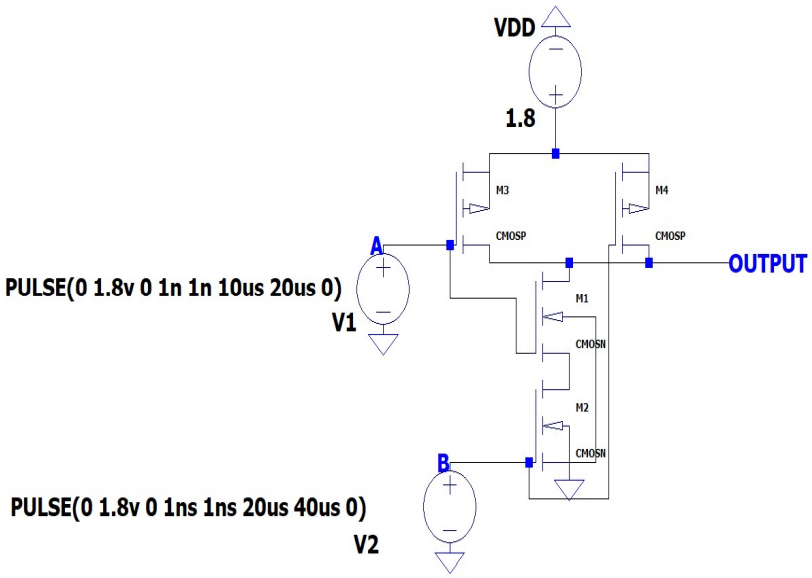
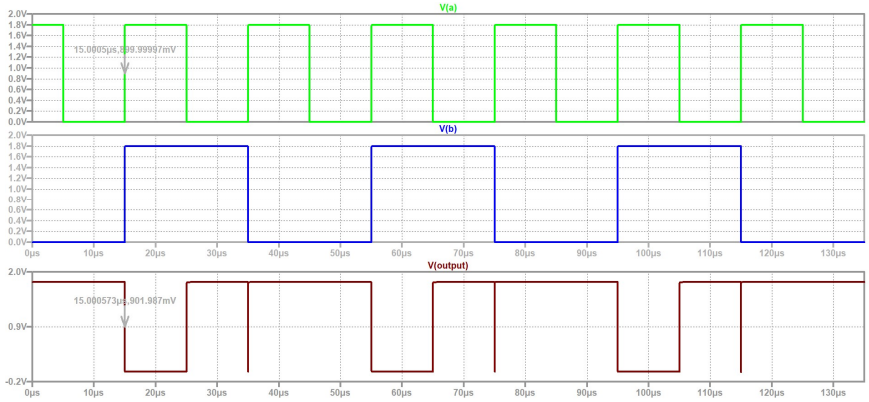
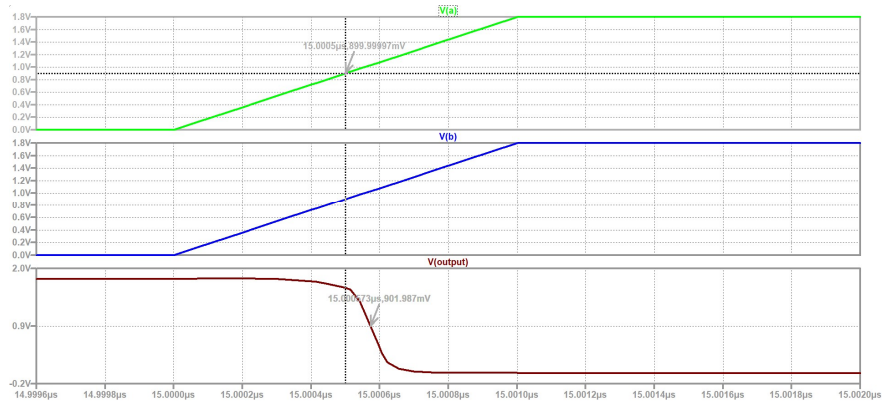
.INCLUDE tsmc018.lib
.INCLUDE TSMC018.LIB
.tran 0 200us 65us

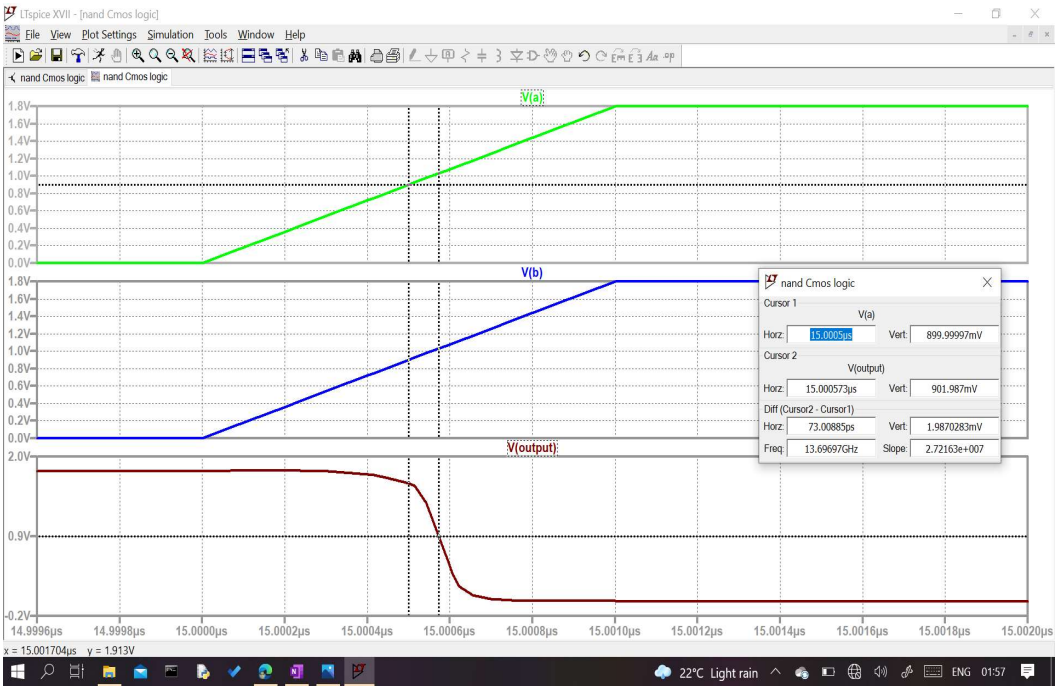


The Waveforms for NAND logic are displayed as below:

1. Without load
For Both input High and output 0 the delay is calculated:

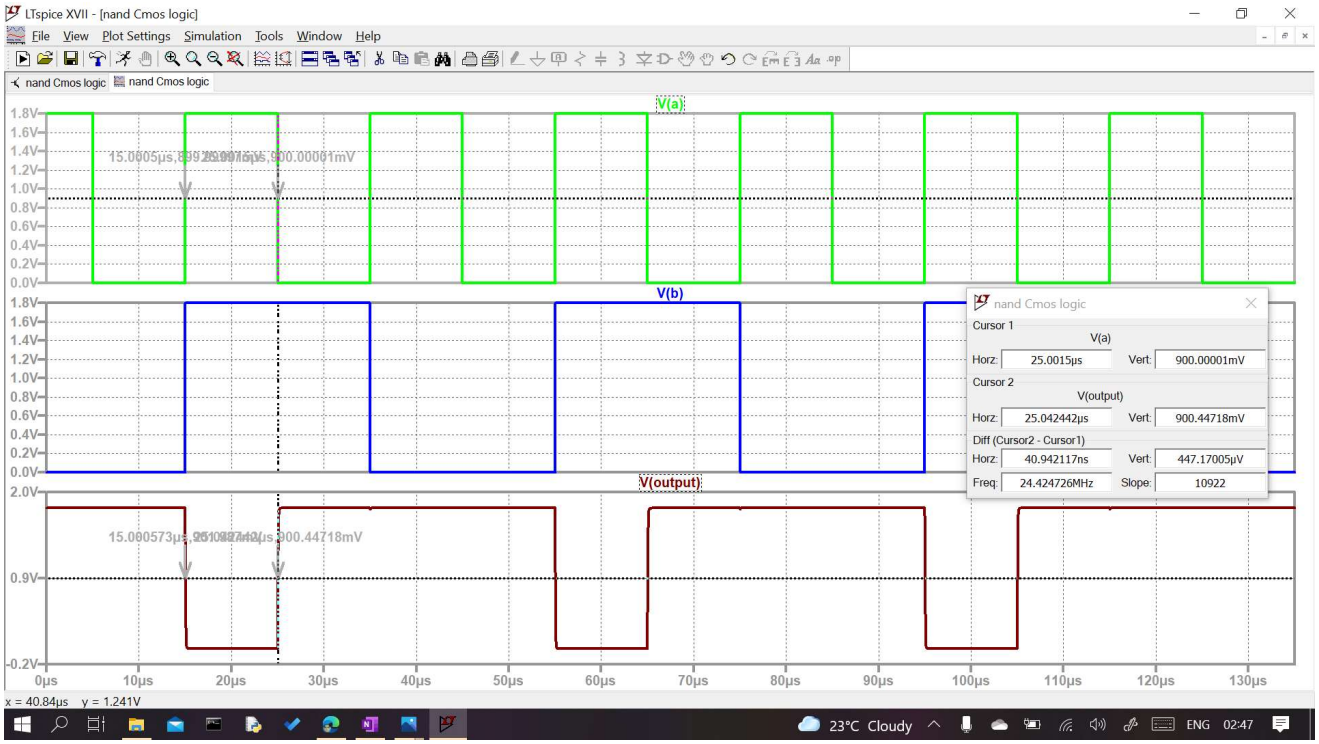


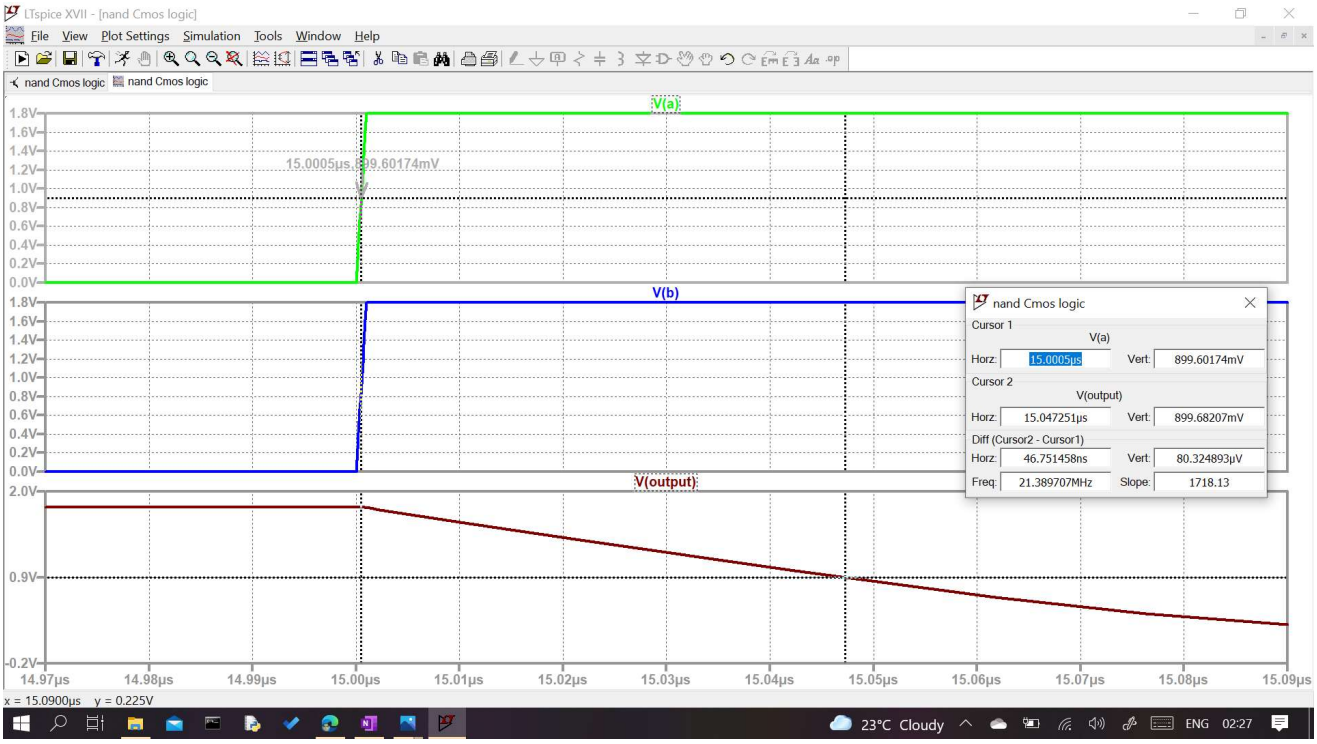




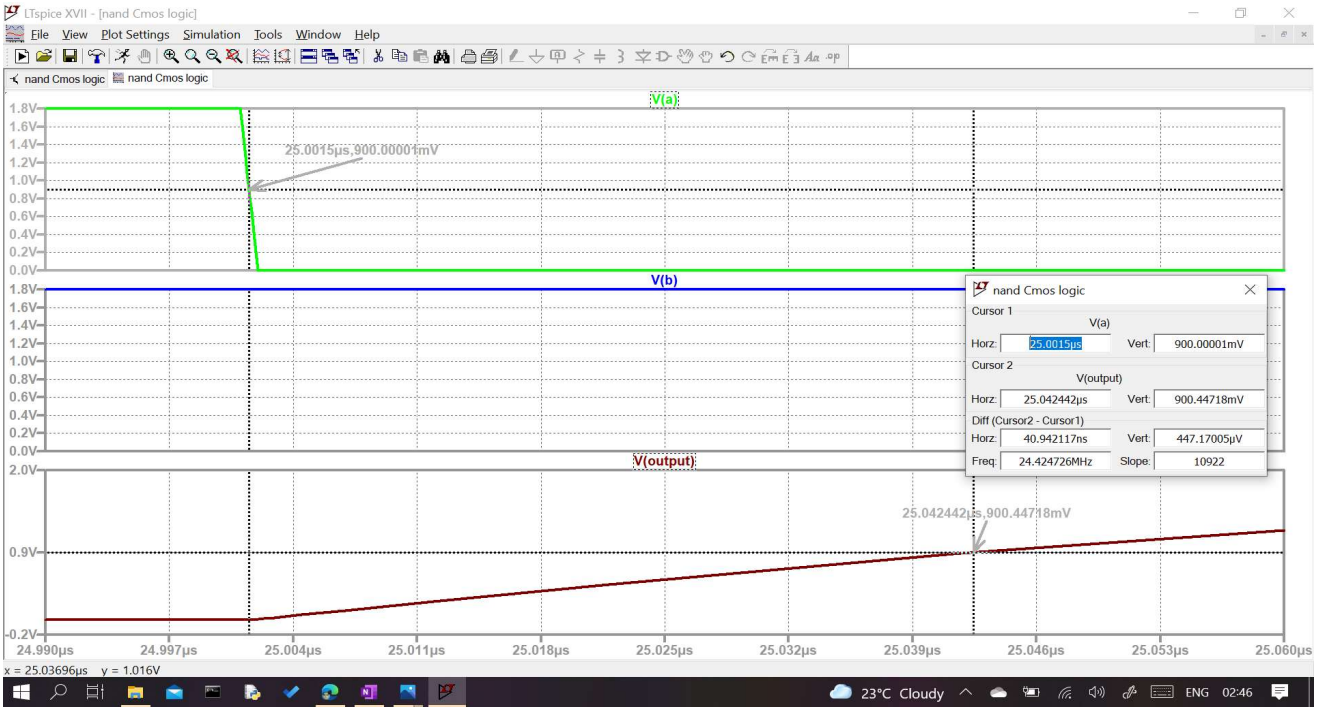
From the above delay is 73.00885ps for output ZERO and input Both High this is without load.

Wit C Load





With C load 10pf :
For output Zero With the input being Both High Delay is : 46.751ns



Input A	Input B	Output	Without load Delay	With Load Delay
High(1)	High (1)	Low(0)	73.00885 ps	46.751ns
Low(0)	High(1)	High(1)	60 ps	40.924 ns

We can observe that the Delay is different for Different input combination.