Assignment: Design and Simulate the schematic and corresponding optimized layout of an inverter chain with optimized number of inverters to get the minimum delay for a load capacitance of 100 fF.

To find the number of stages

$D = N F^{1/N} + P$ [$P = N$ for N no of stages]

Differentiating with respect to N

$\frac{\partial D}{\partial N} = 0$ we get

$-F^{1/N} \ln F^{1/N} + F^{1/N} + P_{inv} = 0$

$P_{inv} + f(1 - \ln f) = 0$

Solving further we get

$f^{1/N} = 2.718$ — ①

$f = G_{MB} = \frac{100fF}{C_{ingate}}$ — ②

Input Gate Calculation:

from TSMC Data sheet we get $\omega_x = 8.58 \times 10^{-3}$

NMOS $C_{gate} = 8.58 \times 10^{-3} \times 270n \times 180n$ [NMOS, $\omega = 270nm$, $L = 180nm$]

$= 0.43fF$

$C_{gate_p} = 8.58 \times 10^{-3} \times 180n \times 5u$

$= 0.83\,fF$

$C_{gate} = 1.26\,fF$

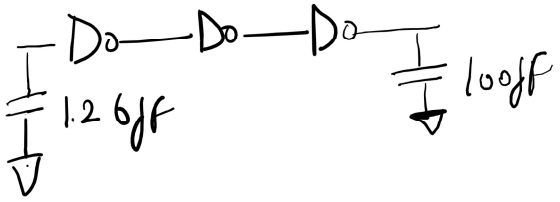
from equation (2)

$F = 79.36$

using in equation (1)

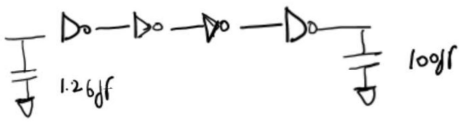
$N = 3.98$

for 3 stages



$D_3 = 15.89$

for N = 4 Stages:



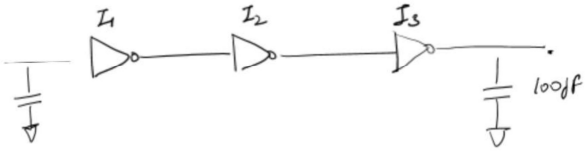
$D_4 = 15.938$

$D_3 < D_4$ → So Three Stages will give the optimum Results.

Since Now we know that there are Three Stages we can Calculate for the best Stage effort

Best Stage effort: $\sqrt[3]{79.31} = 4.29$

$D_3 = 15.85$



$C_{in_i} = \frac{C_{out} \times g_i}{f}$

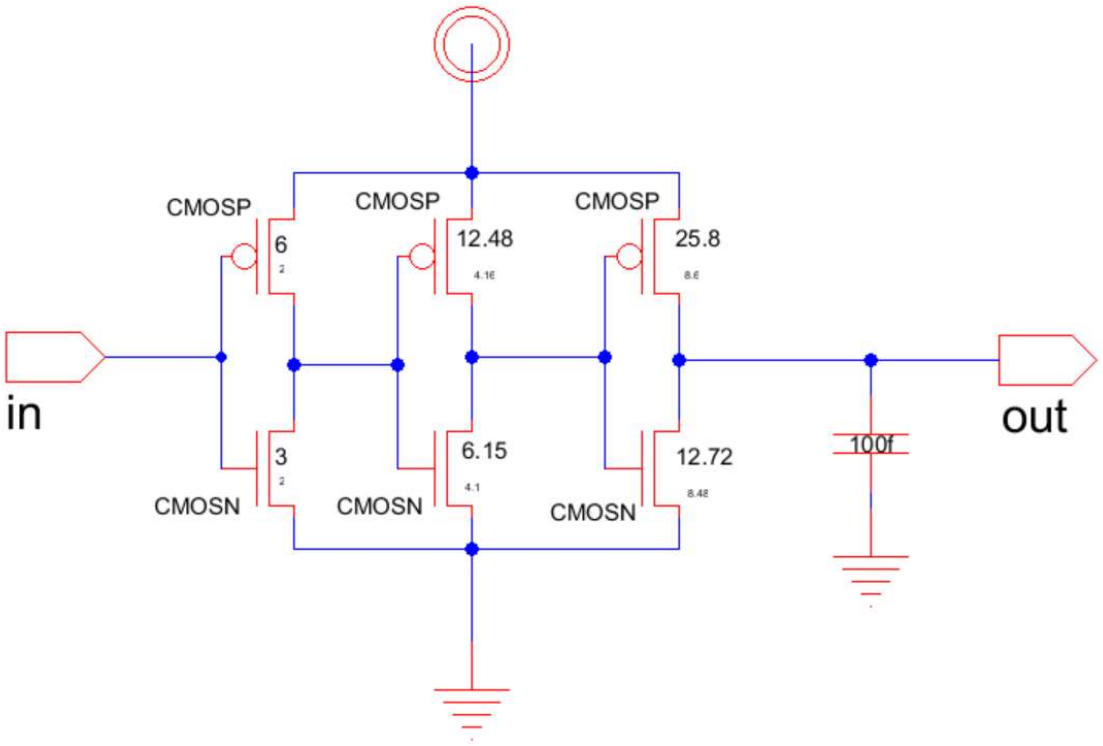
$C_{in_3} = 23.3fF$

$C_{in_2} = 5.43fF$

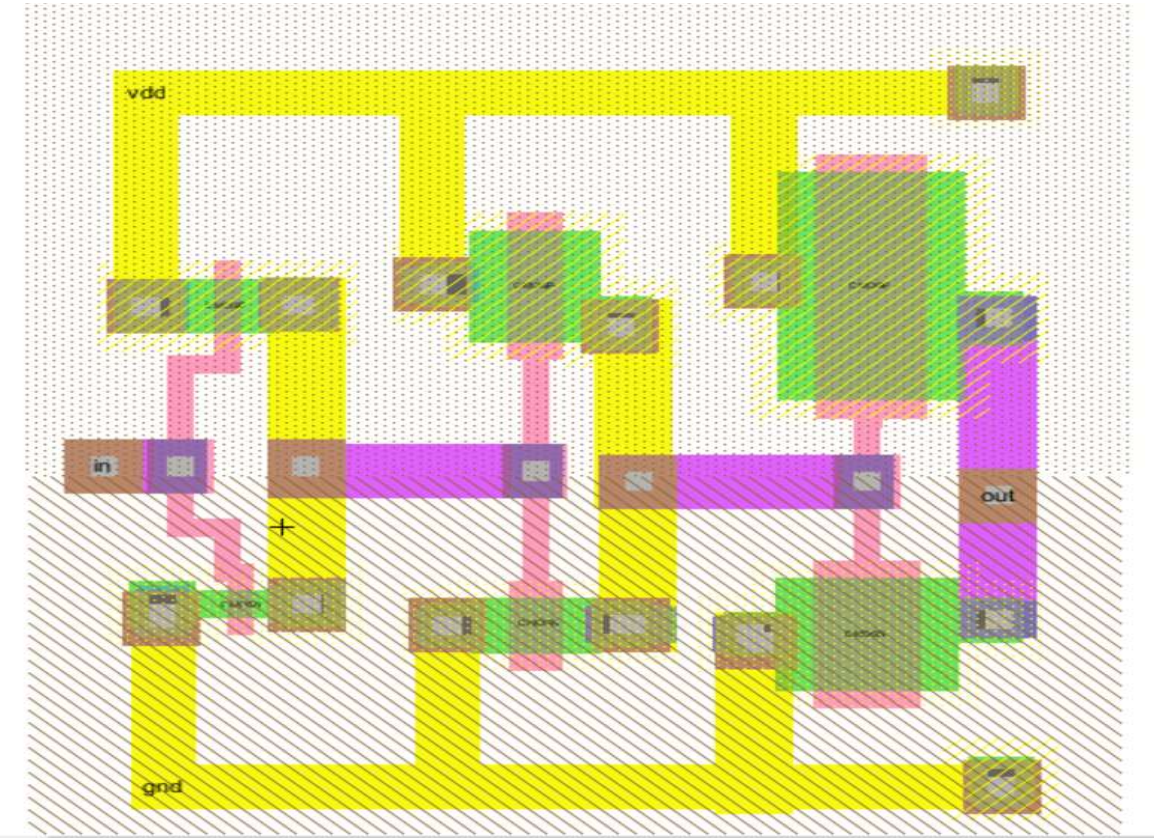
$C_{in_1} = 1.26fF$

According to these the size of the inverter will be changed

SCHEMATIC



LAYOUT



OBSERVATION MADE:

CIRCUIT	DELAY(SECONDS)
SINGLE INVERTER (SCHEMATIC, CL=100fF)	2.82834e-009
INVERTER CHAIN(SCHEMATIC, CL=100fF)	1.21055e-009
INVERTER CHAIN(LAYOUT)	1.75892e-010

We can clearly observe that the Delay has reduced significantly upon increasing the stages to an optimum level as calculated above.