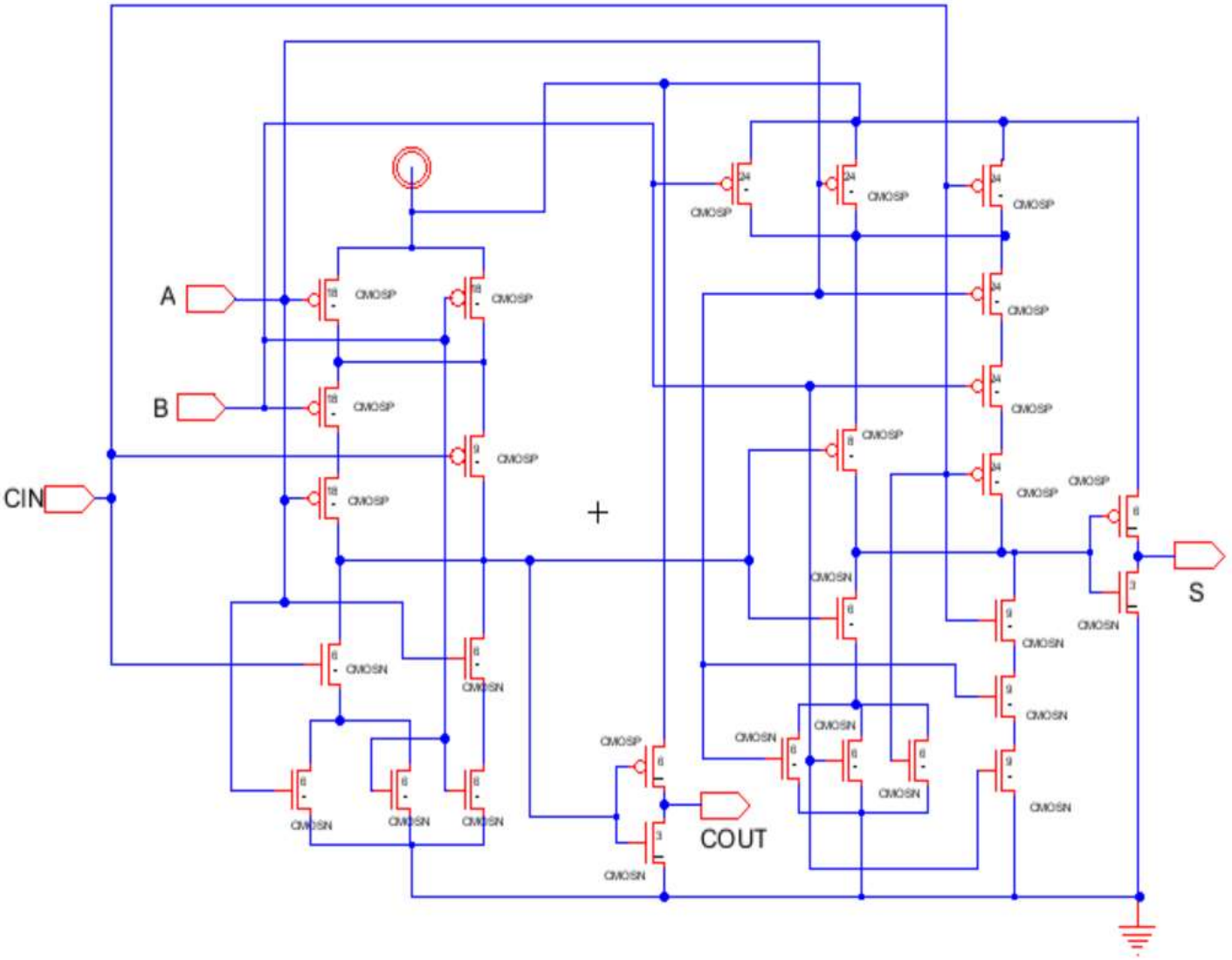
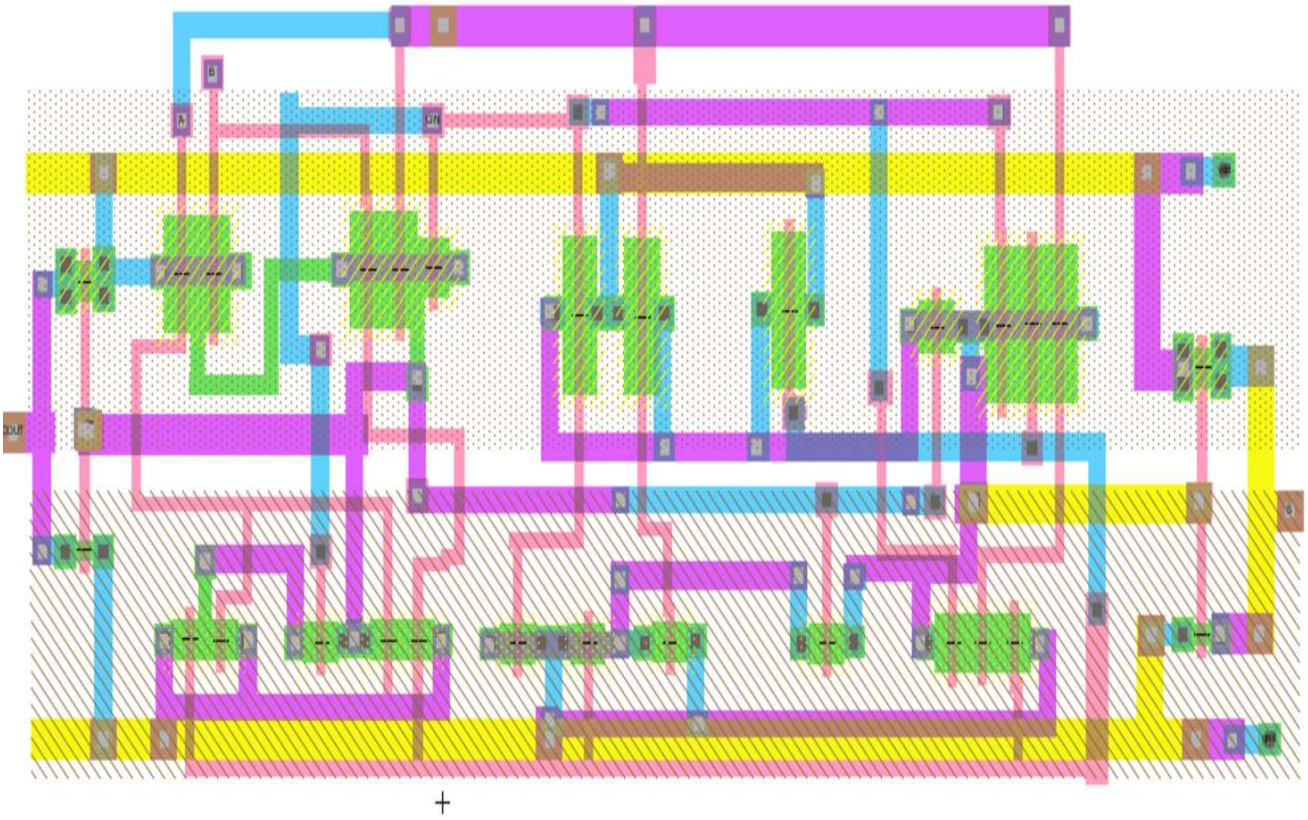
FULL ADDER

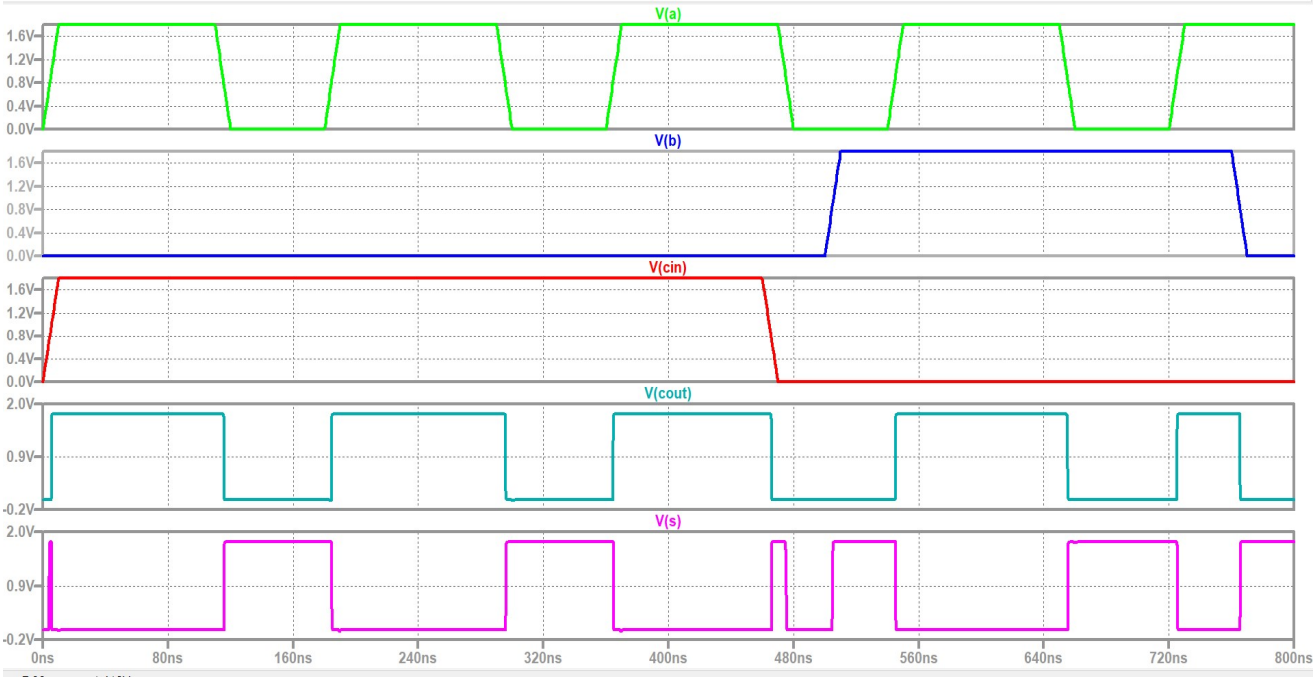
SCHEMATIC DIAGRAM



LAYOUT DESIGN



WAVEFORMS FOR THE DIFFERENT INPUTS



NETLIST CODE USED FOR CALUCULATING DELAYS:

```
* Spice Code nodes in cell cell 'FullAdder{sch}'
vdd vdd 0 DC 1.8
vin A 0 DC pulse 0 1.8 0 10ns 10ns 100ns 180ns
vin1 B 0 DC pulse 0 1.8 0.5u 10ns 10ns 250ns 400ns
vin2 CIN 0 DC pulse 0 1.8 0u 10ns 10ns 450ns 800ns
.measure tran tf trig v(S) val=1.62 fall=1 td=0ns targ v(S) val=0.18 fall=1
.measure tran tr trig v(S) val =0.18 rise=1 td=0ns targ v(S) val=1.62 rise =1
.measure tran tfC trig v(COUT) val=1.62 fall=1 td=0ns targ v(COUT) val=0.18 fall=1
.measure tran trC trig v(COUT) val =0.18 rise=1 td=0ns targ v(COUT) val=1.62 rise =1
.measure tdelay param ((tf+tr)/2)
.measure tdelayC param ((tfC+trC)/2)
.tran 0.1u .8us
.include C:\Esoftwarei\tsmc018.lib
.END
.END
```

Delay calculations in different input combinations

A	B	Cin	SUM(schematic)	Cout(schematic)	SUM(schematic)	Cout(schematic)
0	0	0	2.76815e-010	2.85726e-010	2.95151e-009	3.8359e-010
0	0	1	1.13445e-010	2.19511e-010	1.90637e-010	2.89809e-010
0	1	0	1.79346e-010	2.39557e-010	3.01113e-010	4.15054e-010
0	1	1	1.03666e-010	2.02321e-010	1.70848e-010	2.8359e-010
1	0	0	1.62226e-010	2.72656e-010	3.34133e-010	5.79764e-010
1	0	1	3.01052e-010	4.79102e-010	3.51052e-010	5.99451e-010
1	1	0	1.20017e-010	2.68834e-010	3.14595e-010	4.01465e-010
1	1	1	2.86815e-010	2.97824e-010	3.11062e-010	4.04034e-010

From the table above highest delay is observed for the combination of 101.