EEE 120

Capstone Project Answer Sheet (Online Class)

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Semester/Year/Session (A/B):Summer/2023/C Date:4/7/2023

Task C-1: Planning the Synchronous Sequential Machines

(5 pts) Interview your stakeholders (TAs, Instructors, family, friend, OR "Yourself"…etc.). Ask questions regarding the form, function, and features needed by potential customers for this design. Make sure to capture what the customer prefers from this type of solution, as well as what environment the customer plans to use this design. Summarize your findings here and document the names of who you interviewed.

Myself: I would like the design to be simple and try to use it for scientific measurements.

Brother: He wants the solution to be quick and try to measure dietary supplements.

Dad: He wants the solution to be accurate and precise and start in a balanced state.

Mom: She wants to use the solution for cooking and wants it to be easy to use.

(5 pts) Please include a comment on why your automation adds value from multiple perspectives (technological, societal, financial, environmental, etc.). (*What value does this add? What is the type of customer for whom this is designed? Where is this most needed? What couldn't you do before?*) [2-3 sentences are sufficient]

This is designed to be used in a retail environment in shops, so it can be used to measure food items or expensive items like gold or silver in high end jewelry stores. An automated measurement saves the retailer time and gives more accuracy and precision to the measurements. Most balances have a lot of inputs and are hard to use and this provides simplicity to the user.

(5 pts) It is allowable to continue to ask questions of stakeholders throughout the design process (and is preferred of a conscientious engineer). This can be done as you are designing, before you are designing if you need input and clarifications, or after you are done designing if you want feedback on improvements. Summarize any changes to your understanding or design based on the feedback you received during your initial interviews or continual interviews?

One of the feedbacks I received was to make a simple design, so I wanted to minimize the number of states I used to get a simple design.

One of the requirements was to get greater accuracy, so I will make a second design with more states and complexity.

Task C-2: Document the Synchronous Sequential Machines

Design #1: (2 pts) What assumptions did you make in the design of this machine? (Based on stakeholder's requests)

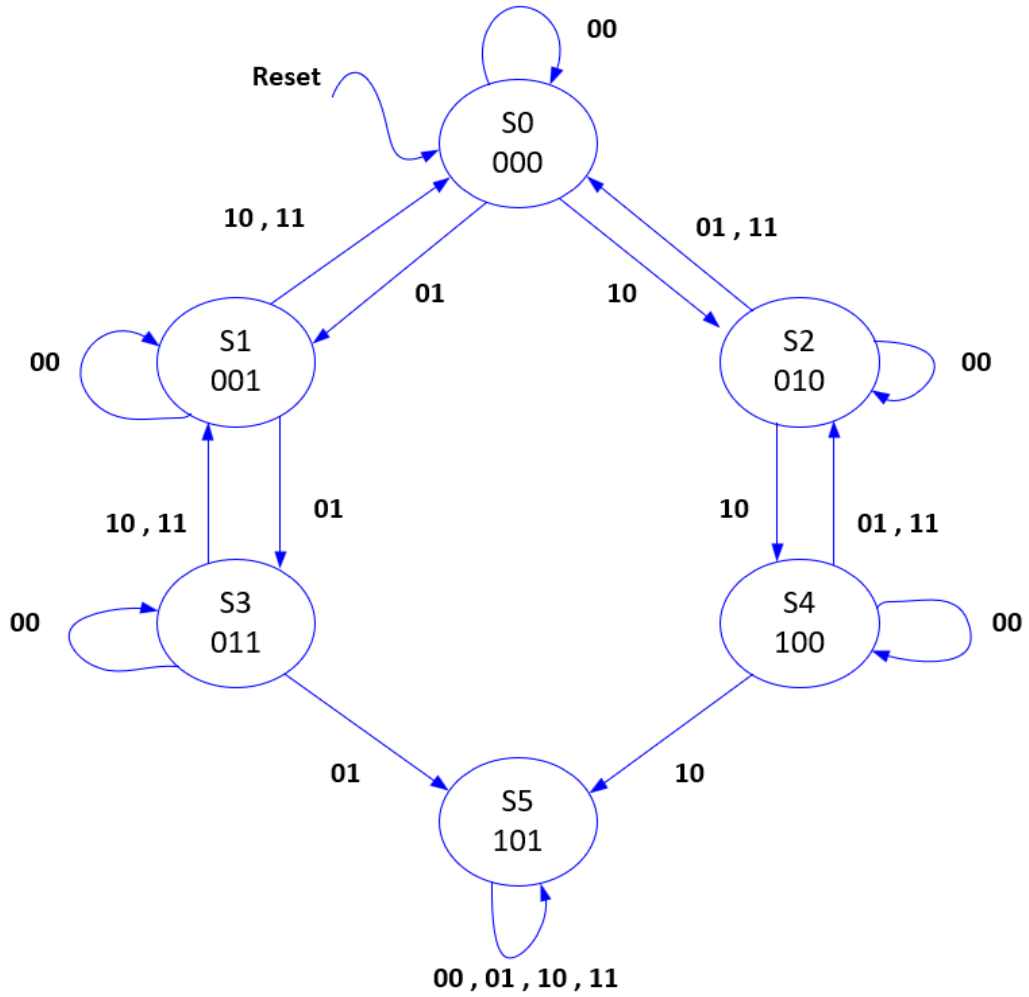
Assumptions:

- Will use an asynchronous reset to put the balance in known state
- Will start in the balanced state on power up.
- One weight should be added at a time

(3 pts) Create a state definition table here that describes in plain English what each state in your machine means and what binary values you have assigned to represent each state, inputs, and outputs.

S0	balanced state	000
S1	added weight to left side	001
S2	added weight to right side	010
S3	added weight to left side	011
S4	added weight to right side	100
S5	error state	101
S6	not used	110
S7	not used	111

(12 pts) Show your state diagrams, state transition tables and your circuit planning work (Karnaugh maps/MUX/DEC/etc.) used in your design process. (You can do this by hand if you wish, do **not** show the



Inputs	
W1W0=00	No Weight Added
W1W0=01	Weight Added to Left
W1W0=10	Weight Added to Right
W1W0=11	Weight Added to Lighter Side

State Tr	Q2	Q1	Q0	W1	W0	Q2*	Q1*	Q0*	J2	K2	J1	K1	J0	K0	L	R	E
S0->S0	0	0	0	0	0	0	0	0	0	X	0	X	0	X	0	0	0
S0->S1	0	0	0	0	1	0	0	1	0	X	0	X	1	X	0	0	0
S0->S2	0	0	0	1	0	0	1	0	0	X	1	X	0	X	0	0	0
S0->S0	0	0	0	1	1	0	0	0	0	X	0	X	0	X	0	0	0
S1->S1	0	0	1	0	0	0	0	1	0	X	0	X	X	0	1	0	0
S1->S3	0	0	1	0	1	0	1	1	0	X	1	X	X	0	1	0	0
S1->S0	0	0	1	1	0	0	0	0	0	X	0	X	X	1	1	0	0
S1->S0	0	0	1	1	1	0	0	0	0	X	0	X	X	1	1	0	0
S2->S2	0	1	0	0	0	0	1	0	0	X	X	0	0	X	0	1	0
S2->S0	0	1	0	0	1	0	0	0	0	X	X	1	0	X	0	1	0
S2->S4	0	1	0	1	0	1	0	0	1	X	X	1	0	X	0	1	0
S2->S0	0	1	0	1	1	0	0	0	0	X	X	1	0	X	0	1	0
S3->S3	0	1	1	0	0	0	1	1	0	X	X	0	X	0	1	0	0
S3->S5	0	1	1	0	1	1	0	1	1	X	X	1	X	0	1	0	0
S3->S1	0	1	1	1	0	0	0	1	0	X	X	1	X	0	1	0	0
S3->S1	0	1	1	1	1	0	0	1	0	X	X	1	X	0	1	0	0
S4->S4	1	0	0	0	0	1	0	0	X	0	0	X	0	X	0	1	0
S4->S2	1	0	0	0	1	0	1	0	X	1	1	X	0	X	0	1	0
S4->S5	1	0	0	1	0	1	0	1	X	0	0	X	1	X	0	1	0
S4->S2	1	0	0	1	1	0	1	0	X	1	1	X	0	X	0	1	0
S5->S5	1	0	1	0	0	1	0	1	X	0	0	X	X	0	0	0	1
S5->S5	1	0	1	0	1	1	0	1	X	0	0	X	X	0	0	0	1
S5->S5	1	0	1	1	0	1	0	1	X	0	0	X	X	0	0	0	1
S5->S5	1	0	1	1	1	1	0	1	X	0	0	X	X	0	0	0	1
S6->??	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
S6->??	1	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
S6->??	1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
S6->??	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
S7->??	1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
S7->??	1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
S7->??	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
S7->??	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

Using 5 variable K maps only some of them are shown here for simplicity:

Q2=0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	1	0	0
10	0	0	0	1

Q2=1	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

J2 = Q1Q0’W1W0’ + Q1Q0W1’W0

Q2=0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

Q2=1	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

K2 = Q0'W0

Q2=0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	1	1	1	1
10	0	0	0	0

Q2=1	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

L=Q2'Q0

Q2=0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

Q2=1	00	01	11	10
00	1	1	1	1
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

W=Q1Q0'+Q2Q0'

Q2=0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

Q2=1	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

E=Q2Q0

(3 pts) List your final design equations and required logic gates (including types of Flip Flops) needed to complete this circuit. Do **not** show the full circuit schematic here. You will implement (i.e. build on Digital) only one design. This design will be chosen based on Tasks C-3 and C-4.

J2 = Q1Q0'W1W0' + Q1Q0W1'W0

K2 = Q0'W0

J1 = Q2Q0'W0 + Q2'Q0W1W0' + Q2'Q0W1'W0

K1 = W1'W0 + Q0'W1

J0 = Q2W1W0' + Q2'Q1'W1'W0

K0 = Q2'Q1'W1

L = Q2'Q0

R = Q1Q0' + Q2Q0'

E = Q2Q0

Design #2: (2 pts) What assumptions did you make in the design of this machine? (Based on stakeholder's requests)

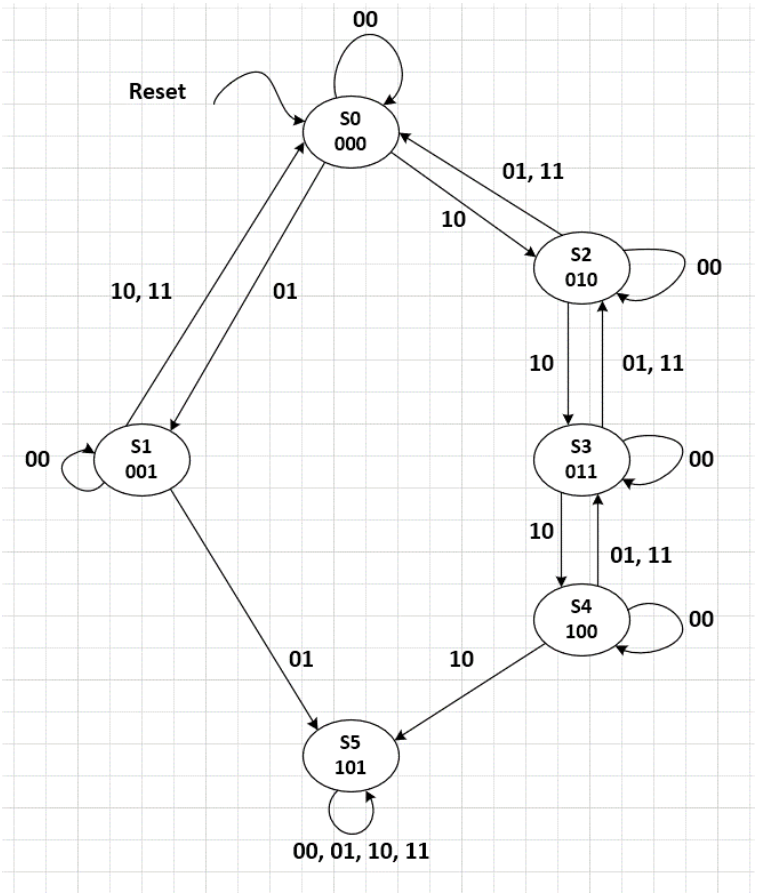
Assumptions:

- Will use an asynchronous reset to put the balance in known state
- Will start in the balanced state
- Two weights should be added at a time

(3 pts) Create a state definition table here that describes in plain English what each state in your machine means and what binary values you have assigned to represent each state.

S0	balanced state	000
S1	added weight to left side	001
S2	added weight to right side	010
S3	added weight to right side	011
S4	added weight to right side	100
S5	error state	101
S6	not used	110
S7	not used	111

(12 pts) Show your state diagrams, state transition tables and your circuit planning work (Karnaugh maps/MUX/DEC/etc.) used in your design process. (You can do this by hand if you wish, do **not** show the full circuit schematic here.)



Inputs	
W1W0=00	No Weight Added
W1W0=01	2 Weights Added to Left
W1W0=10	2 Weights Added to Right
W1W0=11	Weight Removed from Heavier Side

State Tr	Q2	Q1	Q0	W1	W0	Q2*	Q1*	Q0*	J2	K2	J1	K1	J0	K0	L	R	E
S0->S0	0	0	0	0	0	0	0	0	0	X	0	X	0	X	0	0	0
S0->S1	0	0	0	0	1	0	0	1	0	X	0	X	1	X	0	0	0
S0->S2	0	0	0	1	0	0	1	0	0	X	1	X	0	X	0	0	0
S0->S0	0	0	0	1	1	0	0	0	0	X	0	X	0	X	0	0	0
S1->S1	0	0	1	0	0	0	0	1	0	X	0	X	X	0	1	0	0
S1->S5	0	0	1	0	1	1	0	1	1	X	0	X	X	0	1	0	0
S1->S0	0	0	1	1	0	0	0	0	0	X	0	X	X	1	1	0	0
S1->S0	0	0	1	1	1	0	0	0	0	X	0	X	X	1	1	0	0
S2->S2	0	1	0	0	0	0	1	0	0	X	X	0	0	X	0	1	0
S2->S0	0	1	0	0	1	0	0	0	0	X	X	1	0	X	0	1	0
S2->S3	0	1	0	1	0	0	1	1	0	X	X	0	1	X	0	1	0
S2->S0	0	1	0	1	1	0	0	0	0	X	X	1	0	X	0	1	0
S3->S3	0	1	1	0	0	0	1	1	0	X	X	0	X	0	0	1	0
S3->S2	0	1	1	0	1	0	1	0	0	X	X	0	X	1	0	1	0
S3->S4	0	1	1	1	0	1	0	0	1	X	X	1	X	1	0	1	0
S3->S2	0	1	1	1	1	0	1	0	0	X	X	0	X	1	0	1	0
S4->S4	1	0	0	0	0	1	0	0	X	0	0	X	0	X	0	1	0
S4->S3	1	0	0	0	1	0	1	1	X	1	1	X	1	X	0	1	0
S4->S5	1	0	0	1	0	1	0	1	X	0	0	X	1	X	0	1	0
S4->S3	1	0	0	1	1	0	1	1	X	1	1	X	1	X	0	1	0
S5->S5	1	0	1	0	0	1	0	1	X	0	0	X	X	0	0	0	1
S5->S5	1	0	1	0	1	1	0	1	X	0	0	X	X	0	0	0	1
S5->S5	1	0	1	1	0	1	0	1	X	0	0	X	X	0	0	0	1
S5->S5	1	0	1	1	1	1	0	1	X	0	0	X	X	0	0	0	1
S6->??	1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X
S6->??	1	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
S6->??	1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X
S6->??	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X
S7->??	1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X
S7->??	1	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X
S7->??	1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X
S7->??	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X

Q2=0	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	0	0	0	1
10	0	0	0	0

Q2=1	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

J2 = Q1’Q0W1’W0 + Q1Q0W1W0’

Q2=0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

Q2=1	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

K2 = Q0'W0

Q2=0	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	0	0	0	0

Q2=1	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

L=Q2'Q1'Q0

Q2=0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

Q2=1	00	01	11	10
00	1	1	1	1
01	0	0	0	0
11	X	X	X	X
10	X	X	X	X

R=Q1+Q2Q0'

Q2=0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

Q2=1	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

E=Q2Q0

(3 pts) List your final design equations and required logic gates (including types of Flip Flops) needed to complete this circuit. Do **not** show the full circuit schematic here. You will implement (i.e. build on Digital) only one design. This design will be chosen based on Tasks C-3 and C-4.

J2 = Q1'Q0W1'W0 + Q1Q0W1W0'

K2 = Q0'W0

J1 = Q2Q0'W0 + Q2'Q0'W1W0'

K1 = Q0'W0 + Q0W1W0'

J0 = Q2W1 + Q1'W1'W0 + Q1W1W0'

K0 = Q2'W1 + Q1W0

L = Q2'Q1'Q0

R = Q1 + Q2Q0'

E = Q2Q0

Task C-3: Determine Criteria and Weighting for Judging Your Designs

(5 pts) Using the guidelines in the laboratory FAQ's, list your 5 criteria and associated weights here used to help decide between the two design models (weights should add to 100%):

Criteria	Weight
# FFs	20
# Logic Gates	20
#Time to Build	20
#Boolean Terms * #Literals	40
Working	0

Task C-4: Apply the Criteria to Pick the Best Design

(2 pts) Describe how you applied each of the criteria and weighting system in the above task to pick the best design. How did you choose these criteria (customer interviews, engineering preference)?

I used the design equations to calculate the number of flops, logic gates, and literals. This also gives me an idea of the time needed to build the circuit so I used the criteria that was the simplest and efficient time to build the circuit to choose a winner. Based on the customer interviews they wanted a simpler and efficient design.

(3 pts) Which design is better based on your criteria and weighting system and why? Please explain how the winning design scored in each category and why (the winning design does not need to score the highest in every category, but it does need to score higher overall when applying the criteria weights).

Criteria	Weight	Design 1	Design 2
# FFs	20	20 pts (3 Flops)	20 pts (3 Flops)
# Logic Gates	20	20 pts (21 gates)	18 pts (23 gates)
#Time to Build	20	20 pts (45 mins)	16 pts (1 hour)
#Boolean Terms * #Literals	40	38 pts (43 literals, 15 terms)	36 pts (41 literals, 16 terms)
Working	0	0	0

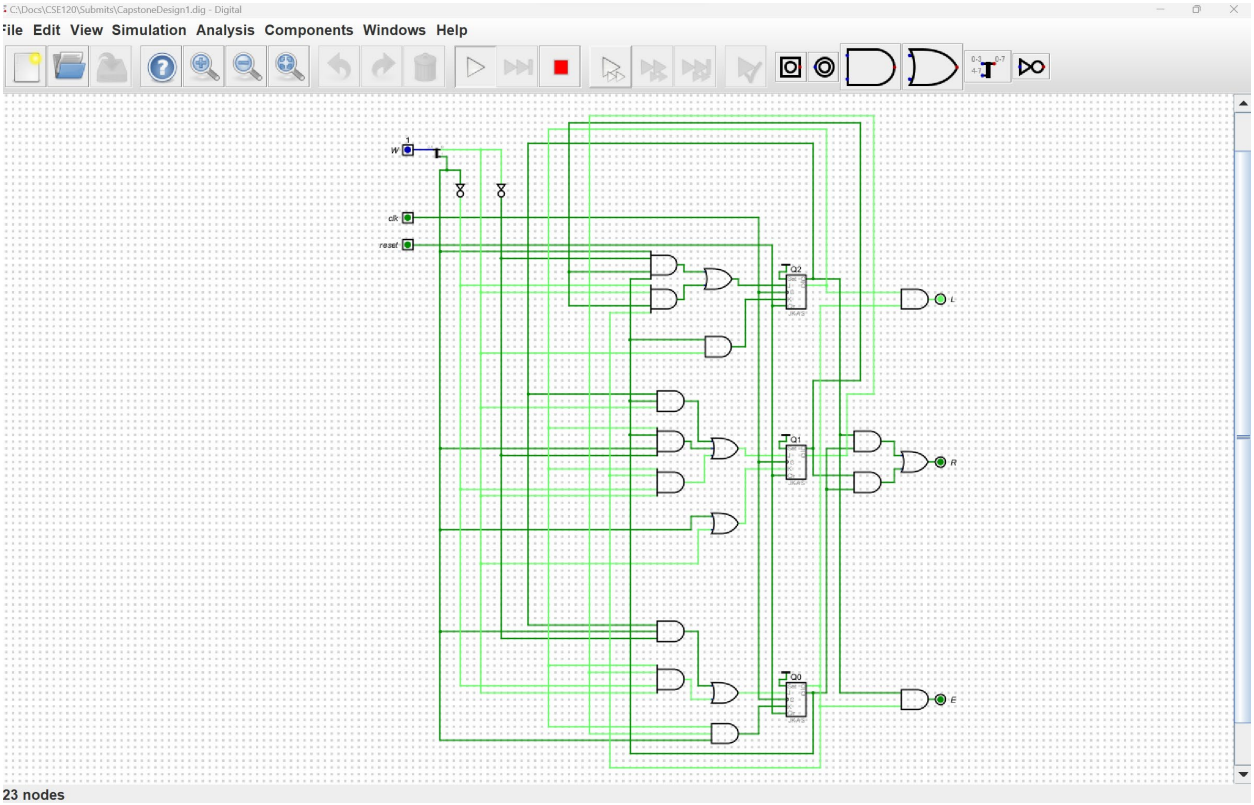
Total : Design 1 = 98 points

Design 2 = 90 points

Design 1 is more efficient and less logic gates and is the winner!

Task C-5: Build and Simulate Winning Design in Digital

(10 pts) Insert a copy of your chosen Digital Schematic here. Please make sure that you have outputs or tunnels connected to each flip flop so that you can easily monitor your states. Make sure that the logic and equations match the final equations presented in either Design 1 or Design 2.



(20 pts) Testing: Demonstrate that your "best" circuit meets the completed design specification. You only need to test one design, the one you chose according to your criteria in Task C-4. Use the table below for testing your circuit. Note the following:

- First write the names of the inputs and outputs. The names should match the manual's convention. Do not use A and B, or X and Y. Graders do not understand what those are.
- Fill-in the table with values you tested. Ideally, you need to test all arrows on the state diagram. If it is tedious, you need to come up with a sufficient testing plan.
- Modify the table as needed.
- If your expected output does not match the actual output, answer the questions at the end of this task.

Inputs **[Input names go here]**	**Expected Outputs According to Diagram** **[Output names go here]**	**Actual Outputs According to Circuit Simulation** **[Output names go here]**
Reset =1 , W = X	S0 , L = 0, R = 0, E = 0	S0 , L = 0, R = 0, E = 0
S0 -> S1, W = 01	S1 , L = 1, R = 0, E = 0	S1 , L = 1, R = 0, E = 0
S1 -> S0, W = 10, 11	S0 , L = 0, R = 0, E = 0	S0 , L = 0, R = 0, E = 0
S0 -> S2 , W = 10	S2 , L = 0, R = 1, E = 0	S2 , L = 0, R = 1, E = 0
S1 -> S3, W = 01	S3, L = 1, R = 0, E = 0	S3, L = 1, R = 0, E = 0
S2 -> S0, W = 01, 11	S0, L = 0, R = 0, E = 0	S0, L = 0, R = 0, E = 0
S2-> S4, W = 10	S4, L = 0, R = 1, E = 0	S4, L = 0, R = 1, E = 0
S0-> S3, W = 01 (twice)	S3, L = 1, R = 0, E = 0	S3, L = 1, R = 0, E = 0
S0-> S4, W = 10 (twice)	S4, L = 0, R = 1, E = 0	S4, L = 0, R = 1, E = 0
S3-> S1, W = 10, 11	S1, L = 1, R = 0, E = 0	S1, L = 1, R = 0, E = 0
S4-> S2, W = 01, 11	S2, L = 0, R = 1, E = 0	S2, L = 0, R = 1, E = 0
S3->S0, W = 10, 11 (twice)	S0, L = 0, R = 0, E = 0	S0, L = 0, R = 0, E = 0
S4-> S0, W = 01, 11 (twice)	S0, L = 0, R = 0, E = 0	S0, L = 0, R = 0, E = 0
S3-> S5, W = 01	S5, L = 0, R = 0, E = 1	S5, L = 0, R = 0, E = 1
S4-> S5, W = 10	S5, L = 0, R = 0, E = 1	S5, L = 0, R = 0, E = 1
S5-> S5, W = 00, 01, 10, 11	S5, L = 0, R = 0, E = 1	S5, L = 0, R = 0, E = 1

If your circuit does not work, answer the following questions:

- Where do you think the mistake is coming from? The design? The table? The kmaps? The circuit? Something else?
  Answer:_____

- How would you correct this mistake if you were given more time?
  Answer:_____

Task C-6: Record a Video Demonstration of the Winning Design (Optional)

(partial credit) If your circuit is not working and want to get partial credit, you can record a video demonstration showing at least 16 clock cycles being simulated through your Digital schematic. This could be a detailed explanation for the last two questions in Task C-5.

For every clock cycle, explain the inputs, what current state you are in, and point out any outputs that should be noted. Be sure to show what happens for different input combinations when the wheelchair is 3 positions to the left and right of center. Your demonstration should be able to showcase all possible states and transitions required to get there. If you include any asynchronous inputs, make sure to show those features as well. Add a link to your video here:

CAPSTONE DESIGN PROJECT: LAB REPORT GRADE SHEET

Name:

Grading Criteria	Max Points	Points lost
Template		
Neatness, Clarity, and Concision	5	
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task C-1: Planning the Synchronous Sequential Machines	15	
Task C-2: Document the Synchronous Sequential Machines	40	
Task C-3: Determine Criteria and Weighting for Judging Your Designs	5	
Task C-4: Apply the Criteria to Pick the Best Design	5	
Task C-5: Build and Simulate Winning Design in Digital	30	
Task C-6: Record a Video Demonstration of the Winning Design		
Self-Assessment Worksheet (The content of the self-assessment worksheet will not be graded. Full credit is given for including the completed worksheet.)	(2 extra points)	
Lab Score	**Points Lost**	
	Late Lab	
	Lab Score	

SELF-ASSESSMENT WORKSHEET

Put an 'X' in the table below indicating how strongly you agree or disagree that the outcomes of the assigned tasks were achieved. Use '5' to indicate that you 'strongly agree' and '1' to indicate that you 'strongly disagree'. Use 'NA', Not Applicable, when the tasks you performed did not elicit this outcome. Credit will be given for including this worksheet with your lab report. However, your **responses will not be graded**, they are for your instructor's information only.

Table 1: Self-Assessment of Outcomes for the Capstone Design Project Lab.

After completing the assigned tasks and report I am able to:	5	4	3	2	1	NA
Initiate a design process based on a value proposition and feedback from various stakeholders.	X					
Make assumptions to complete an incomplete functional specification.	X					
Use classical design techniques (i.e., state diagrams, state transition tables, and Karnaugh Maps), to design a synchronous sequential machine starting with a functional specification.	X					
Build, and debug a synchronous sequential machine.	X					
Develop reasonable engineering criteria for comparing different designs.	X					
Apply engineering criteria to select a 'best' design.	X					

Write below any suggestions you have for improving this laboratory exercise so that the stated learning outcomes are achieved.