EEE 120

Lab 4 Answer Sheet (Online Class)

The Complete Microprocessor

Name: Nitin Rao

Semester/Year/Session (A/B): Summer/2023/C Date:6/17/2023

**Task 4-1: Build and Test the Memory-Address-Generation Circuit**

Include a picture of your Digital circuit here:

A screenshot of a computer

Description automatically generated

Please comment on the single biggest issue you were facing when designing the circuit.

There were no issues with designing the circuit.

Did the circuit behave as expected? If no, what was wrong?

Yes, the circuit did behave as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

Figuring out how to use the tunnel in the circuit.

**Task 4-2: Build and Test the Controller Circuit**

Include a picture of your two\_bit\_mux circuit here:

A screenshot of a computer

Description automatically generated

Please comment on the single biggest issue you were facing when designing the circuit.

It was tricky and I almost forgot to rename it immediately before making changes.

Did the circuit behave as expected? If not, what was wrong?

Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

There were no issues with simulating the circuit.

Include a picture of your two\_bit\_reg circuit here:

A screenshot of a computer

Description automatically generated

Please comment on the single biggest issue you were facing when designing the circuit.

There were no issues with designing the circuit.

Did the circuit behave as expected? If no, what was wrong?

Yes the circuit did behave as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

There were no issues with simulating the circuit.

Include a picture of your controller circuit here:

A screenshot of a computer

Description automatically generated

Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue designing the circuit were loading the ROM and designing the splitters.

Did the circuit behave as expected? If no, what was wrong?

Yes, the circuit did behave as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

Figuring out all the inputs and sequencing them was the biggest issue.

**Task 4-3: Build the Complete Microprocessor Circuit**

Include a picture of your Digital circuit here (make sure to show final values as shown in figure 17):

A screenshot of a computer program

Description automatically generated with medium confidence

Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue was the splitter connections because they got updated when I changed the width of the circuits.

Did the circuit behave as expected? If no, what was wrong?

Yes, the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

Cycling through all the clocks and noting down all the changes was the biggest issue in simulating the circuit.

**Task 4-4: Simulate the Design in Verilog**

Include a picture of your waveforms here:

A screenshot of a computer

Description automatically generated

Please comment on the single biggest issue you were facing when simulating the processor.

The biggest issue was editing the ram\_vals into a text file and removing and editing the file.

Did the circuit behave as expected? If no, what was wrong?

Yes the circuit did behave as expected!

Please comment on the single biggest issue you were facing when simulating the circuit.

Loading all the waveforms and checking them was the biggest issue I faced when simulating the circuit.

**Task 4-5: Add the AND, ZERO, SUB, and STORE ACC Instructions**

Use Table 1 and Table 2 to enter your values into the microinstruction definition table for each of the four instructions asked for in the laboratory manual. Be sure to label the name of each and every instruction.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Table 1** | | | | | | | | | |
|  | Instruction | AND | | | | ZERO | | | |
|  | Opcode | 3 | | | | 4 | | | |
|  | step | 00 | 01 | 02 | 03 | 00 | 01 | 02 | 03 |
| **Description** | **Bit #** |  |  |  |  |  |  |  |  |
| load\_ir | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| write | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| read | 2 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| acc\_to\_db | 3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| load\_acc | 4 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| pass | 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| invert | 6 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| arith | 7 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| load\_mar | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| use\_pc | 9 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| unused | 11:10 | 00 | 00 | 00 | 0 | 00 | 00 | 00 | 0 |
| Next\_step[1:0] | 13:12 | 01 | 00 | 00 | 0 | 01 | 00 | 00 | 0 |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Table 2** | | | | | | | | | |
|  | Instruction | SUB | | | | STORE ACC | | | |
|  | Opcode | 5 | | | | 6 | | | |
|  | step | 00 | 01 | 02 | 03 | 00 | 01 | 02 | 03 |
| **Description** | **Bit #** |  |  |  |  |  |  |  |  |
| load\_ir | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| write | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| read | 2 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| acc\_to\_db | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| load\_acc | 4 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| pass | 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| invert | 6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| arith | 7 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| load\_mar | 8 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| use\_pc | 9 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| unused | 11:10 | 00 | 00 | 00 | 0 | 00 | 00 | 00 | 0 |
| Next\_step[1:0] | 13:12 | 01 | 00 | 00 | 0 | 01 | 10 | 00 | 0 |

Test your instructions by writing and executing programs. Record at least **four** programs and the output of each program in tables like that of Table .

|  |  |  |
| --- | --- | --- |
| **Table 1** | | |
| Program #1 ( AND 7 and D) | | |
| Address | Value | Operation (In English) |
| 0 | 0 | The 'Load ACC' Opcode |
| 1 | 7 | The number '7' to be loaded into the Accumulator |
| 2 | 3 | The 'AND to ACC' Opcode |
| 3 | D | The number 'D' to be ANDed to the Accumulator |
| 4 | 2 | The 'Stop' Opcode |
|  |  |  |
| What was the final output of your program? \_\_\_5\_\_ | | |
| Was the program successful? YES\_ | | |
| If not what error(s) did you find in your circuit? | | |

|  |  |  |
| --- | --- | --- |
| **Table 2** | | |
| Program #2 ( ZERO load 7 and then subtract by itself) | | |
| Address | Value | Operation (In English) |
| 0 | 0 | The 'Load ACC' Opcode |
| 1 | 7 | The number '7' to be loaded into the Accumulator |
| 2 | 4 | The 'ZERO to ACC' Opcode |
| 3 | 0 | not needed |
| 4 | 2 | The 'Stop' Opcode |
|  |  |  |
| What was the final output of your program? \_\_\_0\_\_ | | |
| Was the program successful? YES\_ | | |
| If not what error(s) did you find in your circuit? | | |

|  |  |  |
| --- | --- | --- |
| **Table 3** | | |
| Program #3 SUB (LOAD 3 INTO ACC, SUBTRACT 7 FROM RAM, -4 INTO ACC | | |
| Address | Value | Operation (In English) |
| 0 | 0 | The 'Load ACC' Opcode |
| 1 | 3 | The number '3' to be loaded into the Accumulator |
| 2 | 5 | The 'SUB from ACC' Opcode |
| 3 | 7 | The RAM Value loaded and Subtracted |
| 4 | 2 | The 'Stop' Opcode |
|  |  |  |
| What was the final output of your program? C (-4) | | |
| Was the program successful? YES\_ | | |
| If not what error(s) did you find in your circuit? | | |

|  |  |  |
| --- | --- | --- |
| **Table 4** | | |
| Program #4 ( STORE ACC VALUE 7 IN ADDR E) | | |
| Address | Value | Operation (In English) |
| 0 | 0 | The 'Load ACC' Opcode |
| 1 | 7 | The number '7' to be loaded into the Accumulator |
| 2 | 6 | The 'STORE ACC' Opcode |
| 3 | E | Address ‘D’ where 7 will be stored |
| 4 | 2 | The 'Stop' Opcode |
|  |  |  |
| What was the final output of your program? 7 | | |
| Was the program successful? YES\_ | | |
| If not what error(s) did you find in your circuit? | | |

Include a picture of your AND waveforms here:

A screenshot of a computer

Description automatically generated

Include a picture of your ZERO waveforms here:

A screenshot of a computer

Description automatically generated

Include a picture of your SUB waveforms here:

A screenshot of a computer

Description automatically generated

Include a picture of your STORE ACC waveforms here:

A screenshot of a computer

Description automatically generated

Did the circuit behave as expected? If no, what was wrong?

Yes the circuit behaved as expected.

Please comment on the single biggest issue you were facing when simulating the circuit.

The sheer amount of editing the ROM and running all the verifications was difficult and time-consuming.

Include a picture of your rom\_vals.hex if your made choice 1 or 2 or a picture of the ROM for choice 3 here:

A screenshot of a computer code

Description automatically generated with low confidence

Include your program from ram\_vals.txt:

A picture containing text, font, screenshot, white

Description automatically generatedA picture containing text, font, white, screenshot

Description automatically generated

A black text on a white background

Description automatically generated with low confidenceA picture containing text, font, white, screenshot

Description automatically generated

**Task 4-6: Invent Your Own Instruction (Extra Credit)**

**TWOCOMP**

**(LOAD ACC VALUE, PERFORM 2’s COMPLEMENT OF RAM VALUE AND STORE IN ACC)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Table 5** | | | | | |
|  | Instruction | TWOCOMP | | | |
|  | Opcode | 7 | | | |
|  | step | 00 | 01 | 02 | 03 |
| **Description** | **Bit #** |  |  |  |  |
| load\_ir | 0 | 1 | 0 | 0 | 0 |
| write | 1 | 0 | 0 | 0 | 0 |
| read | 2 | 1 | 1 | 0 | 0 |
| acc\_to\_db | 3 | 0 | 0 | 0 | 0 |
| load\_acc | 4 | 0 | 1 | 0 | 0 |
| pass | 5 | 0 | 1 | 0 | 0 |
| invert | 6 | 0 | 1 | 0 | 0 |
| arith | 7 | 0 | 1 | 0 | 0 |
| load\_mar | 8 | 0 | 0 | 0 | 0 |
| use\_pc | 9 | 1 | 1 | 0 | 0 |
| unused | 11:10 | 00 | 00 | 00 | 0 |
| Next\_step[1:0] | 13:12 | 01 | 00 | 00 | 0 |

Include your Verilog program here:

A black text on a white background

Description automatically generated with low confidence

Include a picture of your waveforms here:

2’s Complement of 7 is 9 which is the expected value.

A screenshot of a computer

Description automatically generated

Include a picture of your ROM contents here:

A picture containing text, font, white, typography

Description automatically generated

**Task 4-7: Create a video and submit your report (Optional)**

Include a picture of your final microprocessor here:

[This task is useful to get partial credit if your schematic is not working. Take advantage of it to explain to the grader your understanding of the circuit. More importantly, explain where you think the mistake is in and what you would do if you were given more time to fix it.]

Record a short video showing your schematic in Digital and your waveforms in GTKWave. Show schematic and the waveforms for AND, Zero, Subtract, Store ACC, and your extra credit instruction (if you did one). Be sure to show yourself in the video and show your screen. **Upload the video to your Google Drive (personal one or ASU one). Copy and paste the sharing link to that video here. Make sure the link is working and pointing to the correct video. Do NOT upload your video to YouTube.** If your circuit is not working as expected, explain in the video how it is not working and where you expect the mistake to be from.

**Video Link:**

**At the beginning of your recording, say your name, the task number and circuit name. Be brief in your recording. Submit the completed template to Canvas.**

**Make sure all your files are in the Lab3 directory. Create a zip file of the Lab3 directory. Remember to turn in the zip file and your completed template on Canvas! Make sure you upload the template before the zip file.**

Lab 4: Lab Report Grade Sheet

|  |  |
| --- | --- |
| **Name:** |  |

## Instructor Assessment

|  |  |  |
| --- | --- | --- |
| **Grading Criteria** | **Max Points** | **Points Lost** |
| **Description of Assigned Tasks, Work Performed & Outcomes Met** |  |  |
| Task 4-1: Build and Test the Memory-Address-Generation Circuit | 10 |  |
| Task 4-2: Build and Test the Controller Circuit | 10 |  |
| Task 4-3: Build the Complete Microprocessor Circuit | 10 |  |
| Task 4-4: Write and Execute a Simple Program for Your Microprocessor in Simulation | 20 |  |
| Task 4-5: Add the ‘AND’, ‘Zero’, ‘Subtract’, and ‘Store ACC’ Instructions | 30 |  |
| Task 4-6: Invent Your Own Instruction (Extra Credit) | 10 |  |
| Task 4-7: Record your video (Optional) |  |  |
|  | **Points Lost** |  |
| Lab Score (80 points total) | **Late Lab** |  |
|  | **Lab Score** |  |