mux-8ops.v U

lab11 > mux-8ops.v

```v
module all_ops(output [7:0] out, input i1, input i2);
    and (out[0], i1, i2);
    xor (out[1], i1, i2);
    nand (out[2], i1, i2);
    or (out[3], i1, i2);
    not (out[4], i1);
    not (out[5], i2);
    nor (out[6], i1, i2);
    xnor (out[7], i1, i2);
endmodule

module mux_8x1(output out, input [7:0] d, input s2, input s1, input s0);
    wire n2, n1, n0;
    wire [7:0] w;

    not (n2, s2);
    not (n1, s1);
    not (n0, s0);

    and_4 a0 (w[0], n2, n1, n0, d[0]);
```

mux-8ops-tb.v U

lab11 > mux-8ops-tb.v

```v
`include "mux-8ops.v"

module testbench;
    reg cin1, cin2, s2, s1, s0;
    wire [7:0] d;
    wire cout;

    all_ops ops (d, cin1, cin2);
    mux_8x1 mux (cout, d, s2, s1, s0);

    // 0 → Bitwise AND
    // 1 → Bitwise XOR
    // 2 → Bitwise NAND
    // 3 → Bitwise OR
    // 4 → Bitwise NOT (for 1st Input)
    // 5 → Bitwise NOT (for 2nd Input)
    // 6 → Bitwise NOR
    // 7 → Bitwise XNOR

    initial begin
```

TERMINAL OUTPUT DEBUG CONSOLE PROBLEMS GITLENS

zsh - lab11

```
abhishek@hp in repo: COA/lab11 on  main [?] via V took 27ms
❯ vvp a.out
                0 : in1=1 in2=0 S=000 out=0
               10 : in1=1 in2=0 S=001 out=1
               20 : in1=1 in2=0 S=011 out=1
               30 : in1=1 in2=0 S=010 out=1
               40 : in1=1 in2=0 S=110 out=0
               50 : in1=1 in2=0 S=111 out=0
               60 : in1=1 in2=0 S=101 out=1
               70 : in1=1 in2=0 S=100 out=0
```

mux-8ops.v U

lab11 > mux-8ops.v

```
    and_4 a0 (w[0], n2, n1, n0, d[0]);
    and_4 a1 (w[1], n2, n1, s0, d[1]);
    and_4 a2 (w[2], n2, s1, n0, d[2]);
    and_4 a3 (w[3], n2, s1, s0, d[3]);
    and_4 a4 (w[4], s2, n1, n0, d[4]);
    and_4 a5 (w[5], s2, n1, s0, d[5]);
    and_4 a6 (w[6], s2, s1, n0, d[6]);
    and_4 a7 (w[7], s2, s1, s0, d[7]);

    or_8 r0 (out, w);
endmodule

module and_4(output out, input a0, input a1, input a2, input a3);
    wire w1, w2;
    and (w1, a0, a1);
    and (w2, a2, a3);
    and (out, w1, w2);
endmodule
```

mux-8ops-tb.v U

lab11 > mux-8ops-tb.v

```
    initial begin
        cin1 = 1'b1; cin2 = 1'b0;
        s2 = 1'b0; s1 = 1'b0; s0 = 1'b0;
        #10; s0 = s0 + 1;
        #10; s1 = s1 + 1;
        #10; s0 = s0 + 1;
        #10; s2 = s2 + 1;
        #10; s0 = s0 + 1;
        #10; s1 = s1 + 1;
        #10; s0 = s0 + 1;
    end

    initial
        $monitor($time, " : in1=%b in2=%b S=%b%b%b out=%b", ci
endmodule
```

TERMINAL OUTPUT DEBUG CONSOLE PROBLEMS GITLENS

zsh - lab11

```
abhishek@hp in repo: COA/lab11 on  main [?] via V took 27ms
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                0 : in1=1 in2=0 S=000 out=0
               10 : in1=1 in2=0 S=001 out=1
               20 : in1=1 in2=0 S=011 out=1
               30 : in1=1 in2=0 S=010 out=1
               40 : in1=1 in2=0 S=110 out=0
               50 : in1=1 in2=0 S=111 out=0
               60 : in1=1 in2=0 S=101 out=1
               70 : in1=1 in2=0 S=100 out=0
```

mux-8ops.v U

lab11 > mux-8ops.v

```
31
32  module and_4(output out, input a0, input a1, input a2, input a3);
33      wire w1, w2;
34      and (w1, a0, a1);
35      and (w2, a2, a3);
36      and (out, w1, w2);
37  endmodule
38
39  module or_8(output out, input [7:0] a);
40      wire [6:0] w;
41      genvar i;
42      for (i = 0; i < 4; i = i + 1) begin
43          or (w[i], a[i], a[7-i]);
44      end
45      or (w[5], w[0], w[1]);
46      or (w[6], w[2], w[3]);
47      or (out, w[5], w[6]);
48  endmodule
```

mux-8ops-tb.v U

lab11 > mux-8ops-tb.v

```
19
20      initial begin
21          cin1 = 1'b1; cin2 = 1'b0;
22          s2 = 1'b0; s1 = 1'b0; s0 = 1'b0;
23          #10; s0 = s0 + 1;
24          #10; s1 = s1 + 1;
25          #10; s0 = s0 + 1;
26          #10; s2 = s2 + 1;
27          #10; s0 = s0 + 1;
28          #10; s1 = s1 + 1;
29          #10; s0 = s0 + 1;
30      end
31
32      initial
33          $monitor($time, " : in1=%b in2=%b S=%b%b%b out=%b", ci
34  endmodule
35
```

TERMINAL OUTPUT DEBUG CONSOLE PROBLEMS GITLENS

zsh - lab11

```
abhishek@hp in repo: COA/lab11 on  main [?] via V took 27ms
❯ vvp a.out
                0 : in1=1 in2=0 S=000 out=0
               10 : in1=1 in2=0 S=001 out=1
               20 : in1=1 in2=0 S=011 out=1
               30 : in1=1 in2=0 S=010 out=1
               40 : in1=1 in2=0 S=110 out=0
               50 : in1=1 in2=0 S=111 out=0
               60 : in1=1 in2=0 S=101 out=1
               70 : in1=1 in2=0 S=100 out=0
```

parity-bit.v U

lab11 > parity-bit.v

```v
module parity_8(output out1, output out2, input [7:0] a);
    wire [6:0] w;
    genvar i;
    for (i = 0; i < 4; i = i + 1) begin
        xor (w[i], a[i], a[7-i]);
    end
    xor (w[5], w[0], w[1]);
    xor (w[6], w[2], w[3]);
    xor (out1, w[5], w[6]);
    not (out2, out1);
endmodule

```

parity-bit-tb.v U

lab11 > parity-bit-tb.v

```v
`include "parity-bit.v"

module testbench;
    reg [7:0] cin;
    wire out1, out2;

    parity_8 parity (out1, out2, cin);

    initial begin
        cin = 8'b00000000;
        #10; cin = 8'b00100011;
        #10; cin = 8'b10101001;
        #10; cin = 8'b10111101;
        #10; cin = 8'b11111111;
        #10; cin = 8'b11111110;
        #10; cin = 8'b01010111;
        #10; cin = 8'b00000010;
        #10; cin = 8'b00100100;
    end

```

TERMINAL OUTPUT DEBUG CONSOLE PROBLEMS GITLENS

zsh - lab11

```
abhishek@hp in repo: COA/lab11 on  main [?] via V took 26ms
❯ vvp a.out
                0 : input=00000000 even-parity=0 odd-parity=1
               10 : input=00100011 even-parity=1 odd-parity=0
               20 : input=10101001 even-parity=0 odd-parity=1
               30 : input=10111101 even-parity=0 odd-parity=1
               40 : input=11111111 even-parity=0 odd-parity=1
               50 : input=11111110 even-parity=1 odd-parity=0
               60 : input=01010111 even-parity=1 odd-parity=0
               70 : input=00000010 even-parity=1 odd-parity=0
               80 : input=00100100 even-parity=0 odd-parity=1
```