and-3.v U

lab10 > and-3.v

```v
module and_3(output out, input b, input c, input d);
    wire w1;
    and (w1, b, c);
    and (out, w1, d);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 21ms
❯ iverilog and-3-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 35ms
❯ vvp a.out
                   0 : b=0 c=0 d=0 out=0
                  10 : b=0 c=0 d=1 out=0
                  20 : b=0 c=1 d=1 out=0
                  30 : b=0 c=1 d=0 out=0
                  40 : b=1 c=1 d=0 out=0
                  50 : b=1 c=1 d=1 out=1
                  60 : b=1 c=0 d=1 out=0
                  70 : b=1 c=0 d=0 out=0

abhishek@hp in repo: COA/lab10 on  main [?] via V took 18ms
❯
```

or-3.v U

lab10 > or-3.v

```v
module or_3(output out, input b, input c, input d);
    wire w1;
    or (w1, b, c);
    or (out, w1, d);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 18ms
❯ iverilog or-3-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 41ms
❯ vvp a.out
                   0 : b=0 c=0 d=0 out=0
                  10 : b=0 c=0 d=1 out=1
                  20 : b=0 c=1 d=1 out=1
                  30 : b=0 c=1 d=0 out=1
                  40 : b=1 c=1 d=0 out=1
                  50 : b=1 c=1 d=1 out=1
                  60 : b=1 c=0 d=1 out=1
                  70 : b=1 c=0 d=0 out=1

abhishek@hp in repo: COA/lab10 on  main [?] via V took 18ms
❯
```

not.v U

lab10 > not.v

```v
module not_v (input a, output out);
    not (out, a);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 18ms
❯ iverilog not-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 21ms
❯ vvp a.out
                0 : a=0 out=1
               10 : a=1 out=0

abhishek@hp in repo: COA/lab10 on  main [?] via V took 26ms
❯
```

nand.v U

lab10 > nand.v

```v
module nand_v (output out, input a, input b);
    wire w1;
    and (w1, a, b);
    not (out, w1);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 26ms
❯ iverilog nand-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 22ms
❯ vvp a.out
                0 : a=0 b=0 out=1
               10 : a=0 b=1 out=1
               20 : a=1 b=1 out=0
               30 : a=1 b=0 out=1

abhishek@hp in repo: COA/lab10 on  main [?] via V took 21ms
❯
```

nor.v U

lab10 > nor.v

```v
module nor_v (output out, input a, input b);
    wire w1;
    or (w1, a, b);
    not (out, w1);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 21ms
❯ iverilog nor-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 21ms
❯ vvp a.out
                   0 : a=0 b=0 out=1
                  10 : a=0 b=1 out=0
                  20 : a=1 b=1 out=0
                  30 : a=1 b=0 out=0

abhishek@hp in repo: COA/lab10 on  main [?] via V took 19ms
❯
```

xor.v U

lab10 > xor.v

```v
module xor_v(output out, input a, input b);
    wire w1, w2, w3, w4;
    not (w1, a);
    not (w2, b);
    and (w3, w1, b);
    and (w4, a, w2);
    or (out, w3, w4);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 24ms
❯ iverilog xor-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 20ms
❯ vvp a.out
                   0 : a=0 b=0 out=0
                  10 : a=0 b=1 out=1
                  20 : a=1 b=1 out=0
                  30 : a=1 b=0 out=1

abhishek@hp in repo: COA/lab10 on  main [?] via V took 18ms
❯
```

xnor.v U

lab10 > xnor.v

```v
module xnor_v(output out, input a, input b);
    wire w1, w2, w3, w4;
    not (w1, a);
    not (w2, b);
    and (w3, a, b);
    and (w4, w1, w2);
    or (out, w3, w4);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 22ms
❯ iverilog xnor-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 36ms
❯ vvp a.out
                0 : a=0 b=0 out=1
               10 : a=0 b=1 out=0
               20 : a=1 b=1 out=1
               30 : a=1 b=0 out=0

abhishek@hp in repo: COA/lab10 on  main [?] via V took 20ms
❯
```

and-nor.v U

lab10 > and-nor.v

```v
module and_nor(output out, input a, input b, input c);
    wire w1, w2, w3, w4, w5;
    nor_v nor1(w1, a, a);
    nor_v nor2(w2, b, b);
    nor_v nor3(w3, w1, w2);
    nor_v nor4(w4, w3, w3);
    nor_v nor5(w5, c, c);
    nor_v nor6(out, w4, w5);
endmodule

module nor_v (output out, input a, input b);
    wire w1;
    or (w1, a, b);
    not (out, w1);
endmodule
```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 20ms
❯ iverilog and-nor-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 23ms
❯ vvp a.out
                   0 : a=0 b=0 c=0 out=0
                  10 : a=0 b=0 c=1 out=0
                  20 : a=0 b=1 c=1 out=0
                  30 : a=0 b=1 c=0 out=0
                  40 : a=1 b=1 c=0 out=0
                  50 : a=1 b=1 c=1 out=1
                  60 : a=1 b=0 c=1 out=0
                  70 : a=1 b=0 c=0 out=0

abhishek@hp in repo: COA/lab10 on  main [?] via V took 21ms
❯
```

xor-nand.v U

lab10 > xor-nand.v

```
1  module xor_nand(output out, input a, input b);
2      wire w1, w2, w3;
3      nand_v nand1(w1, a, b);
4      nand_v nand2(w2, a, w1);
5      nand_v nand3(w3, b, w1);
6      nand_v nand4(out, w2, w3);
7  endmodule
8
9  module nand_v (output out, input a, input b);
10     wire w1;
11     and (w1, a, b);
12     not (out, w1);
13 endmodule
14
```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 21ms
❯ iverilog xor-nand-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 23ms
❯ vvp a.out
                 0 : a=0 b=0 out=0
                10 : a=0 b=1 out=1
                20 : a=1 b=1 out=0
                30 : a=1 b=0 out=1

abhishek@hp in repo: COA/lab10 on  main [?] via V took 34ms
❯
```

half-adder.v U

lab10 > half-adder.v

```
1  module half_adder_nand(output sum, output carry,input a, input b);
2      wire w1;
3      xor_nand xor1(sum, a, b);
4      nand_v nand1(w1, a, b);
5      nand_v nand2(carry, w1, w1);
6  endmodule
7
8  module xor_nand(output out, input a, input b);
9      wire w1, w2, w3;
10     nand_v nand1(w1, a, b);
11     nand_v nand2(w2, a, w1);
12     nand_v nand3(w3, b, w1);
13     nand_v nand4(out, w2, w3);
14 endmodule
15
16 module nand_v (output out, input a, input b);
17     wire w1;
18     and (w1, a, b);
19     not (out, w1);
20 endmodule
21
```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 34ms
❯ iverilog half-adder-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 22ms
❯ vvp a.out
                   0 : a=0 b=0 sum=0 carry=0
                  10 : a=0 b=1 sum=1 carry=0
                  20 : a=1 b=1 sum=0 carry=1
                  30 : a=1 b=0 sum=1 carry=0

abhishek@hp in repo: COA/lab10 on  main [?] via V took 22ms
❯
```

full-adder.v U

lab10 > full-adder.v

```v
module full_adder(sum,cout,a,b,cin);
    output sum, cout;
    input a, b, cin;
    wire w1,c1,c2;
    half_adder half1(w1, c1, a, b);
    half_adder half2(sum, c2, w1, cin);
    or(cout, c1, c2);
endmodule
module half_adder(sum,cout,a,b);
    output sum, cout;
    input a, b;
    xor(sum, a, b);
    and(cout, a, b);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 22ms
❯ iverilog full-adder-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 23ms
❯ vvp a.out
                   0 a=0 b=0 carry_in=0 sum=0 carry_out=0
                  10 a=0 b=0 carry_in=1 sum=1 carry_out=0
                  20 a=0 b=1 carry_in=1 sum=0 carry_out=1
                  30 a=0 b=1 carry_in=0 sum=1 carry_out=0
                  40 a=1 b=1 carry_in=0 sum=0 carry_out=1
                  50 a=1 b=1 carry_in=1 sum=1 carry_out=1
                  60 a=1 b=0 carry_in=1 sum=0 carry_out=1
                  70 a=1 b=0 carry_in=0 sum=1 carry_out=0

abhishek@hp in repo: COA/lab10 on  main [?] via V took 19ms
❯
```

mux.v U

lab10 > mux.v

```v
module mux(output out, input d0, input d1, input d2, input d3, input s1, input s0);
    wire n1, n0, w1, w2, w3, w4;
    not (n1, s1);
    not (n0, s0);
    and_3 a0 (w1, n1, n0, d0);
    and_3 a1 (w2, n1, s0, d1);
    and_3 a2 (w3, s1, n0, d2);
    and_3 a3 (w4, s1, s0, d3);
    or_4 r0 (out, w1, w2, w3, w4);
endmodule

module and_3(output out, input b, input c, input d);
    wire w1;
    and (w1, b, c);
    and (out, w1, d);
endmodule

module or_4(output out, input a0, input a1, input a2, input a3);
    wire w1, w2;
    or (w1, a0, a1);
    or (w2, a2, a3);
    or (out, w1, w2);
endmodule

```

.../Programs/COA/lab10

```
abhishek@hp in repo: COA/lab10 on  main [?] via V took 19ms
❯ iverilog mux-tb.v

abhishek@hp in repo: COA/lab10 on  main [?] via V took 21ms
❯ vvp a.out
                   0 : d0 = 0, d1 = 1, d2 = 1, d3 = 0, s1 = 0, s0 = 0, out = 0
                  10 : d0 = 0, d1 = 1, d2 = 1, d3 = 0, s1 = 0, s0 = 1, out = 1
                  20 : d0 = 0, d1 = 1, d2 = 1, d3 = 0, s1 = 1, s0 = 1, out = 0
                  30 : d0 = 0, d1 = 1, d2 = 1, d3 = 0, s1 = 1, s0 = 0, out = 1
                  50 : d0 = 1, d1 = 0, d2 = 0, d3 = 1, s1 = 0, s0 = 0, out = 1
                  60 : d0 = 1, d1 = 0, d2 = 0, d3 = 1, s1 = 0, s0 = 1, out = 0
                  70 : d0 = 1, d1 = 0, d2 = 0, d3 = 1, s1 = 1, s0 = 1, out = 1
                  80 : d0 = 1, d1 = 0, d2 = 0, d3 = 1, s1 = 1, s0 = 0, out = 0

abhishek@hp in repo: COA/lab10 on  main [?] via V took 24ms
❯
```