



chip_name

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1 chip_name		0x00000000 - 0x0000001F
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1.1 block1		0x00000000 - 0x0000000B
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1.1.1 reg1					Reg. 	0x00000000
bits	name	s/w	h/w	default	description	
31:0	fld	rw	rw	0x0		

1.1.2 reggroup1		0x00000004 - 0x0000000B
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1.1.2.1 reg1

Reg.
31:0

0x00000004

bits	name	s/w	h/w	default	description
31:0	fld	rw	rw	0x0	

1.1.2.2 reg2


Reg.
31:0


0x00000008


bits	name	s/w	h/w	default	description
31:0	fld1	rw	rw	0x0	

End RegGroup

1.2 block2		0x0000000C - 0x0000001F
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1.2.1 reggroup1		0x0000000C - 0x00000013
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1.2.1.1 reg1					Reg. 	0x0000000C
bits	name	s/w	h/w	default	description	
31:0	fld	rw	rw	0x0		


1.2.1.2 reg2					Reg. 	0x00000010
bits	name	s/w	h/w	default	description	
31:0	fld1	rw	rw	0x0		


End RegGroup

1.2.2 ref_name					RegGrp 	0x00000014 - 0x0000001F

1.2.2.1 reg1					Reg. 	0x00000014
bits	name	s/w	h/w	default	description	
31:0	fld	rw	rw	0x0		

1.2.2.2 reggroup1					RegGrp 	0x00000018 - 0x0000001F

1.2.2.2.1 reg1					Reg. 	0x00000018
bits	name	s/w	h/w	default	description	
31:0	fld	rw	rw	0x0		

1.2.2.2.2 reg2					Reg. 	0x0000001C
bits	name	s/w	h/w	default	description	
31:0	fld1	rw	rw	0x0		

End RegGroup

End RegGroup