chip\_name

Index	Com	ponent		Default		Address	Page
	chip_name					0 - 0x0000001F	2
.1	block1					0 - 0x0000000B	2
.1.1	reg1			0x0000000			2
.1.2	reggroup1					4 - 0x0000000B	2
.1.2.1	reg1			0x0000000			2
.1.2.2	reg2			0x0000000			2
.2	block2					C - 0x0000001F	2
.2.1	reggroup1					C - 0x00000013	2
.2.1.1	reg1			0x0000000			3
.2.1.2	reg2			0x0000000	00 0x00000010	0	3
.2.2	ref_name					4 - 0x000001F	3
.2.2.1	reg1			0x0000000			3
.2.2.2	reggroup1					8 - 0x000001F	3
.2.2.2.1	reg1			0x0000000			3
.2.2.2.2	reg2			0x0000000			3
1 block	1					Block	0x00000000 -
.1 block	1					Block □ T	0x00000000 - 0x0000000B
						Block T	
		s/w	h/w	de	efault	Reg.	0x0000000B
l.1.1 reg1	l	S/W rw	h/w rw	de 0x0	efault	Reg.	0x0000000B
bits 1:0 fld	name				efault	Reg.	0x0000000B
bits 11:0 fld	name				efault	Reg.	0x0000000B  0x00000000 escription  0x00000004 -
.1.1 reg1 bits 1:0 fld .1.2 regg	name			0x0	efault	Reg.	0x0000000B  0x00000000 escription  0x00000004 - 0x0000000B
1:0 fld	name group1	rw	rw	0x0		Reg.	0x0000000B  0x00000000  escription  0x00000004 - 0x0000000B
bits 1:0 fld  .1.2 regg  .1.2.1 re	name group1	rw s/w	rw h/w	0x0		Reg.	0x0000000B  0x00000000  escription  0x00000004 - 0x0000000B

1.1.2.	2 reg2				Reg.	0x00000008
bits	name	s/w	h/w	default	de	scription
31:0	fld1	rw	rw	0x0		

4.0 L.L L.O
1.2 block2 0x0000000C - 0x0000001F

End RegGroup

1.2.1 reggroup1	RegGrp	0x000000C -
		0x00000013

.2.1.1 re	g1					Reg.	0x000000C
bits	name	s/w	h/w		default		description
1:0 fld		rw	rw	0x0			
.2.1.2 re	<b>j</b> 2					Reg.	0x00000010
bits	name	s/w	h/w		default		description
1:0 fld1		rw	rw	0x0			·
					End RegGroup		
.2.2 ref_	name					RegGrp	0x00000014 -
,							0x0000001F
.2.2.1 re	g1					Reg.	0x00000014
		o hu	<b>b</b> /w		dofoult		docorintian
bits 1:0 fld	name	s/w rw	h/w rw	0x0	default		description
- , -							
.2.2.2 re	agroup1					RegGrp	0x00000018 -
	,						0x0000001F
.2.2.2.1	eg1					Reg.	0x00000018
bits	name	s/w	h/w		default		description
1:0 fld		rw	rw	0x0			
.2.2.2.2	eg2					Reg.	0x0000001C
bits	name	s/w	h/w	0.0	default		description
1:0 fld1		rw	rw	0x0			
					End RegGroup		
					Ella RegGloup		
					End RegGroup		