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Here, we will start with an example which consist, one of the ways to describe the simple properties of this tool.

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**In this example clock\_edge, reset\_level, reset\_type and repeat properties are applied to blocks and registers**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1 Chip1 | | | Chip1 | | chip | 0x0 |
| offset |  | external | |  | size |  |
|  | | | | | | |
| oid=b10bb88d-e467-4f2d-856f-3f4ca6ee01dc | | | | | | |
|  | | | | | | |

**In-line Property specification**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1.1 Block1 | | | Block1 | | block | 0x0 |
| offset |  | external | |  | size |  |
|  | | | | | | |
| oid=1abe2011-a368-416c-b4af-9740ba5e4055 | | | | | | |
| {clock\_edge=posedge; reset\_type=async} | | | | | | |

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| 1.1.1 reg\_grp2 | | | | reg\_grp2 | | | section | | 0x0 | |
| offset |  | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=43a5e4e6-c724-4619-b72d-063c953e5a89 | | | | | | | | | | |
|  | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.1.1 Reg1 | | | | | | | | Reg1 | | | | | reg32 | | 0x0 |
| offset | | 0 | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=68cb2db6-6b4f-42f4-89db-e02125ca360d | | | | | | | | | | | | | | | |
| {clock\_edge=negedge;reset\_type=sync} | | | | | | | | | | | | | | | |
| Bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 1:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |
| 2:3 | Fld2 | | | Ro |  | | 0 | | | This is new fild | | | | | |
| 6:30 | Fld3 | | | Ro | Rw | | 0 | | | This is fld3 field | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.1.2 Reg2 | | | | | | | | Reg2 | | | | | reg32 | | 0x8 |
| offset | | 8 | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=dc118bc6-bdd9-4a01-858b-fae80b3c4ef6 | | | | | | | | | | | | | | | |
| {reset\_level=high} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

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| --- |
| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.2 Reg3 | | | | | | | | Reg3 | | | | | reg32 | | 0x9, 0xa... |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=75e2a002-0d92-495d-8acc-393531da0441 | | | | | | | | | | | | | | | |
| {repeat=2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 11:0 | fld | | | ro | rw | | 0 | | | This is regggg3 | | | | | |
| 13:27 | Fx\_c | | | Ro |  | | 0 | | | Fx\_c reg to fun | | | | | |

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| 1.1.3 Reg34 | | | | | | | | Reg34 | | | | | reg32 | | 0xb, 0xc... |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=94f2428d-efc4-4563-b56a-0c8c968af5f0 | | | | | | | | | | | | | | | |
| {repeat=2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | ro | rw | | 0 | | | This is regggg34 | | | | | |

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| 1.1.4 Reg35 | | | | | | | | Reg35 | | | | | reg32 | | 0xd, 0xe... |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=9c6b2eea-5ebc-4cc9-8f64-9ab44ca87ce1 | | | | | | | | | | | | | | | |
| {repeat=2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | ro | rw | | 0 | | | This is regggg35 | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.5 Reg36 | | | | | | | | Reg36 | | | | | reg32 | | 0xf, 0x10... |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=39f4a54b-3386-4f7d-ac6c-46e4c03244e6 | | | | | | | | | | | | | | | |
| {repeat=2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | ro | rw | | 0 | | | This is regggg36 | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.6 Reg37 | | | | | | | | Reg37 | | | | | reg32 | | 0x11, 0x12... |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=ee4fb16c-ffc6-4a38-ab78-5148bb293204 | | | | | | | | | | | | | | | |
| {repeat=2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | ro | rw | | 0 | | | This is regggg37 | | | | | |

**Explicitly Property Specification**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2 Block2 | | | Block2 | | block | 0x13 | | | | |
| offset |  | external | |  | size |  | | repest | | 2 |
| Clock\_edge | posedge | Reset\_level | | high |  |  | Reset\_type | | async | |
|  | | | | | | | | | | |
| oid=f9c9d507-9a3e-4216-bcd5-fd1e318ea1ef | | | | | | | | | | |
|  | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1 reg\_group | | | | reg\_group | | | section | | 0x13 | |
| offset |  | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=57aac560-7119-44e7-a60e-c6128bc7e256 | | | | | | | | | | |
|  | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1.1 Reg1 | | | | | | | | Reg1 | | | | | reg32 | | 0x13 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=d6b5724c-2032-45ad-851b-a0f28764e1ce | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1.2 Reg2 | | | | | | | | Reg2 | | | | | reg32 | | 0x14 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
| Reset\_type | | sync |  | | |  | | |  | |  |  | |  | |
|  | | | | | | | | | | | | | | | |
| oid=b1ffb381-5556-4bcf-8c89-a2bf8be3121a | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

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| --- |
| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.2 Reg3 | | | | | | | | Reg3 | | | | | reg32 | | 0x15 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
| Clock\_edge | | posedge | Reset\_level | | | low | | |  | |  |  | |  | |
|  | | | | | | | | | | | | | | | |
| oid=00027183-27d6-4be4-a2af-8f5d445a66e0 | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld | | | ro | rw | | 0 | | |  | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3 reg\_group36 | | | | reg\_group36 | | | section | | 0x16 | |
| offset |  | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=0560906b-137a-4f72-b86d-64f67df429b9 | | | | | | | | | | |
|  | | | | | | | | | | |

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| 1.2.3.1 Reg1 | | | | | | | | Reg1 | | | | | reg32 | | 0x16 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=befb91a9-2cc8-42c7-af2b-6b77871235e9 | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.2 Reg2 | | | | | | | | Reg2 | | | | | reg32 | | 0x17 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
| Reset\_type | | sync |  | | |  | | |  | |  |  | |  | |
|  | | | | | | | | | | | | | | | |
| oid=88537f91-3563-471f-abf1-49559a0b445f | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.3 Reg13 | | | | | | | | Reg13 | | | | | reg32 | | 0x18 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=2c64c7de-86f3-420f-a859-1fe22837a9cc | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.4 Reg24 | | | | | | | | Reg24 | | | | | reg32 | | 0x19 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
| Reset\_type | | sync |  | | |  | | |  | |  |  | |  | |
|  | | | | | | | | | | | | | | | |
| oid=e13a3113-0cac-4a89-b6e5-6373d60165c6 | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.5 Reg15 | | | | | | | | Reg15 | | | | | reg32 | | 0x1a |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=11898aae-0fc4-4026-b3f0-f1bb8c4422ca | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.6 Reg2677 | | | | | | | | Reg2677 | | | | | reg32 | | 0x1b |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
| Reset\_type | | sync |  | | |  | | |  | |  |  | |  | |
|  | | | | | | | | | | | | | | | |
| oid=6698f9d2-af8a-424b-ae2c-76247871125a | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

|  |
| --- |
| End RegGroup |