|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Table of Content** | | | | |
| **Table of Content** | | | | |
| **Index** | **Component** | **Default** | **Address** | **Page** |
| 1 | [chip1](#1.0) |  | 0x00 |  |
| 1.1 | [test44](#1.1.0) |  | 0x0 |  |
| 1.1.1 | [reg\_name](#1.1.1.0) | 0x00 | 0x0 |  |
| 1 | [chip1](#1.0) |  | 0x00 |  |
| 1.1 | [test44](#1.1.0) |  | 0x0 |  |
| 1.1.1 | [reg\_name](#1.1.1.0) | 0x00 | 0x0 |  |
| 1 | [chip1](#1.0) |  | 0x00 |  |
| 1.1 | [block421](#1.0) |  | 0x00 |  |
| 1.1.1 | [reggroup1](#1.1.0) |  | 0x00 |  |
| 1.1.2 | [reg1](#1.1.1.0) | 0x00000000 | 0x28 |  |
| 1.2 | [block1](#1.0) |  | 0x2C |  |
| 1.2.1 | [reggroup1](#1.1.0) |  | 0x2C |  |
| 1.2.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x2C |  |
| 1.2.1.2 | [reg2](#1.0) | 0x00000000 | 0x30 |  |
| 1.2.2 | [reg1](#1.1.0) | 0x00000000 | 0x34 |  |
| 1.2.3 | [block2](#1.1.1.0) |  | 0x38 |  |
| 1.2.3.1 | [reggroup1](#1.1.2.0) |  | 0x38 |  |
| 1.2.3.1.1 | [reg1](#1.2.0) | 0x00000000 | 0x38 |  |
| 1.2.3.1.2 | [reg2](#1.2.1.0) | 0x00000000 | 0x3C |  |
| 1.2.3.2 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x40 |  |
| 1.3 | [block3](#1.2.1.2.0) |  | 0x44 |  |
| 1.3.1 | [reggroup1](#1.2.2.0) |  | 0x44 |  |
| 1.3.1.1 | [reg1](#1.2.3.0) | 0x00000000 | 0x44 |  |
| 1.3.1.2 | [reg2](#1.2.3.1.0) | 0x00000000 | 0x48 |  |
| 1.3.2 | [reg1](#1.2.3.1.1.0) | 0x00000000 | 0x4C |  |
| 1 | [chip1](#1.2.3.1.2.0) |  | 0x00 |  |
| 1.1 | [block421](#1.0) |  | 0x00 |  |
| 1.1.1 | [reggroup1](#1.1.0) |  | 0x00 |  |
| 1.1.2 | [reg1](#1.1.1.0) | 0x00000000 | 0x28 |  |
| 1.2 | [block1](#1.0) |  | 0x2C |  |
| 1.2.1 | [reggroup1](#1.1.0) |  | 0x2C |  |
| 1.2.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x2C |  |
| 1.2.1.2 | [reg2](#1.0) | 0x00000000 | 0x30 |  |
| 1.2.2 | [reg1](#1.1.0) | 0x00000000 | 0x34 |  |
| 1.2.3 | [block2](#1.1.1.0) |  | 0x38 |  |
| 1.2.3.1 | [reggroup1](#1.1.2.0) |  | 0x38 |  |
| 1.2.3.1.1 | [reg1](#1.2.0) | 0x00000000 | 0x38 |  |
| 1.2.3.1.2 | [reg2](#1.2.1.0) | 0x00000000 | 0x3C |  |
| 1.2.3.2 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x40 |  |
| 1.3 | [block3](#1.2.1.2.0) |  | 0x44 |  |
| 1.3.1 | [reggroup1](#1.2.2.0) |  | 0x44 |  |
| 1.3.1.1 | [reg1](#1.2.3.0) | 0x00000000 | 0x44 |  |
| 1.3.1.2 | [reg2](#1.2.3.1.0) | 0x00000000 | 0x48 |  |
| 1.3.2 | [reg1](#1.2.3.1.1.0) | 0x00000000 | 0x4C |  |
| 1 | [chip1](#1.2.3.1.2.0) |  | 0x00 |  |
| 1.1 | [block421](#1.0) |  | 0x00 |  |
| 1.1.1 | [reggroup1](#1.1.0) |  | 0x00 |  |
| 1.1.2 | [reg1](#1.1.1.0) | 0x00000000 | 0x28 |  |
| 1.2 | [block1](#1.0) |  | 0x2C |  |
| 1.2.1 | [reggroup1](#1.1.0) |  | 0x2C |  |
| 1.2.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x2C |  |
| 1.2.1.2 | [reg2](#1.0) | 0x00000000 | 0x30 |  |
| 1.2.2 | [reg1](#1.1.0) | 0x00000000 | 0x34 |  |
| 1.2.3 | [block2](#1.1.1.0) |  | 0x38 |  |
| 1.2.3.1 | [reggroup1](#1.1.2.0) |  | 0x38 |  |
| 1.2.3.1.1 | [reg1](#1.2.0) | 0x00000000 | 0x38 |  |
| 1.2.3.1.2 | [reg2](#1.2.1.0) | 0x00000000 | 0x3C |  |
| 1.2.3.2 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x40 |  |
| 1.3 | [block3](#1.2.1.2.0) |  | 0x44 |  |
| 1.3.1 | [reggroup1](#1.2.2.0) |  | 0x44 |  |
| 1.3.1.1 | [reg1](#1.2.3.0) | 0x00000000 | 0x44 |  |
| 1.3.1.2 | [reg2](#1.2.3.1.0) | 0x00000000 | 0x48 |  |
| 1.3.2 | [reg1](#1.2.3.1.1.0) | 0x00000000 | 0x4C |  |
| 1 | [chip1](#1.2.3.1.2.0) |  | 0x00 |  |
| 1.1 | [block421](#1.0) |  | 0x00 |  |
| 1.1.1 | [reggroup1](#1.1.0) |  | 0x00 |  |
| 1.1.2 | [reg1](#1.1.1.0) | 0x00000000 | 0x28 |  |
| 1.2 | [block1](#1.0) |  | 0x2C |  |
| 1.2.1 | [reggroup1](#1.1.0) |  | 0x2C |  |
| 1.2.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x2C |  |
| 1.2.1.2 | [reg2](#1.0) | 0x00000000 | 0x30 |  |
| 1.2.2 | [reg1](#1.1.0) | 0x00000000 | 0x34 |  |
| 1.2.3 | [block2](#1.1.1.0) |  | 0x38 |  |
| 1.2.3.1 | [reggroup1](#1.1.2.0) |  | 0x38 |  |
| 1.2.3.1.1 | [reg1](#1.2.0) | 0x00000000 | 0x38 |  |
| 1.2.3.1.2 | [reg2](#1.2.1.0) | 0x00000000 | 0x3C |  |
| 1.2.3.2 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x40 |  |
| 1.3 | [block3](#1.2.1.2.0) |  | 0x44 |  |
| 1.3.1 | [reggroup1](#1.2.2.0) |  | 0x44 |  |
| 1.3.1.1 | [reg1](#1.2.3.0) | 0x00000000 | 0x44 |  |
| 1.3.1.2 | [reg2](#1.2.3.1.0) | 0x00000000 | 0x48 |  |
| 1.3.2 | [reg1](#1.2.3.1.1.0) | 0x00000000 | 0x4C |  |
| 1 | [chip1](#1.2.3.1.2.0) |  | 0x00 |  |
| 1.1 | [block421](#1.0) |  | 0x00 |  |
| 1.1.1 | [reggroup1](#1.1.0) |  | 0x00 |  |
| 1.1.2 | [reg1](#1.1.1.0) | 0x00000000 | 0x28 |  |
| 1.2 | [block1](#1.0) |  | 0x2C |  |
| 1.2.1 | [reggroup1](#1.1.0) |  | 0x2C |  |
| 1.2.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x2C |  |
| 1.2.1.2 | [reg2](#1.0) | 0x00000000 | 0x30 |  |
| 1.2.2 | [reg1](#1.1.0) | 0x00000000 | 0x34 |  |
| 1.2.3 | [block2](#1.1.1.0) |  | 0x38 |  |
| 1.2.3.1 | [reggroup1](#1.1.2.0) |  | 0x38 |  |
| 1.2.3.1.1 | [reg1](#1.2.0) | 0x00000000 | 0x38 |  |
| 1.2.3.1.2 | [reg2](#1.2.1.0) | 0x00000000 | 0x3C |  |
| 1.2.3.2 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x40 |  |
| 1.3 | [block3](#1.2.1.2.0) |  | 0x44 |  |
| 1.3.1 | [reggroup1](#1.2.2.0) |  | 0x44 |  |
| 1.3.1.1 | [reg1](#1.2.3.0) | 0x00000000 | 0x44 |  |
| 1.3.1.2 | [reg2](#1.2.3.1.0) | 0x00000000 | 0x48 |  |
| 1.3.2 | [reg1](#1.2.3.1.1.0) | 0x00000000 | 0x4C |  |
| 1.3.3 | [reg\_name\_7](#1.2.3.1.2.0) | 0x00 | 0x50 |  |
| 1.3.4 | [reg\_name](#1.2.3.2.0) | 0x0000000000000000 | 0x51 |  |
| 1 | [chip1](#1.3.0) |  | 0x00 |  |
| 1.1 | [block421](#1.0) |  | 0x00 |  |
| 1.1.1 | [reggroup1](#1.1.0) |  | 0x00 |  |
| 1.1.2 | [reg1](#1.1.1.0) | 0x00000000 | 0x28 |  |
| 1.2 | [block1](#1.0) |  | 0x2C |  |
| 1.2.1 | [reggroup1](#1.1.0) |  | 0x2C |  |
| 1.2.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x2C |  |
| 1.2.1.2 | [reg2](#1.0) | 0x00000000 | 0x30 |  |
| 1.2.2 | [reg1](#1.1.0) | 0x00000000 | 0x34 |  |
| 1.2.3 | [block2](#1.1.1.0) |  | 0x38 |  |
| 1.2.3.1 | [reggroup1](#1.1.2.0) |  | 0x38 |  |
| 1.2.3.1.1 | [reg1](#1.2.0) | 0x00000000 | 0x38 |  |
| 1.2.3.1.2 | [reg2](#1.2.1.0) | 0x00000000 | 0x3C |  |
| 1.2.3.2 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x40 |  |
| 1.3 | [block3](#1.2.1.2.0) |  | 0x44 |  |
| 1.3.1 | [reggroup1](#1.2.2.0) |  | 0x44 |  |
| 1.3.1.1 | [reg1](#1.2.3.0) | 0x00000000 | 0x44 |  |
| 1.3.1.2 | [reg2](#1.2.3.1.0) | 0x00000000 | 0x48 |  |
| 1.3.2 | [reg1](#1.2.3.1.1.0) | 0x00000000 | 0x4C |  |
| 1.3.3 | [reg\_name\_7](#1.2.3.1.2.0) | 0x00 | 0x50 |  |
| 1.3.4 | [reg\_name](#1.2.3.2.0) | 0x0000000000000000 | 0x51 |  |
| 1 | [chip1](#1.3.0) |  | 0x00 |  |
| 1.1 | [block421](#1.0) |  | 0x00 |  |
| 1.1.1 | [reggroup1](#1.1.0) |  | 0x00 |  |
| 1.1.2 | [reg1](#1.1.1.0) | 0x00000000 | 0x28 |  |
| 1.2 | [block1](#1.0) |  | 0x2C |  |
| 1.2.1 | [reggroup1](#1.1.0) |  | 0x2C |  |
| 1.2.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x2C |  |
| 1.2.1.2 | [reg2](#1.0) | 0x00000000 | 0x30 |  |
| 1.2.2 | [reg1](#1.1.0) | 0x00000000 | 0x34 |  |
| 1.2.3 | [block2](#1.1.1.0) |  | 0x38 |  |
| 1.2.3.1 | [reggroup1](#1.1.2.0) |  | 0x38 |  |
| 1.2.3.1.1 | [reg1](#1.2.0) | 0x00000000 | 0x38 |  |
| 1.2.3.1.2 | [reg2](#1.2.1.0) | 0x00000000 | 0x3C |  |
| 1.2.3.2 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x40 |  |
| 1.3 | [block3](#1.2.1.2.0) |  | 0x44 |  |
| 1.3.1 | [reggroup1](#1.2.2.0) |  | 0x44 |  |
| 1.3.1.1 | [reg1](#1.2.3.0) | 0x00000000 | 0x44 |  |
| 1.3.1.2 | [reg2](#1.2.3.1.0) | 0x00000000 | 0x48 |  |
| 1.3.2 | [reg1](#1.2.3.1.1.0) | 0x00000000 | 0x4C |  |
| 1.3.3 | [reg\_name\_7](#1.2.3.1.2.0) | 0x00 | 0x50 |  |
| 1 | [chip1](#1.2.3.2.0) |  | 0x00 |  |
| 1.1 | [block421](#1.0) |  | 0x00 |  |
| 1.1.1 | [reggroup1](#1.1.0) |  | 0x00 |  |
| 1.1.2 | [reg1](#1.1.1.0) | 0x00000000 | 0x28 |  |
| 1.2 | [block1](#1.0) |  | 0x2C |  |
| 1.2.1 | [reggroup1](#1.1.0) |  | 0x2C |  |
| 1.2.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x2C |  |
| 1.2.1.2 | [reg2](#1.0) | 0x00000000 | 0x30 |  |
| 1.2.2 | [reg1](#1.1.0) | 0x00000000 | 0x34 |  |
| 1.2.3 | [block2](#1.1.1.0) |  | 0x38 |  |
| 1.2.3.1 | [reggroup1](#1.1.2.0) |  | 0x38 |  |
| 1.2.3.1.1 | [reg1](#1.2.0) | 0x00000000 | 0x38 |  |
| 1.2.3.1.2 | [reg2](#1.2.1.0) | 0x00000000 | 0x3C |  |
| 1.2.3.2 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x40 |  |
| 1.3 | [block3](#1.2.1.2.0) |  | 0x44 |  |
| 1.3.1 | [reggroup1](#1.2.2.0) |  | 0x44 |  |
| 1.3.1.1 | [reg1](#1.2.3.0) | 0x00000000 | 0x44 |  |
| 1.3.1.2 | [reg2](#1.2.3.1.0) | 0x00000000 | 0x48 |  |
| 1.3.2 | [reg1](#1.2.3.1.1.0) | 0x00000000 | 0x4C |  |
| 1.3.3 | [reg\_name\_7](#1.2.3.1.2.0) | 0x00 | 0x50 |  |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1.0 | | | chip1 | | chip |  |
| offset | 0 | external | |  | size | 81 |
|  | | | | | | |
|  | | | | | | |
| {diff\_regwidth=true} | | | | | | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1.1.0 | | | block421 | | block |  |
| offset | 0 | external | |  | size | 44 |
|  | | | | | | |
|  | | | | | | |
| , | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.1.0 | | | | reggroup1 | | | mem | | |  |
| offset | 0 | depth | 10 | | width | 32 | | default | 00000000000000000000000000000000 | |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| {type=mem;external=true;memwidth=32;count=10;max\_reg\_size=32} | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 40 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| , | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 3 | f2 | | | ro | rw | | 0x0 | | |  | | | | | |
| 1:0 | f1 | | | ro | rw | | 0x0 | | |  | | | | | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1.1.0 | | | block1 | | block |  |
| offset | 44 | external | |  | size | 24 |
|  | | | | | | |
|  | | | | | | |
|  | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.1.0 | | | | reggroup1 | | | section | |  | |
| offset | 0 | external |  | | repeat |  | | size | | 8 |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| {max\_reg\_size=32} | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| , | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | rw | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | rw | rw | | 0x0 | | | {next=reg2.f2} | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.0 | | | | | | | | reg2 | | | | | reg32 | |  |
| offset | | 4 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | rw | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | rw | rw | | 0x0 | | |  | | | | | |

|  |
| --- |
| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 8 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| , | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | ro | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | ro | rw | | 0x0 | | |  | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.2.0 | | | | block2 | | | section | |  | |
| offset | 12 | external |  | | repeat |  | | size | | 12 |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| {type=subblock;refnodetype=section} | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.0 | | | | reggroup1 | | | section | |  | |
| offset | 0 | external |  | | repeat |  | | size | | 8 |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| {max\_reg\_size=32;context=block2} | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| , | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | rw | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | rw | rw | | 0x0 | | | {next=reg2.f2} | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1.1.0 | | | | | | | | reg2 | | | | | reg32 | |  |
| offset | | 4 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | rw | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | rw | rw | | 0x0 | | |  | | | | | |

|  |
| --- |
| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1.2.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 8 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| , | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | ro | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | ro | rw | | 0x0 | | |  | | | | | |

|  |
| --- |
| End RegGroup |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1.2.2.0 | | | block3 | | block |  |
| offset | 68 | external | |  | size | 13 |
|  | | | | | | |
|  | | | | | | |
|  | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.0 | | | | reggroup1 | | | section | |  | |
| offset | 0 | external |  | | repeat |  | | size | | 8 |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| {max\_reg\_size=32} | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| , | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | ro | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | ro | rw | | 0x0 | | |  | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.1.1.0 | | | | | | | | reg2 | | | | | reg32 | |  |
| offset | | 4 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | ro | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | ro | rw | | 0x0 | | |  | | | | | |

|  |
| --- |
| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.1.2.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 8 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| , | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:16 | f2 | | | ro | rw | | 0x0 | | |  | | | | | |
| 15:0 | f1 | | | ro | rw | | 0x0 | | |  | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.3.2.0 | | | | | | | | reg\_name\_7 | | | | | reg32 | |  |
| offset | | 12 | external | | |  | | | size | | 8 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 6:1 | f | | | rw | ro | | 0x0 | | |  | | | | | |