|  |  |  |  |  |
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| 1.1 | [block1](#1.1.0) |  | 0x00 |  |
| 1.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x00 |  |
| 1.1.2 | [reggroup1](#1.1.2.0) |  | 0x04 |  |
| 1.1.2.1 | [reg1](#1.1.2.1.0) | 0x00000000 | 0x04 |  |
| 1.1.2.2 | [reg2](#1.1.2.2.0) | 0x00000000 | 0x08 |  |
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| 1.2.1 | [reggroup1](#1.2.1.0) |  | 0x0C |  |
| 1.2.1.1 | [reg1](#1.2.1.1.0) | 0x00000000 | 0x0C |  |
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| 1.2.2 | [ref\_name](#1.2.2.0) |  | 0x14 |  |
| 1.2.2.1 | [reg1](#1.2.2.1.0) | 0x00000000 | 0x14 |  |
| 1.2.2.2 | [reggroup1](#1.2.2.2.0) |  | 0x18 |  |
| 1.2.2.2.1 | [reg1](#1.2.2.2.1.0) | 0x00000000 | 0x18 |  |
| 1.2.2.2.2 | [reg2](#1.2.2.2.2.0) | 0x00000000 | 0x1C |  |
| 1 | [chip\_name](#1.0) |  | 0x00 |  |
| 1.1 | [block1](#1.1.0) |  | 0x00 |  |
| 1.1.1 | [reg1](#1.1.1.0) | 0x00000000 | 0x00 |  |
| 1.1.2 | [reggroup1](#1.1.2.0) |  | 0x04 |  |
| 1.1.2.1 | [reg1](#1.1.2.1.0) | 0x00000000 | 0x04 |  |
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| 1.2.1.2 | [reg2](#1.2.1.2.0) | 0x00000000 | 0x10 |  |
| 1.2.2 | [ref\_name](#1.2.2.0) |  | 0x14 |  |
| 1.2.2.1 | [reg1](#1.2.2.1.0) | 0x00000000 | 0x14 |  |
| 1.2.2.2 | [reggroup1](#1.2.2.2.0) |  | 0x18 |  |
| 1.2.2.2.1 | [reg1](#1.2.2.2.1.0) | 0x00000000 | 0x18 |  |
| 1.2.2.2.2 | [reg2](#1.2.2.2.2.0) | 0x00000000 | 0x1C |  |

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| --- | --- | --- | --- | --- | --- | --- |
| 1.0 | | | chip\_name | | chip |  |
| offset | 0 | external | |  | size | 32 |
|  | | | | | | |
|  | | | | | | |
| {coverage=on} | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- |
| 1.1.0 | | | block1 | | block |  |
| offset | 0 | external | |  | size | 12 |
|  | | | | | | |
|  | | | | | | |
| {hdl\_path=block1\_idsinst;abs\_hdl\_path=chip\_name\_ids.block1\_idsinst;coverage=on;max\_reg\_size=32} | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {hdl\_path=reg1;abs\_hdl\_path=chip\_name\_ids.block1\_idsinst.reg1;coverage=on} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | rw | rw | | 0x0 | | | {hdl\_path=\_fld\_q;abs\_hdl\_path=chip\_name\_ids.block1\_idsinst.reg1\_fld\_q} | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.2.0 | | | | reggroup1 | | | section | |  | |
| offset | 4 | external |  | | repeat |  | | size | | 8 |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| {coverage=on;max\_reg\_size=32} | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.2.1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {hdl\_path=reggroup1\_reg1;abs\_hdl\_path=chip\_name\_ids.block1\_idsinst.reggroup1\_reg1;coverage=on} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | rw | rw | | 0x0 | | | {hdl\_path=\_fld\_q;abs\_hdl\_path=chip\_name\_ids.block1\_idsinst.reggroup1\_reg1\_fld\_q} | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.2.2.0 | | | | | | | | reg2 | | | | | reg32 | |  |
| offset | | 4 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {hdl\_path=reggroup1\_reg2;abs\_hdl\_path=chip\_name\_ids.block1\_idsinst.reggroup1\_reg2;coverage=on} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld1 | | | rw | rw | | 0x0 | | | {hdl\_path=\_fld1\_q;abs\_hdl\_path=chip\_name\_ids.block1\_idsinst.reggroup1\_reg2\_fld1\_q} | | | | | |

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| End RegGroup |

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| --- | --- | --- | --- | --- | --- | --- |
| 1.2.0 | | | block2 | | block |  |
| offset | 12 | external | |  | size | 20 |
|  | | | | | | |
|  | | | | | | |
| {hdl\_path=block2\_idsinst;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst;coverage=on} | | | | | | |

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| 1.2.1.0 | | | | reggroup1 | | | section | |  | |
| offset | 0 | external |  | | repeat |  | | size | | 8 |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| {coverage=on;max\_reg\_size=32} | | | | | | | | | | |

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| 1.2.1.1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {hdl\_path=reggroup1\_reg1;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.reggroup1\_reg1;coverage=on} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | rw | rw | | 0x0 | | | {hdl\_path=\_fld\_q;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.reggroup1\_reg1\_fld\_q} | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1.2.0 | | | | | | | | reg2 | | | | | reg32 | |  |
| offset | | 4 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {hdl\_path=reggroup1\_reg2;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.reggroup1\_reg2;coverage=on} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld1 | | | rw | rw | | 0x0 | | | {hdl\_path=\_fld1\_q;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.reggroup1\_reg2\_fld1\_q} | | | | | |

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| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |
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| 1.2.2.0 | | | | ref\_name | | | section | |  | |
| offset | 8 | external |  | | repeat |  | | size | | 12 |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| , {type=subblock;refnodetype=section;coverage=on;max\_reg\_size=32} | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.2.1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {hdl\_path=ref\_name\_reg1;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.ref\_name\_reg1;coverage=on} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | rw | rw | | 0x0 | | | {hdl\_path=\_fld\_q;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.ref\_name\_reg1\_fld\_q} | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.2.2.0 | | | | reggroup1 | | | section | |  | |
| offset | 4 | external |  | | repeat |  | | size | | 8 |
|  | | | | | | | | | | |
|  | | | | | | | | | | |
| {coverage=on;max\_reg\_size=32;context=ref\_name} | | | | | | | | | | |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.2.2.1.0 | | | | | | | | reg1 | | | | | reg32 | |  |
| offset | | 0 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {hdl\_path=reggroup1\_reg1;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.reggroup1\_reg1;coverage=on} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | rw | rw | | 0x0 | | | {hdl\_path=\_fld\_q;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.reggroup1\_reg1\_fld\_q} | | | | | |

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| 1.2.2.2.2.0 | | | | | | | | reg2 | | | | | reg32 | |  |
| offset | | 4 | external | | |  | | | size | | 32 |  | |  | |
|  | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| {hdl\_path=reggroup1\_reg2;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.reggroup1\_reg2;coverage=on} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld1 | | | rw | rw | | 0x0 | | | {hdl\_path=\_fld1\_q;abs\_hdl\_path=chip\_name\_ids.block2\_idsinst.reggroup1\_reg2\_fld1\_q} | | | | | |

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| End RegGroup |

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| --- |
| End RegGroup |