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| 1 reg\_map | | | reg\_map | | block | 0x0 |
| offset | 0x0 | external | |  | size |  |
|  | | | | | | |
| oid=9a1eac54-688c-4231-94ea-1a8b63878181 | | | | | | |
| {output\_file\_name=reg\_map}  {module\_name=reg\_map}  {reset\_type=async}  {rtl.bit\_enable=true}  {rtl.byte\_enable=true}  {u\_field\_names=true}  {u\_use\_eeprom=true}  {gen\_pin\_complex\_functions=false}  {lock\_bitmask=true} | | | | | | |

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| 1.1 volatile | | | | volatile | | | section | | 0x0 | |
| offset | 0x0 | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=0310dafb-27c6-4937-9a7b-bfdf22477b2b | | | | | | | | | | |
|  | | | | | | | | | | |

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| 1.1.1 status\_0 | | | | | | | | | | | | | | | | | | | status\_0 | | | | | | | | | | | reg32 | | | | | | 0x0 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=4203b8bf-7b3b-4a3c-a187-5ced6cd2e7c5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test = true}  {no\_reg\_bit\_bash\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 3:0 | | dsc\_major | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Major Die Source Code**  This position will be selected once the shadow registers have loaded.  {hdl\_path = wrapper.u\_dig\_top.dsc\_major\_dft} | | | | | | | | | | | | | | | | | | | |
| 7:4 | | dsc\_minor | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Minor Die Source Code**  This position will be selected once the shadow registers have loaded.  {hdl\_path = wrapper.u\_dig\_top.dsc\_minor\_dft} | | | | | | | | | | | | | | | | | | | |
| 15:8 | | dsc\_rtl | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **RTL Die Source Code**  This position will be selected once the shadow registers have loaded.  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_dsc\_rtl\_tieoffs.dsc\_rtl} | | | | | | | | | | | | | | | | | | | |

**EEPROM Status/Control**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| 1.1.2 ee\_cfg | | | | | | | | | | | | | | | | | | | ee\_cfg | | | | | | | | | | | reg32 | | | | | | 0x1 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=e5fc3e7d-4cbe-4e71-94b7-06c727ab7bbe | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_cfg\_}  {no\_reg\_bit\_bash\_test=true} {no\_reg\_access\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | ee\_erase | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Setting this bit will perform an ERASE operation only on the EEPROM the next time an EEPROM address is written. It is self-clearing when the ERASE operation is complete.  {hdl\_path = ee\_erase\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 1 | | ee\_prog | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Setting this bit will perform a PROGRAM operation only on the EEPROM the next time an EEPROM address is written. ee\_erase has precedence, so if it is set this bit is ignored. It is self-clearing when the PROGRAM operation is complete.  {hdl\_path = ee\_prog\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 3:2 | | ee\_block\_mode | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 00: Single Word Write Access  01: Odd Word Write Access (address ignored)  10: Even Word Write Access (address ignored)  11: All Word Write Access (address ignored)  This field only affects write operations.  {hdl\_path = ee\_block\_mode\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 6:4 | | ee\_vread | | | | | | | RW | | | | RO | | | | 0x0 | | | | | VREAD EEPROM setting per EEPROM V2.0 spec  {hdl\_path = ee\_vread\_q} | | | | | | | | | | | | | | | | | | | |
| 7 | | ee\_force\_sbe | | | | | | | RW | | | | RO | | | | 0x0 | | | | | Forces a single bit error  {hdl\_path = ee\_force\_sbe\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 8 | | ee\_force\_dbe | | | | | | | RW | | | | RO | | | | 0x0 | | | | | Forces a multi bit error  {hdl\_path = ee\_force\_dbe\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 9 | | ee\_dis\_ecc | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Correct Single bit errors when they occur  1: Do not correct single bit errors when they occur. Prevents single-bit and dual-bit error flags from being set.  {hdl\_path = ee\_dis\_ecc\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 10 | | ee\_no\_ecc | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Upper bits of EEPROM are written with calculated ECC bits.  1: ECC is disabled. No ECC calculation or correction will occur. Upper bits of EEPROM are written with data bits from ser\_data. Upper bits of read return upper bits from EEPROM.  {hdl\_path = ee\_no\_ecc\_q} | | | | | | | | | | | | | | | | | | | |
| 11 | | ee\_raw\_ecc | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: ECC bits encode error information  ECC bit 2: 1 if single bit error, 0 if no error  ECC bit 3: 1 if double bit error, 0 if not error  All other ECC bits are always 0  1: ECC bits return the ECC code (top bits in EEPROM)  {hdl\_path = ee\_raw\_ecc\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 12 | | ee\_en\_override | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Normal operation  1: Force ee\_en output high  {hdl\_path = ee\_en\_override\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 14:13 | | ee\_override | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 00: Normal operation  01: Force ee\_rd output high  10: Force ee\_er output high  11: Force ee\_pr output high  {hdl\_path = ee\_override\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 15 | | ee\_force\_reload | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Write to a 1 to reload all shadow registers with EEPROM values. If the noload ids\_top input or ee\_noload is set the reload will not occur. This bit is self-clearing after reload is completed.  {hdl\_path = ee\_force\_reload\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 16 | | ee\_noload | | | | | | | RW | | | | RO | | | | 0x0 | | | | | When set shadow will not update when EEPROM is written  {hdl\_path = ee\_noload\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 17 | | ee\_abort | | | | | | | RW | | | | RW | | | | 0x0 | | | | | When set the EEPROM controller will abort the current action return to idle. **This is only possible on designs with non-blocking EEPROM writes. Those with the define EEPROM\_WRITE\_BLOCKS set in** ids\_user\_defs **should not include this field.**  {hdl\_path = ee\_abort\_q}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |

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| 1.1.3 ee\_status0 | | | | | | | | | | | | | | | | | | | ee\_status0 | | | | | | | | | | | reg32 | | | | | | 0x2 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000400 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=ed979a26-d3ee-4937-91df-a9e3078594a7 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_status0\_}  {no\_reg\_hw\_reset\_test=true}  {no\_reg\_bit\_bash\_test=true}  {no\_reg\_access\_test=true}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | ee\_dbe\_flag | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Set if a dual bit error has occurred. ~~This bit is clear on read.~~ {hdl\_path = ee\_dbe\_flag\_q} | | | | | | | | | | | | | | | | | | | |
| 1 | | ee\_sbe\_flag | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Set if a single bit error has occurred. This bit is clear on read.  {hdl\_path = ee\_sbe\_flag\_q} | | | | | | | | | | | | | | | | | | | |
| 2 | | ee\_err | | | | | | | RC | | | | RW | | | | 0x0 | | | | | Error flag, goes high when an error occurs during an EEPROM write  {hdl\_path = ee\_err\_q} | | | | | | | | | | | | | | | | | | | |
| 7:3 | | ee\_err\_status | | | | | | | RO | | | | RW | | | | 0x0 | | | | | Status of when the last EEPROM error.  Bit 4:  0 – error occurred during erase  1 – error occurred during program  Bit 3:  0 – error occurred during Ramp Up  1 – error occurred during Ramp Down  Bit 2: Program Pulse value  Bit 1: hlat value  Bit 0: llat value  {hdl\_path = ee\_err\_status\_q} | | | | | | | | | | | | | | | | | | | |
| 10:8 | | ee\_addr | | | | | | | RW | | | | RW | | | | 0x4 | | | | | Contains the address for an EEPROM access, On a write or a read to EEPROM this register is updated with the access address.  {hdl\_path = ee\_addr\_q} | | | | | | | | | | | | | | | | | | | |
| 16:11 | | ee\_ecc | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Contains the ECC for an EEPROM access. On a write this register contains the written ECC, on a read this register contains the read ECC.  {hdl\_path = ee\_ecc\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.4 ee\_status1 | | | | | | | | | | | | | | | | | | | ee\_status1 | | | | | | | | | | | reg32 | | | | | | 0x3 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=159acfec-c21c-41ec-bd70-e4d13cf34f10 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_status1\_}  {no\_reg\_bit\_bash\_test=true} {no\_reg\_access\_test=true}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 25:0 | | ee\_data | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Contains the data for an EEPROM access.  On a write this register contains the written data  On a read this register contains the read data.  {hdl\_path = ee\_data\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.5 ee\_pat\_test | | | | | | | | | | | | | | | | | | | ee\_pat\_test | | | | | | | | | | | reg32 | | | | | | 0x4 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=3378d2e3-3e42-4c4d-8f0d-e1efbff0f476 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_pat\_test\_}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | pat\_test\_start | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Write to 1 to start pattern check testing. If EE\_LOOP is low, this bit will self-clear when the last address is reached. If EE\_LOOP is high, this bit must be written to 0 to stop test. This bit always clears on a fail.  {hdl\_path = pat\_test\_start\_q} | | | | | | | | | | | | | | | | | | | |
| 2:1 | | pat\_test\_status | | | | | | | RO | | | | WO | | | | 0x0 | | | | | Bits are cleared after a read or reset.  00: Reset condition (no result from pat testing)  01: Pass, no failure detected during pat testing  10: Fail, failure detected during pat testing  11: Running, pat test is still running  {hdl\_path = pat\_test\_status\_q} | | | | | | | | | | | | | | | | | | | |
| 4:3 | | pat\_test\_pattern | | | | | | | RW | | | | RO | | | | 0x0 | | | | | Defines the pattern that will be checked when reading the EEPROM.  00: all zeros  01: all ones  10: checker-board starting with zero (“010101…”)  11: checker-board starting with one (“101010…”)  {hdl\_path = pat\_test\_pattern\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.6 ee\_mar\_test | | | | | | | | | | | | | | | | | | | ee\_mar\_test | | | | | | | | | | | reg32 | | | | | | 0x5 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=5c5d81bb-b04a-4392-b6e6-d6e96f529fbf | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_mar\_test\_}  {lock=(shadow\_opt\_2.lock\_t & shadow\_opt\_2.lock\_a & shadow\_opt\_2.lock\_c & shadow\_opt\_2.lock\_o & shadow\_opt\_2.lock\_s & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | margin\_start | | | | | | | RW | | | | RW | | | | 0x0 | | | | | Write to 1 to start margin testing. If EE\_LOOP is low, this bit will self-clear when the last EEPROM address is reached. If EE\_LOOP is high, this bit must be written to 0 to stop test. This bit always clears on a fail.  {hdl\_path = margin\_start\_q} | | | | | | | | | | | | | | | | | | | |
| 1 | | margin\_no\_max | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Max reference voltage will be used during margin testing  1: Max voltage reference will be skipped during margin testing  {hdl\_path = margin\_no\_max\_q} | | | | | | | | | | | | | | | | | | | |
| 2 | | margin\_no\_min | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Min reference voltage will be used during margin testing  1: Min voltage reference will be skipped during margin testing  {hdl\_path = margin\_no\_min\_q} | | | | | | | | | | | | | | | | | | | |
| 4:3 | | margin\_status | | | | | | | RO | | | | WO | | | | 0x0 | | | | | Bits are cleared after a read or reset.  00: Reset condition (no result from margin testing)  01: Pass, no failure detected during margin testing  10: Fail, failure detected during margin testing  11: Running, margin test is still running  {hdl\_path = margin\_status\_q} | | | | | | | | | | | | | | | | | | | |
| 5 | | margin\_min\_max\_fail | | | | | | | RO | | | | WO | | | | 0x0 | | | | | If margining fails, this bit indicates if the min or max reference failed.  0: Min margining failed.  1: Max margining failed.  {hdl\_path = margin\_min\_max\_fail\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.7 ee\_test\_cfg | | | | | | | | | | | | | | | | | | | ee\_test\_cfg | | | | | | | | | | | reg32 | | | | | | 0x6 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=37caf7fa-7537-4f6a-8bed-b4d1f2b707de | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_ee\_test\_cfg\_}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | ee\_loop | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Test completes at final address or fail  1: Test loops until MARGIN\_START is written low or fail.  {hdl\_path = ee\_loop\_q} | | | | | | | | | | | | | | | | | | | |
| 1 | | ee\_use\_test\_addr | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: No effect  1: Uses EE\_TST\_ADDR as the start address for margin/pattern test.  If EE\_LOOP is set, this bit is ignored and the starting address is always 0x0  {hdl\_path = ee\_use\_test\_addr\_q} | | | | | | | | | | | | | | | | | | | |
| 4:2 | | ee\_test\_addr | | | | | | | RW | | | | RO | | | | 0x0 | | | | | If USE\_TST\_ADDR is set, then margining or check testing will start at this address. If the test fails, this will contain the failing address.  {hdl\_path = ee\_test\_addr\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.8 mux\_control | | | | | | | | | | | | | | | | | | | mux\_control | | | | | | | | | | | reg32 | | | | | | 0x7 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=c66f8d5f-4300-4692-9e9c-028cb4503550 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_mux\_control\_}  {lock=(shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | rma\_mux1\_override\_en | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Normal MUX operation  1: MUX control driven directly by register values  {hdl\_path = rma\_mux1\_override\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 2:1 | | rma\_mux1\_override\_dig | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 00: Output driven to Logic-Low  01: **If MUX disabled: Mandatory** | If MUX enabled: Invalid  10: Output driven by Analog  11: Output driven to Logic-High  {hdl\_path = rma\_mux1\_override\_dig\_q} | | | | | | | | | | | | | | | | | | | |
| 8:3 | | rma\_mux1\_override\_ctrl | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Unreferenced i.e. floating  1: MUX driven by DAC  2: Differential signal referenced to Mid-Scale  4: Single Ended signal referenced to VPOS (VPOS-input)  8: Single Ended signal referenced to VNEG (VNEG-input)  16: No signal: Output driven to Mid-Scale  34: Differential signal referenced to 0 V  All Other Values: Invalid  {hdl\_path = rma\_mux1\_override\_ctrl\_q} | | | | | | | | | | | | | | | | | | | |
| 9 | | rma\_mux2\_override\_en | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Normal MUX operation  1: MUX control driven directly by register values  {hdl\_path = rma\_mux2\_override\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 11:10 | | rma\_mux2\_override\_dig | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 00: Output driven to Logic-Low  01: **If MUX disabled: Mandatory** | If MUX enabled: Invalid  10: Output driven by Analog  11: Output driven to Logic-High  {hdl\_path = rma\_mux2\_override\_dig\_q} | | | | | | | | | | | | | | | | | | | |
| 17:12 | | rma\_mux2\_override\_ctrl | | | | | | | RW | | | | RO | | | | 0x0 | | | | | 0: Unreferenced i.e. floating  1: MUX driven by DAC  2: Differential signal referenced to Mid-Scale  4: Single Ended signal referenced to VPOS (VPOS-input)  8: Single Ended signal referenced to VNEG (VNEG-input)  16: No signal: Output driven to Mid-Scale  34: Differential signal referenced to 0 V  All Other Values: Invalid  {hdl\_path = rma\_mux2\_override\_ctrl\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.9 test\_control | | | | | | | | | | | | | | | | | | | test\_control | | | | | | | | | | | reg32 | | | | | | 0x8 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
| Coverage | | | | | | | on | | | | | | | |  | | | | | | | | |  | | | | | |  | | | | | |  | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=57ce969e-1a9a-41a2-9fa4-507c2669f1c9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_test\_control\_}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 11:0 | | rma\_dac\_direct | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **DAC Direct**  Allows diagnostic DAC to be driven directly from a register.  NOTE: drives both mux1 and mux2 DACS.  NOTE: Muxes mux be set to rma\_dac\_direct\_r position  {hdl\_path = rma\_dac\_direct\_q} | | | | | | | | | | | | | | | | | | | |
| 12 | | rma\_pulse\_train\_en | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Enable Pulse Train**  Setting this bit causes the controller to continuously transmit back-to-back pulses of the type specified by rma\_pulse\_train\_sel (see below).  NOTE: The time interval between pulses will be the minimum as specified by the selected protocol.  NOTE: The pulse width will obey any optional parameter (e.g. ~~Allegro “N” vs “W”~~ opt\_fwd\_width)  ~~NOTE: rma\_force\_highspeed can be enabled to get the high-speed variant of each pulse.~~  {hdl\_path = rma\_pulse\_train\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 15:13 | | rma\_pulse\_train\_sel | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Pulse Train Select**  Options 0-4 include the 45us off time. Options 5-7 have a 0.3us off time (1 clock cycle). Options 6-7 do not result in safe state currents, so icc\_en and icc\_im are set to 1 during the pulse.  0 = Forward  1 = Reverse  2 = Forward (EL)  3 = Reverse (EL)  4 = Warning  5 = Standstill  6 = Critical Fail  7 = Soft Fail  ~~2 = Non-Direction~~  ~~3 = Kefico Diag Flag~~  ~~4 = Critical~~  ~~5 = Soft Fail~~  ~~6 = Half Diag-Bit~~  ~~7 =~~ *~~RESERVED~~*  {hdl\_path = rma\_pulse\_train\_sel\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.10 asil\_diag | | | | | | | | | | | | | | | | | | | asil\_diag | | | | | | | | | | | reg32 | | | | | | 0x9 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=ceb2c963-6f40-4aa8-8586-f6ee8a53fe70 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.volatile\_asil\_diag\_}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 1:0 | | force\_asil\_diag\_fe\_l | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force front-end error left**  This option is OR’d with the force\_asil\_diag\_fe\_l, which is why there is no output coupling (see bug 7657)  {hdl\_path = force\_asil\_diag\_fe\_l\_q} | | | | | | | | | | | | | | | | | | | |
| 3:2 | | force\_asil\_diag\_fe\_r | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force front-end error right**  {hdl\_path = force\_asil\_diag\_fe\_r\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 5:4 | | force\_asil\_diag\_sdm1 | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force filter saturation left error**  0x = Force disabled  10 = Override SDM input with zeros  11 = Override SDM input with ones  {hdl\_path = force\_asil\_diag\_sdm1\_q} | | | | | | | | | | | | | | | | | | | |
| 7:6 | | force\_asil\_diag\_sdm2 | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force filter saturation right error**  0x = Force disabled  10 = Override SDM input with zeros  11 = Override SDM input with ones  {hdl\_path = force\_asil\_diag\_sdm2\_q} | | | | | | | | | | | | | | | | | | | |
| 8 | | force\_asil\_diag\_vreg | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force analog voltage regulator error**  {hdl\_path = force\_asil\_diag\_vreg\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 9 | | force\_asil\_diag\_vregd | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force digital voltage regulator error**  {hdl\_path = force\_asil\_diag\_vregd\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 10 | | force\_asil\_diag\_ibias | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force IBIAS error**  {hdl\_path = force\_asil\_diag\_ibias\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 11 | | force\_asil\_diag\_im | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force ICC 14 mA Comparator Error**  {hdl\_path = force\_asil\_diag\_im\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 12 | | force\_asil\_diag\_hdrive | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force HDRIVE drive error**  {hdl\_path = force\_asil\_diag\_hdrive\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 13 | | force\_asil\_diag\_ob | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force Output Block error**  {hdl\_path = force\_asil\_diag\_ob\_q} | | | | | | | | | | | | | | | | | | | |
| 14 | | force\_asil\_diag\_overfreq | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force overfrequency error**  {hdl\_path = force\_asil\_diag\_overfreq\_q} | | | | | | | | | | | | | | | | | | | |
| 15 | | force\_asil\_diag\_collision | | | | | | | RW | | | | RO | | | | 0x0 | | | | | **Force pulse collision error**  {hdl\_path = force\_asil\_diag\_collision\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.1.11 ch1\_idiff | | | | | | | | | | | | | | | | | | | ch1\_idiff | | | | | | | | | | | reg32 | | | | | | 0xa | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=920f680b-5961-4c21-8af6-895b3a621fdc | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 15:0 | | ch1\_idiff | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Channel 1 I-Diff**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_channel\_1.u\_sdm\_filter.idiff} | | | | | | | | | | | | | | | | | | | |

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| 1.1.12 ch1\_npeak | | | | | | | | | | | | | | | | | | | ch1\_npeak | | | | | | | | | | | reg32 | | | | | | 0xb | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=51a53c69-caf6-4733-a141-f406a44d6c4c | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 15:0 | | ch1\_npeak | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Channel 1 N-Peak**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_channel\_1.u\_peak\_tracking.npeak} | | | | | | | | | | | | | | | | | | | |

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| 1.1.13 ch1\_ppeak | | | | | | | | | | | | | | | | | | | ch1\_ppeak | | | | | | | | | | | reg32 | | | | | | 0xc | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=601b2057-bd4d-4f68-a417-f26caf36c291 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 15:0 | | ch1\_ppeak | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Channel 1 P-Peak**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_channel\_1.u\_peak\_tracking.ppeak} | | | | | | | | | | | | | | | | | | | |

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| 1.1.14 ch1\_pk\_pk | | | | | | | | | | | | | | | | | | | ch1\_pk\_pk | | | | | | | | | | | reg32 | | | | | | 0xd | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=72b5f05e-0776-4ccc-9c69-eac01436386f | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 15:0 | | ch1\_pk\_pk | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Channel 1 Peak-to-Peak**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_channel\_1.u\_peak\_tracking.pk\_pk\_r} | | | | | | | | | | | | | | | | | | | |

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| 1.1.15 ch2\_idiff | | | | | | | | | | | | | | | | | | | ch2\_idiff | | | | | | | | | | | reg32 | | | | | | 0xe | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=9c596ec3-5aa9-4d6f-b1d8-49d2a919ab21 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 15:0 | | ch2\_idiff | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Channel 2 I-Diff**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_channel\_2.u\_sdm\_filter.idiff} | | | | | | | | | | | | | | | | | | | |

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| 1.1.16 ch2\_npeak | | | | | | | | | | | | | | | | | | | ch2\_npeak | | | | | | | | | | | reg32 | | | | | | 0xf | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=d40c3214-4372-49a7-bdf4-71ee219839c9 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 15:0 | | ch2\_npeak | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Channel 2 N-Peak**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_channel\_2.u\_peak\_tracking.npeak} | | | | | | | | | | | | | | | | | | | |

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| 1.1.17 ch2\_ppeak | | | | | | | | | | | | | | | | | | | ch2\_ppeak | | | | | | | | | | | reg32 | | | | | | 0x10 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=662676b5-4e94-4f05-8576-2db31932c6a2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 15:0 | | ch2\_ppeak | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Channel 2 P-Peak**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_channel\_2.u\_peak\_tracking.ppeak} | | | | | | | | | | | | | | | | | | | |

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| 1.1.18 ch2\_pk\_pk | | | | | | | | | | | | | | | | | | | ch2\_pk\_pk | | | | | | | | | | | reg32 | | | | | | 0x11 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=3ca22005-89b6-4985-830b-9ca4a7e9a521 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 15:0 | | ch2\_pk\_pk | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Channel 2 Peak-to-Peak**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_controller.u\_channel\_2.u\_peak\_tracking.pk\_pk\_r} | | | | | | | | | | | | | | | | | | | |

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| 1.1.19 unlock | | | | | | | | | | | | | | | | | | | unlock | | | | | | | | | | | reg32 | | | | | | 0x12 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | | true | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=f7a81319-e6d8-476b-82e4-f5b484830d88 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | unlock | | | | | | | RO | | | | WO | | | | 0x0 | | | | | **Unlock**  {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.unlock } | | | | | | | | | | | | | | | | | | | |

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| End RegGroup |

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| 1.2 shadow | | | | shadow | | | section | | 0x20 | |
| offset | 0x20 | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=23e30691-a41d-406f-a60e-d49514488229 | | | | | | | | | | |
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| 1.2.1 shadow\_trim\_0 | | | | | | | | | | | | | | | | | | | shadow\_trim\_0 | | | | | | | | | | | reg32 | | | | | | 0x20 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=a5ebbb29-3f88-49a8-a420-0377ad942e48 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.shadow\_shadow\_trim\_0\_}  {u\_shadow\_address = 0x34}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 4:0 | | trim\_osc | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {registered = false}  {hdl\_path = trim\_osc\_in} | | | | | | | | | | | | | | | | | | | |
| 9:5 | | trim\_icc\_low | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = trim\_icc\_low\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 13:10 | | trim\_icc\_high | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = trim\_icc\_high\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 18:14 | | trim\_sens | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = trim\_sens\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 22:19 | | trim\_mag\_tc | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = trim\_mag\_tc\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 24:23 | | trim\_icc\_tc | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = trim\_icc\_tc\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |
| 25 | | ibias\_diag\_analog\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = ibias\_diag\_analog\_en\_q}  {output\_coupling = true} | | | | | | | | | | | | | | | | | | | |

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| 1.2.2 shadow\_opt\_0 | | | | | | | | | | | | | | | | | | | shadow\_opt\_0 | | | | | | | | | | | reg32 | | | | | | 0x21 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=84baf4cd-a9a3-4532-8235-669efa00de4f | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_0\_}  {u\_shadow\_address = 0x35}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | opt\_sag\_timer\_disable | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_sag\_timer\_disable\_q} | | | | | | | | | | | | | | | | | | | |
| 1 | | opt\_sag\_timer\_run\_disable | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_sag\_timer\_run\_disable\_q} | | | | | | | | | | | | | | | | | | | |
| 3:2 | | rma\_out\_mode\_default | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = rma\_out\_mode\_default\_q} | | | | | | | | | | | | | | | | | | | |
| 4 | | rma\_mux\_to\_outpin | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = rma\_mux\_to\_outpin\_q} | | | | | | | | | | | | | | | | | | | |
| 11:5 | | rma\_mux1\_default | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = rma\_mux1\_default\_q} | | | | | | | | | | | | | | | | | | | |
| 18:12 | | rma\_mux1\_twowire\_default | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = rma\_mux1\_twowire\_default\_q} | | | | | | | | | | | | | | | | | | | |
| 25:19 | | rma\_mux2\_position | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = rma\_mux2\_position\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.2.3 shadow\_opt\_1 | | | | | | | | | | | | | | | | | | | shadow\_opt\_1 | | | | | | | | | | | reg32 | | | | | | 0x22 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=580279d2-a2cb-4e60-9dda-f95af28f8ed8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_1\_}  {u\_shadow\_address = 0x36}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 3:0 | | opt\_lockout\_sel | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_lockout\_sel\_q} | | | | | | | | | | | | | | | | | | | |
| 6:4 | | opt\_lockout\_hyst\_sel | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_lockout\_hyst\_sel\_q} | | | | | | | | | | | | | | | | | | | |
| 8:7 | | opt\_warn\_level\_sel | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_warn\_level\_sel\_q} | | | | | | | | | | | | | | | | | | | |
| 9 | | opt\_warn\_run\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_warn\_run\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 10 | | opt\_warn\_cal\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_warn\_cal\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 11 | | opt\_el\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_el\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 12 | | opt\_fwd\_width | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_fwd\_width\_q} | | | | | | | | | | | | | | | | | | | |
| 13 | | opt\_dir\_sel | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_dir\_sel\_q} | | | | | | | | | | | | | | | | | | | |
| 14 | | opt\_ch\_wd\_dis | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_ch\_wd\_dis\_q} | | | | | | | | | | | | | | | | | | | |
| 15 | | opt\_standstill\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_standstill\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 16 | | opt\_pk\_update\_sel | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = opt\_pk\_update\_sel\_q} | | | | | | | | | | | | | | | | | | | |
| 17 | | asil\_fe\_diag\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = asil\_fe\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 18 | | asil\_vreg\_diag\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = asil\_vreg\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 19 | | asil\_ibias\_diag\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = asil\_ibias\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 20 | | asil\_hdrive\_diag\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = asil\_hdrive\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 21 | | asil\_ob\_diag\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = asil\_ob\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 22 | | asil\_overfreq\_diag\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = asil\_overfreq\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 23 | | asil\_sat\_diag\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = asil\_sat\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 24 | | asil\_collision\_diag\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = asil\_collision\_diag\_en\_q} | | | | | | | | | | | | | | | | | | | |
| 25 | | asil\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **ASIL Global Enable**  {hdl\_path = asil\_en\_q} | | | | | | | | | | | | | | | | | | | |

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| 1.2.4 shadow\_opt\_2 | | | | | | | | | | | | | | | | | | | shadow\_opt\_2 | | | | | | | | | | | reg32 | | | | | | 0x23 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=dbd95608-b79e-4d9b-96db-97621403b938 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = wrapper.u\_dig\_top.u\_controller\_bist\_top.u\_controller\_top.}  {u\_shadow\_address = 0x37}  {no\_reg\_bit\_bash\_test=true}  {no\_reg\_access\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | lock\_bd | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_2\_lock\_bd\_q}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 1 | | lock\_t | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = lock\_t\_in}  {registered = false}  {lock = shadow\_opt\_2.lock\_t} | | | | | | | | | | | | | | | | | | | |
| 2 | | lock\_a | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = lock\_a\_in}  {registered = false}  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 3 | | lock\_c | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = lock\_c\_in}  {registered = false}  {lock = shadow\_opt\_2.lock\_c} | | | | | | | | | | | | | | | | | | | |
| 4 | | lock\_o | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = lock\_o\_in}  {registered = false}  {lock = shadow\_opt\_2.lock\_o} | | | | | | | | | | | | | | | | | | | |
| 5 | | lock\_s | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = lock\_s\_in}  {registered = false}  {lock = shadow\_opt\_2.lock\_s} | | | | | | | | | | | | | | | | | | | |
| 6 | | out\_2wire | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_2\_out\_2wire\_in}  {registered = false}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 8:7 | | opt\_thresh\_monitor\_cnt | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_2\_opt\_thresh\_monitor\_cnt\_q}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 9 | | opt\_thresh\_monitor\_dis | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_2\_opt\_thresh\_monitor\_dis\_q}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 12:10 | | opt\_lockout\_startup\_standstill\_lor | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_2\_opt\_lockout\_startup\_standstill\_lor\_q}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 13 | | opt\_force\_asil\_diag\_sample | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_2\_opt\_force\_asil\_diag\_sample\_q}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 14 | | rma\_spare\_0 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {output\_coupling = true}  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_2\_rma\_spare\_0\_q}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 15 | | rma\_spare\_1 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **See EEPROM Section**  {output\_coupling = true}  {hdl\_path = u\_ids\_top.u\_reg\_map.shadow\_shadow\_opt\_2\_rma\_spare\_1\_q}  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |

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| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |
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| 1.3 eeprom | | | | eeprom | | | section | | 0x30 | |
| offset | 0x30 | external | true | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=7899b5d6-7923-450f-baab-d35c8bfe6619 | | | | | | | | | | |
| {no\_reg\_hw\_reset\_test=true}  new-----{wr\_rd\_valids=true} | | | | | | | | | | |

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| 1.3.1 factory\_0 | | | | | | | | | | | | | | | | | | | factory\_0 | | | | | | | | | | | reg32 | | | | | | 0x30 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=ade988bb-f9c3-4e86-8840-a51f30f6215b | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = u\_eeprom\_top.eeprom\_array.mem[0]}  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 25:0 | | factory\_0 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **reserved for factory production use** | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | RW | | | | RW | | | | 0x0 | | | | |  | | | | | | | | | | | | | | | | | | | |

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| 1.3.2 factory\_1 | | | | | | | | | | | | | | | | | | | factory\_1 | | | | | | | | | | | reg32 | | | | | | 0x31 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=1f24ff89-2d38-48c2-946a-c7c3e76e837d | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = u\_eeprom\_top.eeprom\_array.mem[1]}  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 25:0 | | factory\_1 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **reserved for factory production use** | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | RW | | | | RW | | | | 0x0 | | | | |  | | | | | | | | | | | | | | | | | | | |

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| 1.3.3 factory\_2 | | | | | | | | | | | | | | | | | | | factory\_2 | | | | | | | | | | | reg32 | | | | | | 0x32 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=617681eb-4c5d-4e0b-9892-544e2f8d7c3b | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = u\_eeprom\_top.eeprom\_array.mem[2]}  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 25:0 | | factory\_2 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **reserved for factory production use** | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | RW | | | | RW | | | | 0x0 | | | | |  | | | | | | | | | | | | | | | | | | | |

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| 1.3.4 factory\_3 | | | | | | | | | | | | | | | | | | | factory\_3 | | | | | | | | | | | reg32 | | | | | | 0x33 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=61d7585f-4ac1-43ca-887f-68187cd21489 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = u\_eeprom\_top.eeprom\_array.mem[3]}  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 25:0 | | factory\_3 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **reserved for factory production use** | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | RW | | | | RW | | | | 0x0 | | | | |  | | | | | | | | | | | | | | | | | | | |

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| 1.3.5 trim\_0 | | | | | | | | | | | | | | | | | | | trim\_0 | | | | | | | | | | | reg32 | | | | | | 0x34 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=70c93a92-8a06-4778-96af-61532efe95ee | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = u\_eeprom\_top.eeprom\_array.mem[4]}  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 4:0 | | trim\_osc | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Oscillator Trim** | | | | | | | | | | | | | | | | | | | |
| 9:5 | | trim\_icc\_low | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **ICC Low Trim** | | | | | | | | | | | | | | | | | | | |
| 13:10 | | trim\_icc\_high | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **ICC High Trim** | | | | | | | | | | | | | | | | | | | |
| 18:14 | | trim\_sens | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Sensitivity Trim** | | | | | | | | | | | | | | | | | | | |
| 22:19 | | trim\_mag\_tc | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Magnetic Temperature Compensation** | | | | | | | | | | | | | | | | | | | |
| 24:23 | | trim\_icc\_tc | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **ICC Temperature Compensation** | | | | | | | | | | | | | | | | | | | |
| 25 | | ibias\_diag\_analog\_en | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Enables Ibias diagnostic in analog**  0 = Ibias diagnostic ingored in analog  1 = ibias diagnostic causes immediate 3.5mA safe state. | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | RW | | | | RW | | | | 0x0 | | | | |  | | | | | | | | | | | | | | | | | | | |

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| 1.3.6 opt\_0 | | | | | | | | | | | | | | | | | | | opt\_0 | | | | | | | | | | | reg32 | | | | | | 0x35 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=17713370-c722-4e55-be9b-2c283e78f91b | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = u\_eeprom\_top.eeprom\_array.mem[5]}  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | opt\_sag\_timer\_disable | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **SAG Timer Watchdog Disable**  Resets the controller after 0.5 s if there is no activity on the output. | | | | | | | | | | | | | | | | | | | |
| 1 | | opt\_sag\_timer\_run\_disable | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **SAG Timer Watchdog in Running Mode Disable**  Disables the SAG Timer Watchdog in Running Mode | | | | | | | | | | | | | | | | | | | |
| 3:2 | | rma\_out\_mode\_default | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Default Output Mode at Power-up**  **NOTE:** Overridden by out\_2wire when out\_2wire is set to ‘one’  00 = switching enabled, mux enabled  01 = switching disabled, mux enabled  1x = switching disabled, mux disabled | | | | | | | | | | | | | | | | | | | |
| 4 | | rma\_mux\_to\_outpin | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Routes mux output signal to output pin**  0: mux signal only to mux pad  1: mux signal routed to output pin | | | | | | | | | | | | | | | | | | | |
| 11:5 | | rma\_mux1\_default | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Default MUX Position at Power-up for Mux1**  This position will be selected once the shadow registers have loaded. | | | | | | | | | | | | | | | | | | | |
| 18:12 | | rma\_mux1\_twowire\_default | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Default MUX Position at Power-up for Mux1 Two-Wire**  This position will be selected once the shadow registers have loaded. | | | | | | | | | | | | | | | | | | | |
| 25:19 | | rma\_mux2\_position | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **MUX Position for Mux2**  The secondary MUX (Mux2) does not respond to DMA commands. The position is exclusively selected via the shadow for this EEPROM field. | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | RW | | | | RW | | | | 0x0 | | | | |  | | | | | | | | | | | | | | | | | | | |

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| 1.3.7 opt\_1 | | | | | | | | | | | | | | | | | | opt\_1 | | | | | | | | | | | reg32 | | | | | | 0x36 | | | | | |
| offset | | | | | | |  | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=89f4ade9-a166-4e41-835f-404ee188c198 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = u\_eeprom\_top.eeprom\_array.mem[6]}  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 3:0 | | opt\_lockout\_sel | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Lockout Level Select**  Gauss level at which lockout is enabled.  Lockout is enabled at the lockout level minus the lockout hysteresis (see opt\_lockout\_hyst\_sel below).  Lockout is disable at the lockout level plus the lockout hysteresis (see opt\_lockout\_hyst\_sel below)  **Steps:** (10 – 40 G in 2 G steps)  0 = 10 G  1 = 12 G  **…**  14 = 38 G  15 = 0 G (NOTE: This position effectively disables lockout) | | | | | | | | | | | | | | | | | | | |
| 6:4 | | opt\_lockout\_hyst\_sel | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Lockout Hysteresis Select**  Hysteresis range around the lockout level (see opt\_lockout\_sel above)  **Steps:**  0 = ±2 G  1 = ±4 G  2 = ±6 G  3 = ±8 G  4 = ±10 G  5 = ±12 G  6 = ±14 G  7 = ±0 G (NOTE: This position effectively disabled lockout hysteresis) | | | | | | | | | | | | | | | | | | | |
| 8:7 | | opt\_warn\_level\_sel | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Warning Level Select**  0 = 1.5 x Lockout Release  1 = 2.0 x Lockout Release  2 = 27.5 G  3 = *RESERVED* | | | | | | | | | | | | | | | | | | | |
| 9 | | opt\_warn\_run\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Low-Field Warning Enable**  0 = low-field warning disabled  1 = low-field warning enabled (5x Lockout Release) | | | | | | | | | | | | | | | | | | | |
| 10 | | opt\_warn\_cal\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Startup Warning Enable**  0 = startup warning pulse disable  1 = startup warning pulse enable | | | | | | | | | | | | | | | | | | | |
| 11 | | opt\_el\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **EL Pulse Enable**  0 = EL pulses disabled  1 = EL pulses enabled | | | | | | | | | | | | | | | | | | | |
| 12 | | opt\_fwd\_width | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Direction Select**  0 = 90 µs  1 = 45 µs | | | | | | | | | | | | | | | | | | | |
| 13 | | opt\_dir\_sel | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Direction Select**  Configures the direction by swapping the two channels internally  ~~0 = Forward: pin 2 🡪 1~~  ~~1 = Forward: pin 1 🡪 2~~  0 = Channel 1 = Left Channel, Channel 2 = Right Channel  1 = Channel 1 = Right Channel, Channel 2 = Left Channel  In both configurations:  FWD = Channel 1 *lags* Channel 2  REV = Channel 1 *leads* Cannel 2 | | | | | | | | | | | | | | | | | | | |
| 14 | | opt\_ch\_wd\_dis | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Channel Watchdog Disable**  0 = channel watchdog enable  1 = channel watchdog disable | | | | | | | | | | | | | | | | | | | |
| 15 | | opt\_standstill\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Standstill Pulse Enable**  0 = standstill pulses disabled  1 = standstill pulses enabled | | | | | | | | | | | | | | | | | | | |
| 16 | | opt\_pk\_update\_sel | | | | | | | RW | | | RW | | | | 0x0 | | | | | **Inward Update Select for Running Mode**  0 = bounded  1= aggressive | | | | | | | | | | | | | | | | | | | |
| 17 | | asil\_fe\_diag\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Diagnostic Enable**  Enables Front End Diagnostics  **NOTE:** If the global ASIL enable bit is not set, this bit will have no effect. | | | | | | | | | | | | | | | | | | | |
| 18 | | asil\_vreg\_diag\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Diagnostic Enable**  Enables Voltage Regulator Diagnostic  **NOTE:** If the global ASIL enable bit is not set, this bit will have no effect. | | | | | | | | | | | | | | | | | | | |
| 19 | | asil\_ibias\_diag\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Diagnostic Enable**  Enables Bias Current Diagnostic  **NOTE:** If the global ASIL enable bit is not set, this bit will have no effect. | | | | | | | | | | | | | | | | | | | |
| 20 | | asil\_hdrive\_diag\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Diagnostic Enable**  Enables Hall Drive Diagnostic  **NOTE:** If the global ASIL enable bit is not set, this bit will have no effect. | | | | | | | | | | | | | | | | | | | |
| 21 | | asil\_ob\_diag\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Diagnostic Enable**  Enables Output Block Diagnostic Right  **NOTE:** If the global ASIL enable bit is not set, this bit will have no effect. | | | | | | | | | | | | | | | | | | | |
| 22 | | asil\_overfreq\_diag\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Diagnostic Enable**  Enables Over Frequency Diagnostic  **NOTE:** If the global ASIL enable bit is not set, this bit will have no effect. | | | | | | | | | | | | | | | | | | | |
| 23 | | asil\_sat\_diag\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Diagnostic Enable**  Enables Filter Saturation Diagnostic  **NOTE:** If the global ASIL enable bit is not set, this bit will have no effect. | | | | | | | | | | | | | | | | | | | |
| 24 | | asil\_collision\_diag\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Diagnostic Enable**  Enables Pulse Collsion Diagnostic  **NOTE:** If the global ASIL enable bit is not set, this bit will have no effect. | | | | | | | | | | | | | | | | | | | |
| 25 | | asil\_en | | | | | | | RW | | | RW | | | | 0x0 | | | | | **ASIL Global Enable**  Prevents device from going into safe-state | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | RW | | | RW | | | | 0x0 | | | | |  | | | | | | | | | | | | | | | | | | | |

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| 1.3.8 opt\_2 | | | | | | | | | | | | | | | | | | | opt\_2 | | | | | | | | | | | reg32 | | | | | | 0x37 | | | | | |
| offset | | | | | | |  | | | | | | | | external | | | | | | | | |  | | | | | | default | | | | | | 0x00000000 | | | | | |
|  | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| oid=e009ce9a-b262-4135-b3be-3e28243833aa | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| {hdl\_path = u\_eeprom\_top.eeprom\_array.mem[7]}  {no\_reg\_bit\_bash\_test=true}  {no\_reg\_access\_test=true} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 31 | 30 | | 29 | 28 | 27 | 26 | | 25 | | 24 | 23 | 22 | | 21 | | 20 | | 19 | | 18 | 17 | | 16 | 15 | 14 | 13 | 12 | 11 | 10 | | 9 | 8 | 7 | 6 | 5 | | 4 | 3 | 2 | 1 | 0 |
| bits | | name | | | | | | | s/w | | | | h/w | | | | default | | | | | description | | | | | | | | | | | | | | | | | | | |
| 0 | | lock\_bd | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Lock Backdoor Unlock**  – Disables the backdoor unlock (makes all locks final)  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 1 | | lock\_t | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Lock Test Modes**  – Disables access to the Allegro Test Modes and registers  {lock = (shadow\_opt\_2.lock\_t & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 2 | | lock\_a | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Allegro EEPROM Lock**  – Locks access to:   * Allegro factory traceability registers * Allegro factory trim registers   {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 3 | | lock\_c | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Customer EEPROM Lock**  – Locks access to the customer portion of the EEPROM  Note: Does not include the other customer accessible lock bits or the customer scratch register.  NOTE: This lock is not used on this device.  {lock = shadow\_opt\_2.lock\_c} | | | | | | | | | | | | | | | | | | | |
| 4 | | lock\_o | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Lock OEM End-of-Line Target Profiling Test Mode Access**  NOTE: This lock is not used on this device.  {lock = shadow\_opt\_2.lock\_o} | | | | | | | | | | | | | | | | | | | |
| 5 | | lock\_s | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Customer EEPROM Scratch Area Lock**  {lock = shadow\_opt\_2.lock\_s} | | | | | | | | | | | | | | | | | | | |
| 6 | | out\_2wire | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Sets the Default Output Mode**  0 = output determined by “outmode”:  (ee\_out\_mode\_default at power-up, otherwise tm\_outmode)  1 = operational output (“mission-mode”)  {lock = (shadow\_opt\_2.lock\_a & !unlock.unlock)} | | | | | | | | | | | | | | | | | | | |
| 8:7 | | opt\_thresh\_monitor\_cnt | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Threshold Monitor Count**  number of threshold monitor transitions, without threshold transitions, that will result in a soft reset  **Steps:**  0 = 2 counts **(DON’T USE THIS SETTING!)**  1 = 4 counts  2 = 8 counts  3 = 15 counts  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 9 | | opt\_thresh\_monitor\_dis | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Threshold Monitor Disable**  disables the threshold monitor  0 = enabled  1 = disabled  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 12:10 | | opt\_lockout\_startup\_standstill\_lor | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Denso LOR Option**  0 = 1x the configured LOR (effectively disables the feature)  1 = 2x the configured LOR  2 = 4x the configured LOR  3 = 6x the configured LOR  4 = 8x the configured LOR  5 = 10x the configured LOR  6 = 12x the configured LOR  7 = 14x the configured LOR  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 13 | | opt\_force\_asil\_diag\_sample | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Force ASIL Diag for Samples**  causes front end fault (left channel)  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 14 | | rma\_spare\_0 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Spare Allegro Trim Bit**  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 15 | | rma\_spare\_1 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Spare Allegro Trim Bit**  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 25:16 | | unused\_0 | | | | | | | RW | | | | RW | | | | 0x0 | | | | | **Unused**  {lock = shadow\_opt\_2.lock\_a} | | | | | | | | | | | | | | | | | | | |
| 31:26 | | ecc | | | | | | | RW | | | | RW | | | | 0x0 | | | | |  | | | | | | | | | | | | | | | | | | | |

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| End RegGroup |