|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Table of Content** | | | | |
| **Table of Content** | | | | |
| **Index** | **Component** | **Default** | **Address** | **Page** |
| 1 | [Chip1](#bookmark1) |  | 0x0 - 0x6 | 2 |
| 1.1 | [Block1](#bookmark2) |  | 0x0 - 0x3 | 2 |
| 1.1.1 | [Reg1](#bookmark3) | 0x00000000 | 0x0 | 2 |
| 1.1.2 | [Reg2](#bookmark4) | 0x00000000 | 0x1 | 2 |
| 1.1.3 | [Reg3](#bookmark5) | 0x00000000 | 0x2, 0x3 ... | 2 |
| 1.2 | [Block2](#bookmark6) |  | 0x4 - 0x6 | 3 |
| 1.2.1 | [reg\_group](#bookmark7) |  | 0x4 - 0x5 | 3 |
| 1.2.1.1 | [Reg1](#bookmark8) | 0x00000000 | 0x4 | 3 |
| 1.2.1.2 | [Reg2](#bookmark9) | 0x00000000 | 0x5 | 3 |
| 1.2.2 | [Reg3](#bookmark10) | 0x00000000 | 0x6 | 3 |

Here, we will start with an example which consist, one of the ways to describe the simple properties of this tool.

Contents

In-lineProperty Specification…………………………………………………………………………………………………………………2

Explicit Property Specification……………………………………………………………………………………………………………….3

**In this example clock\_edge, reset\_level, reset\_type and repeat properties are applied to blocks and registers**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1 Chip1 | | | Chip1 | | chip | 0x0 |
| offset |  | external | |  | size |  |
|  | | | | | | |
| oid=5b680dd8-8980-476d-ab05-69ca71efb561 | | | | | | |
|  | | | | | | |

**In-line Property specification**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 1.1 Block1 | | | Block1 | | block | 0x0 |
| offset |  | external | |  | size |  |
|  | | | | | | |
| oid=cad20127-e5d2-4c2a-b649-245f3bc854f6 | | | | | | |
| {clock\_edge=posedge; reset\_type=async}  New Description in Block | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.1 Reg1 | | | | | | | | Reg1 | | | | | reg32 | | 0x0 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=d21098d3-04bf-4531-a220-340ad03f4d11 | | | | | | | | | | | | | | | |
| {clock\_edge=negedge;reset\_type=sync} | | | | | | | | | | | | | | | |
| Bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.2 Reg2 | | | | | | | | Reg2 | | | | | reg32 | | 0x1 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=ee0aa2c0-a2ee-4d16-ae29-e433dadb9c9d | | | | | | | | | | | | | | | |
| {reset\_level=high} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.1.3 Reg3 | | | | | | | | Reg3 | | | | | reg32 | | 0x2, 0x3... |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=60bbe8e5-5542-490c-b871-a3b4d4976f15 | | | | | | | | | | | | | | | |
| {repeat=2} | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | fld | | | ro | rw | | 0 | | |  | | | | | |

**Explicitly Property Specification**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2 Block2 | | | Block2 | | block | 0x4 | | | | |
| offset |  | external | |  | size |  | | repest | | 2 |
| Clock\_edge | posedge | Reset\_level | | high |  |  | Reset\_type | | async | |
|  | | | | | | | | | | |
| oid=2c9ce19e-920f-462b-a869-c77968738e41 | | | | | | | | | | |
| New Description in Block2  New Description in Block | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1 reg\_group | | | | reg\_group | | | section | | 0x4 | |
| offset |  | external |  | | repeat |  | | size | |  |
|  | | | | | | | | | | |
| oid=11143c15-233a-4fd3-bc10-acd6f23fd57f | | | | | | | | | | |
| New Description in reg grp | | | | | | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1.1 Reg1 | | | | | | | | Reg1 | | | | | reg32 | | 0x4 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
|  | | | | | | | | | | | | | | | |
| oid=1eb666a6-2847-4a5c-90d6-dae7692f917c | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| Bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.1.2 Reg2 | | | | | | | | Reg2 | | | | | reg32 | | 0x5 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
| Reset\_type | | sync |  | | |  | | |  | |  |  | |  | |
|  | | | | | | | | | | | | | | | |
| oid=c1e0c1c0-977e-4ef1-875e-246bb52a16f1 | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld1 | | | ro | rw | | 0 | | |  | | | | | |

|  |
| --- |
| End RegGroup |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1.2.2 Reg3 | | | | | | | | Reg3 | | | | | reg32 | | 0x6 |
| offset | |  | external | | |  | | | size | | 32 | default | | 0x00000000 | |
| Clock\_edge | | posedge | Reset\_level | | | low | | |  | |  |  | |  | |
|  | | | | | | | | | | | | | | | |
| oid=0618537c-9459-4d21-8d83-ad0cbfb4a382 | | | | | | | | | | | | | | | |
|  | | | | | | | | | | | | | | | |
| bits | name | | | s/w | h/w | | default | | | description | | | | | |
| 31:0 | Fld | | | ro | rw | | 0 | | |  | | | | | |