Nitish Kumar Srivastava

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Education

Ph.D., ECE, Cornell University *Aug'14-Jan'20*
Advisors: Prof. Zhiru Zhang & Prof. David Albonesi
Topic: Design and Generation of Efficient Hardware Accelerators for Tensor Computations
GPA: 4.04/4.00

B.Tech, EE, Indian Institute of Technology, Kanpur *July'10-May'14*
Institute Rank 1, GPA: 10.0/10.0

Industry Internship

T2S-Tensor: Compiler for Mapping Dense Tensor Algebra on FPGAs *May'18-Dec'18*
Advisor: Dr. Hongbo Rong, Intel Parallel Computing Labs, Santa Clara, CA

- Created a domain specific language (T2S-Tensor) for generating spatial hardware for tensor algebra.
- Matrix multiplication design with just 10 lines of code matches performance of Intel IP.
- Shown 88-110% performance compared to hand-written ninja implementations of various workloads.
- Created backends for both Intel FPGAs via Opencl and Intel research CGRA.

Academic Research

Tensaurus: Accelerator for Mixed Sparse-Dense Tensor Computations *Oct'17-Aug'19*
Advisors: Dr. Zhiru Zhang and Dr. David Albonesi, ECE, Cornell University

- Designed a new sparse storage format that efficiently utilizes memory bandwidth.
- Determined common computation pattern in tensor kernels and implemented it in hardware.
- Showed performance and energy efficiency improvements over CPUs, GPUs and existing accelerartors.
- Implemented the design in both gem5 and RTL, and synthesized for area and energy analysis.

Operation Dependent Frequency Scaling using Desynchronization *June'15-April'18*
Advisor: Dr. Rajit Manohar, ECE, Cornell University

- Designed efficient clock network using asynchronous handshakes to dynamically scale the frequency.
- Enabled fine-grained frequency scaling of processor based on dynamic instruction stream.
- Used RISC-V rocket chip developed at U.C. Berkely to demonstrate the proposed methodology.

Accelerating Face Detection on Programmable SoC Using HLS *Jan'15-Feb'17*
Advisor: Dr. Zhiru Zhang, ECE, Cornell University

- Designed accelerator for Viola Jones face detection algorithm using High Level Synthesis.
- Achieved a frame rate of more than 30 fps suitable for realtime applications.
- Open sourced the design for HLS community (link).

Study of Resiliency in Asynchronous Pipelines under Variability *May'13-July'13*
Advisor: Dr. Peeter Beerel, ECE, University of Southern California

- Analyzed the variability effects on basic Asynchronous pipeline architectures and characterized them.
- Modelled the effects of delay variations on cycle time using probabilistic methods.
- Appeared in one of the keynote lectures given by my advisor in Japan

Dynamic Power Allocation Algorithm in Multi-beam Satellites *May'12-June'13*
Advisor: Dr. Ajit Chaturvedi, EE, Indian Institute of Technology, Kanpur

- Invented an efficient power allocation algorithm for broadband multi-beam satellites.
- Provided flexibility in obtaining a trade-off between performance and computational complexity.
- Showed the capability of the algorithm to yield optimum solution under various circumstances.

Course Projects

Pointer-Chase Prefetcher for Linked Data Structures *Mar'15-April'15*
Advisor: Dr. Christopher Batten, ECE, Cornell University

- Designed the hardware for Linked Data Structure prefetcher in Verilog.
- Extended the ISA to support compiler hints to prefetch graph nodes into the cache.
- Evaluated the design for power, energy and performance by passing it through the ASIC tool-flow.

Publications

- **Tensaurus: A Versatile Accelerator for Mixed Sparse-Dense Tensor Computations**
  Nitish Srivastava, Hanchen Jin, Shaden Smith, Hongbo Rong, David Albonesi, Zhiru Zhang
  to appear in International Symposium on High-Performance Computer Architecture (HPCA'2020)

- **T2S-Tensor: Productively Generating High-Performance Spatial Hardware for Dense Tensor Computations**
  Nitish Srivastava, Hongbo Rong, Prithayan Barua, Guanyu Feng, Huanqi Cao, Zhiru Zhang, David Albonesi, Vivek Sarkar, Wenguang Chen, Paul Petersen, Geoff Lowney, Adam Herr, Christopher Hughes, Timothy Mattson, Pradeep Dubey
  International Symposium on Field Programmable Custom Computing Machines (FCCM), 2019

- **Operation Dependent Frequency Scaling using Desynchronization**
  Nitish Srivastava and Rajit Manohar, IEEE, Transactions on VLSI systems (TVLSI), 2019

- **Rosetta: A Realistic HLS Benchmark Suite for Software Programmable FPGAs**
  Yuan Zhou, Udit Gupta, Steve Dai, Ritchie Zhao, Nitish Srivastava, Hanchen Jin, Joseph Featherston, Yi-Hsiang Lai, Gai Liu, Gustavo Angarita Velasquez, Wenping Wang, Zhiru Zhang
  International Symposium on Field Programmable Gate Arrays (FPGA), 2018

- **Accelerating Face Detection on Programmable SoC Using C-Based Synthesis.**
  Nitish Srivastava, Steve Dai, Rajit Manohar and Zhiru Zhang
  International Symposium on Field Programmable Gate Arrays (FPGA), 2017

- **Flexible and dynamic power allocation in broadband multi-beam satellites.**
  Nitish Srivastava, and A. K. Chaturvedi IEEE Communications Letters, 2013

Patents

Operation Dependent Frequency Scaling using Desynchronization (under process)

Paper Review

- **IEEE Transactions on Circuits and Systems-I (TCAS-I)**
  8 papers reviewed (7 direct invitations, 1 referred by advisor)
- **IEEE Transactions on Circuits and Systems-II (TCAS-II)**
  10 papers reviewed (all direct invitations)
- **IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)**
  2 papers reviewed (all direct invitations)
- **ACM Transactions on Design Automation of Electronic Systems (TODAES)**
  1 paper reviewed (referred by advisor)
- **ACM Transactions on Architecture and Code Optimizations (TACO)**
  1 paper reviewed (direct invitation)

Selected Awards

- Selected as a **Cornell Fellow** in 2014 for outstanding academic performance.
- **President's Gold Medal** for best academic performance in the graduating batch, 2014.
- **Proficiency Medal** and **Pratik Mishra Gold Medal** for the best performance in ECE 2014.
- Awarded **Viterbi scholarship** (20 selections all over India) in 2013.
- Selected for **Indo-German Winter Academy'12** (total 15 selections all over India).
- Selected for **SURGE-2012** research program at IIT Kanpur.
- **All India Rank (AIR) 364(99.99 percentile)** in IIT JEE'10.
- **District Topper** in Intermediate examination (CBSE board) in 2010.

Technical Skills

Hardware	Gem5, Verilog, Vivado HLS, Altera Opencl, BlueSpec, Synopsys CAD tools
Software	Halide, LLVM, Tensorflow, PyTorch, C, C++, Python, OpenMP, MPI, CUDA

Relevant Courses

Computer Architecture	Operating Systems	Compilers
Parallel Computing	Analysis of Algorithm	Advanced Machine Learning
High-Level Synthesis	Complex-ASIC Design	Digital VLSI