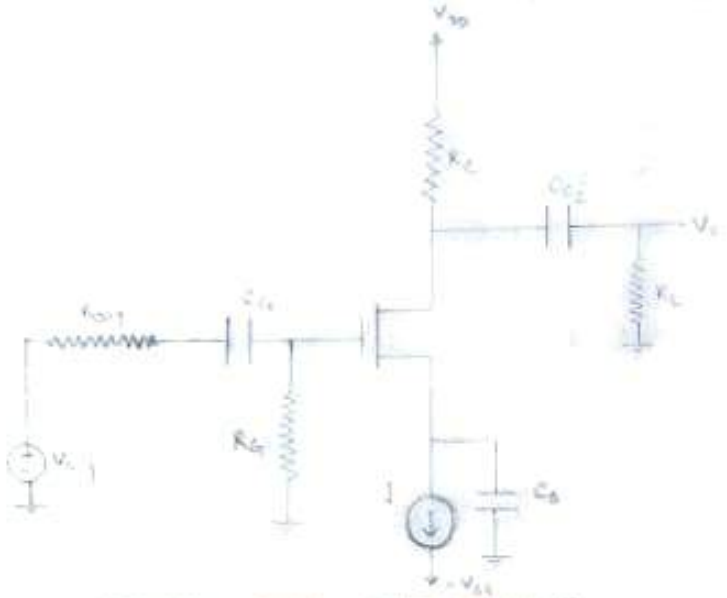
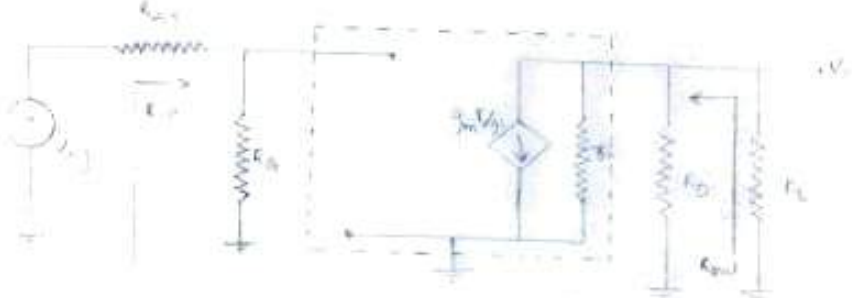


[COMMON SOURCE CONFIGURATION]



[SMALL SIGNAL MODEL]

EXPERIMENT NO - 5

- AIM OF THE EXPERIMENT :-

To design a RC Coupled amplifier using MOSFET (N-channel type) and calculate the parameters

a) DC Condition

b) Gain

c) Frequency response and bandwidth

- APPARATUS REQUIRED :-

a. Breadboard

b. CMOS IC 4007

c. DC power supply

d. Resistors

e. Capacitors

- THEORY :-

The Common Source (or grounded source) is the most widely used of all MOSFET amplifier circuits. A popular common source along with the signal ground bypass capacitor and coupling capacitor is shown in the figure. To determine the gain, we replace it with its corresponding small signal model

From the small signal model we can write

$$V_g = 0$$

$$R_{in} = R_G$$

$$V_o = V_{in} \left(\frac{R_D / R_L}{R_{sig} + R_{in}} \right)$$

· DISCUSSION :-

1. The Common Source Configuration is the best suited for you obtaining the bulk of the gain required in an amplifier.
2. Depending on the magnitude of the gain required either a single CS stage or a cascade of two or three CS stages can be used.
3. A Key step in the design of transistori amplifiers is to bias the transistor to operate at an appropriate point in the saturation region. A good bias design ensures that the parameters of the bias point I_D, V_{ov} and V_{DS} are predictable and stable and do not vary by a large amount when the transistor is replaced by another of the same type.
4. The internal Capacitances of the MOSFET cause the MOS amplifiers' gain to fall off at high frequencies.
5. Also, the coupling and bypass capacitors that are used in discrete MOS amplifiers cause the gain to fall off at low frequencies.
6. The frequency band over which both sets of Capacitances can be neglected and hence over which the gain is constant, is known as midband.
7. The amplifier frequency response is characterized by the midband gain A_m and the lower and upper 3 dB

frequencies f_L and f_H respectively and the bandwidth is $(f_H - f_L)$.

- **PRECAUTIONS:-**
  - The input signal amplitude must be judiously chosen such that the amplified output should not exceed the DC power supply otherwise the output will be clipped.
  - The DC bias point should be properly fixed else the output would not be symmetrical to the input signal variation.

- **CONCLUSION:-**

The circuit was implemented and output determined for a very broad range of frequencies. The frequency response was plotted and the bandwidth was found to be & error was about 0.7 %.

Observation table :-

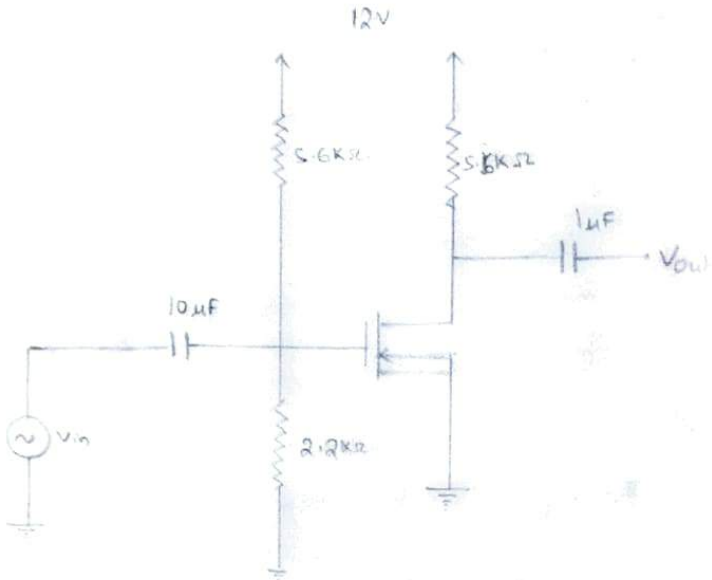
V_{in}	frequency	V_{out}	Gain (V_o/V_{in})	Gain in dB $20\log(V_o/V_{in})$
100mV	10 Hz	108 mV	1.08	0.66 dB
	50 Hz	464 mV	4.64	13.33 dB.
	100 Hz	960 mV	9.6	19.64 dB
	500 Hz	1 V	10	20
	1 KHz	1 V	10	20
	2KHz	1 V	10	20
	5 KHz	1 V	10	20
	7KHz	1 V	10	20
	10KHz	1 V	10	20
	20KHz	1 V	10	20
	50 KHz	1 V	10	20
	100KHz	920 mV	9.2	19.275
	200 KHz	728 mV	7.28	17.242
	500 KHz	400 mV	4	12.041
	1 MHz	2.24 mV	2.24	7.00

Experimental mid frequency Gain = 20 dB.

Theoritical Gain = 20.16 dB.

$$\% \text{ Error} = \frac{20.16 - 20}{20.16} \times 100 = 0.7\ \%$$

Bandwidth = $f_H - f_L$



$$V_G = 12 \times \frac{2.2}{2.2+5.6} = 12 \times \frac{2.2}{7.8} = 3.33\,V.$$

Usually R_G is selected very large (e.g. the MΩ range) with the result that in many applications $R_G \gg R_{sig}$ and

$$V_i \approx V_{sig}.$$

~~Hence, $V_{GS} = V_i$~~; The supply was 12 V.

$$I_D = \frac{12 - 2.1}{5.6\,K\Omega} = 1.71\,mA.$$

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times 1.71\,mA}{1.88} = 1.819\,mA/V$$

Assuming $V_t = 1.5\,V$.

Thus, the theoretical gain of the circuit was found to be $A_V = -g_m R_D$

$$= -1.819 \times 5.6\,K\Omega$$

$$= -10.1872\,(V/V)$$

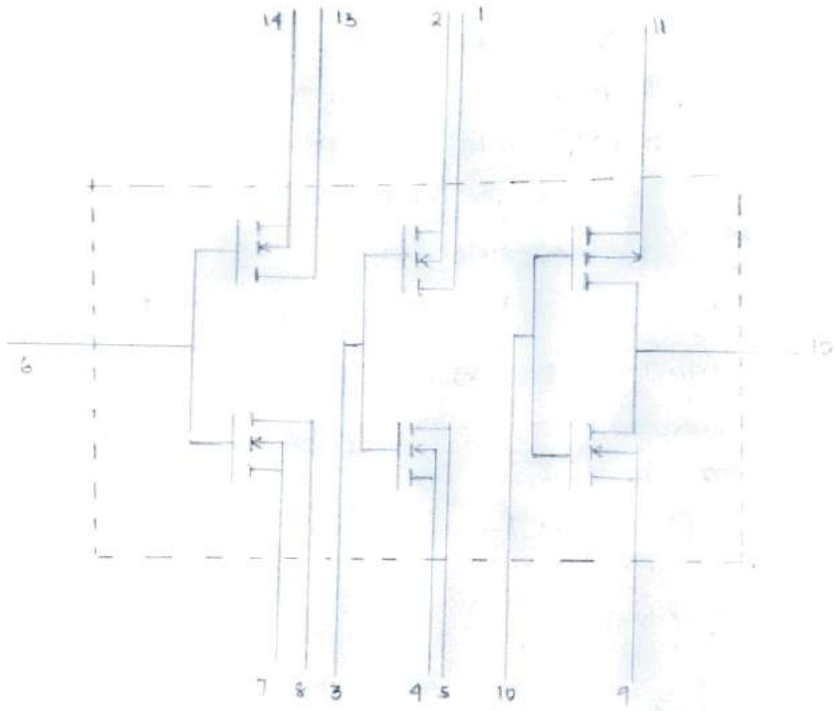
In decibels the gain was found to be 20.16 dB.

- Tabulation -

Starting frequency = 10 Hz.

Ending frequency = 1 MHz.

Input voltage $V_{PK\text{-}PK}$ 100 mV.



CMOS IC 4007 (INTERNAL STRUCTURE)

$$\therefore V_{i_{mid}} = V_{sig}\left(\frac{R_G}{R_G + R_{sig}}\right)$$

Usually R_G is selected very large (e.g. in the MΩ range) with the result that in many applications $R_G \gg R_{sig}$ and

$$V_i \cong V_{sig}$$

Now, $V_{gs} = V_i$

and $V_o = -g_m V_{gs}(r_o \parallel R_D \parallel R_L)$

Thus the voltage gain A_v is

$$A_v = -g_m(r_o \parallel R_D \parallel R_L)$$

and the open-circuit voltage gain is

$$A_{v_o} = -g_m(r_o \parallel R_D)$$

The overall voltage gain from the signal-source to the load will be

$$G_v = \frac{-R_G}{R_G + R_{sig}} g_m(r_o \parallel R_D \parallel R_L)$$

The output resistance is $r_o \parallel R_D$.

· DESIGN OF CIRCUIT & CALCULATION :-

The resistance and capacitance values were taken as given in the circuit diagram

The d.c bias values were measured as follows

$V_D = 2.4$ volt