EXPERIMENTS OF DIGITAL-LAB :-

Verification of GATES

a. To study and verify the truth table of logic gates

2. Half Adder, Full Adder, Subtractor
    a. To realize Half Adder, Full Adder, Half and Full Subtractor
        i. Using X-OR and Basic gates
        ii. Using only NAND gates
3. Excess-3 to BCD & Vice Versa
    a. Using NAND gates
4. Comparators
    a. To verify the truth table of one bit, two and four bit comparators using logic gates
5. MUX/DEMUX
    a. To study and verify the MUX and demux
    b. To verify Half Adder, Full Adder, Half and Full Subtractor using MUX
6. Flip-flops
    a. Truth table verification using i) RS FP, II) T FF, III) D FP, 1V) JK FP
7. Counters
    a. Realization of 3-bit counter and MOD-N Counter
8. Shift Registers
    a. SIPO
    b. SISO
    c. PIPO
    d. PISO
9. VHDL Programming
    a. Half Adder
    b. Full Adder