GLR - 6

FLIP-FLOP

Aim:- Truth table verification of Flip-Flops:

RS FLIP-FLOP

(i) JK Master Slave
(ii) D- Type
(iii) T- Type.

Apparatus Required: -

IC 7410, IC 7400, etc.

Procedure: -

1. Connections are made as per circuit diagram.
2. The truth table is verified for various combinations of inputs.

Truth Table:- (Master Slave JK Flip-Flop)

Preset	Clear	J	K	Clock	Qn+1	$\overline{Qn+1}$	
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	0	0	⎍	Qn	$\overline{Qn}$	No Change
1	1	0	1	⎍	0	1	Reset
1	1	1	0	⎍	1	0	Set
1	1	1	1	⎍	$\overline{Qn}$	Qn	Toggle

D Flip-Flop:-

Preset	Clear	D	Clock	Qn+1	$\overline{Qn+1}$
1	1	0	⎍	0	1
1	1	1	⎍	1	0

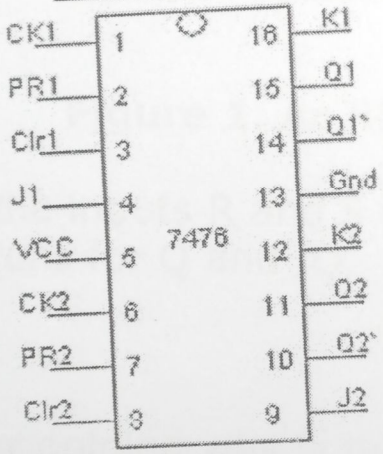
T Flip-Flop:-

Preset	Clear	T	Clock	Qn+1	$\overline{Qn+1}$
1	1	0	⎍	Qn	$\overline{Qn}$
1	1	1	⎍	$\overline{Qn}$	Qn

Exercise:-

- Write the timing diagrams for all the above Flip-Flops

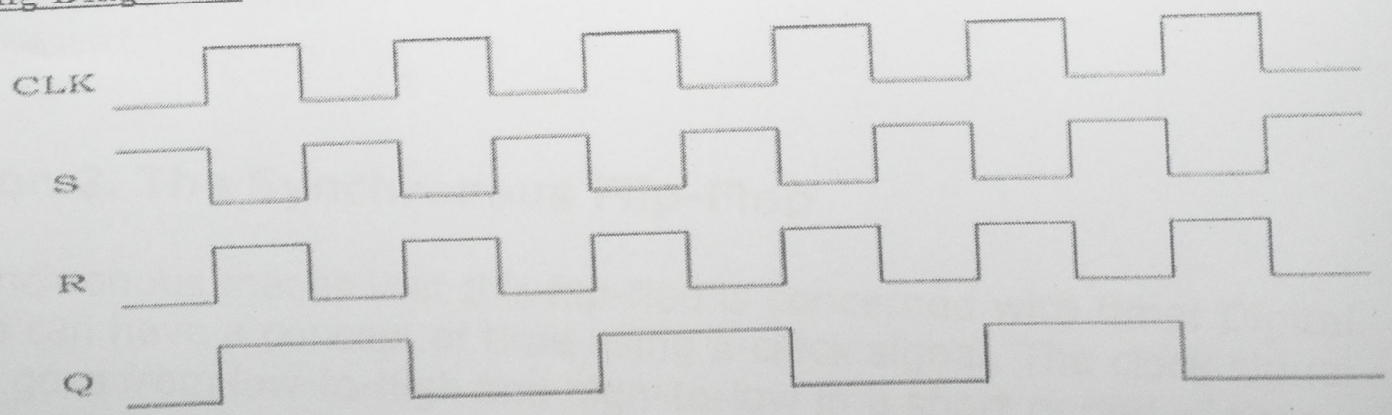
Pin Details:-



Truth Table:-

Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Timing Diagram:-



Preset	Clear	J	K	Clock	Qn+1	$\overline{Qn+1}$	
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	0	0	⎍	Qn	$\overline{Qn}$	No Change
1	1	0	1	⎍	0	1	Reset
1	1	1	0	⎍	1	0	Set
1	1	1	1	⎍	$\overline{Qn}$	Qn	Toggle

(a) Connect the two NOR gates as shown in Figure 1.

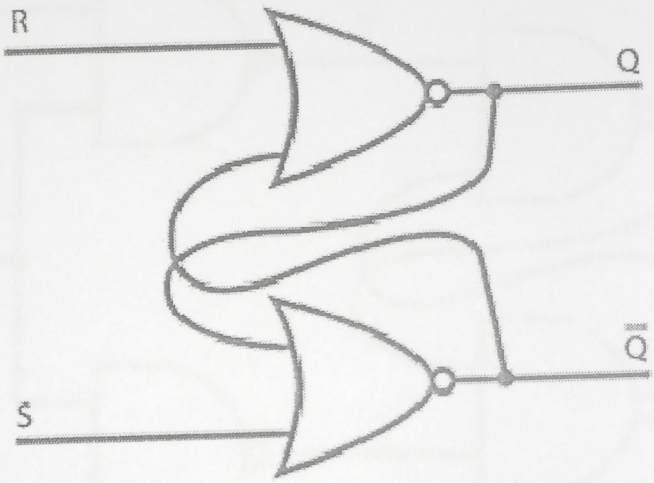


Figure 1. An RS Flip-Flop created using NOR gates.

(b) Vary the inputs R and S (i.e. 0 and +5V) to obtain all the possible combinations for Q and /Q.

(c) In your opinion why is there a Q and /Q output? In your opinion how does this circuit work?

Section 2. The Synchronous Flip-Flop

(a) Synchronous means that this flip-flop is concerned with time! Digital circuits can have a concept of time using a clock signal. The clock signal simply goes from low-to-high and high-to-low in a short period of time.

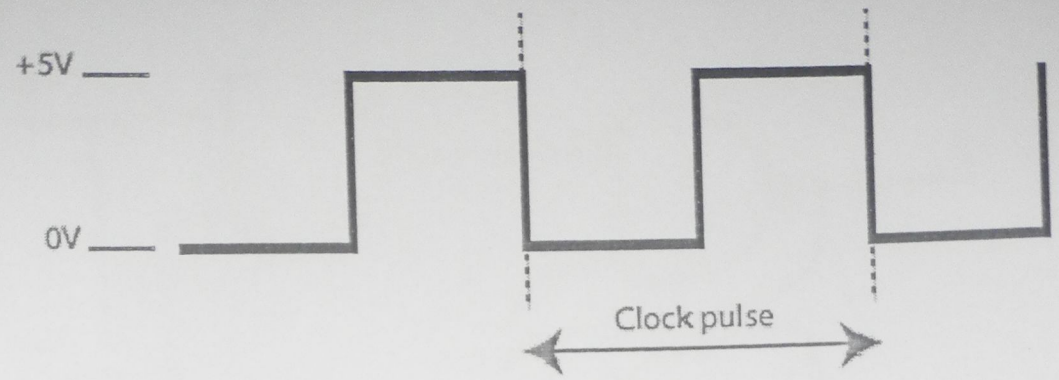


Figure 2. A typical clock signal.

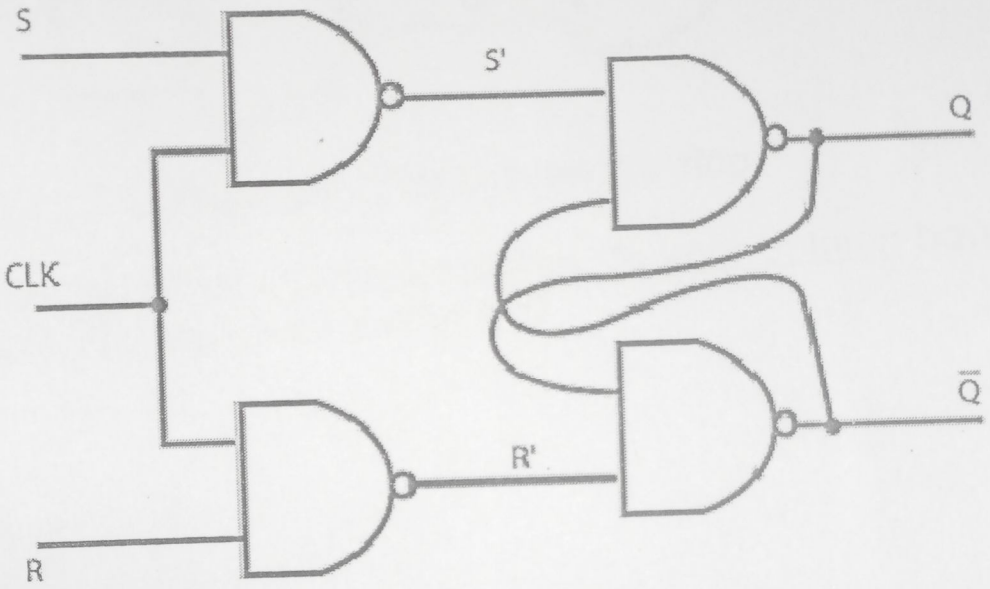


Figure 3. The Synchronous Flip Flop.

Implement the circuit in Figure 3. You can simulate a clock signal by moving the clock line from low to high and back again to low.

(b) Vary inputs R and S and apply the clock pulse. Write the output states into a table as below:

Qn	/Qn	R	S	Qn+1	/Qn+1
0	1	0	0		
1	0	0	0		
0	1	0	1		
1	0	0	1		
0	1	1	0		
1	0	1	0		
0	1	1	1		
1	0	1	1		

(c) Convert the circuit into a D-type flip flop (as shown in Figure 4.)

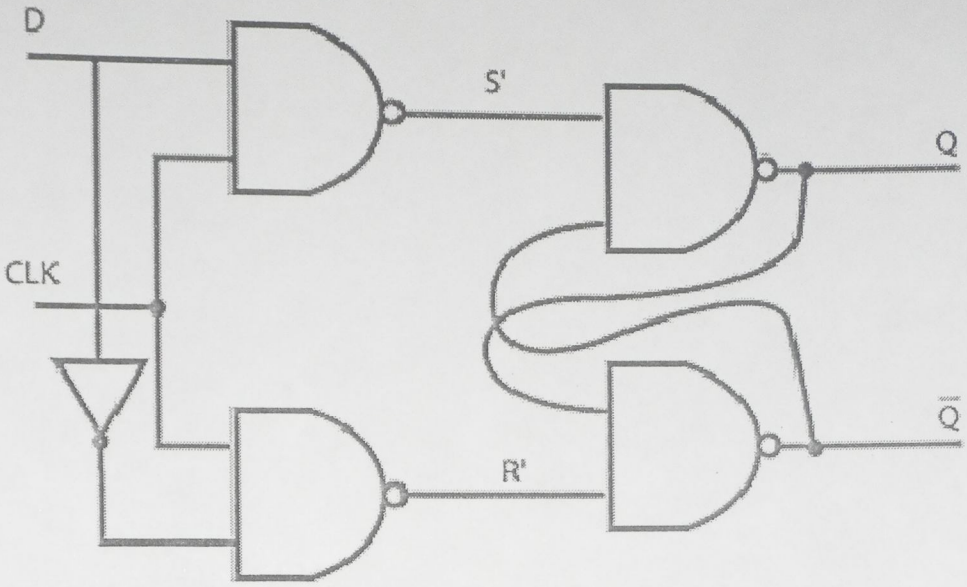


Figure 4. The D-type flip-flop

Draw up the truth table for a D-type flip flop. In your opinion how does it work? what could this circuit be useful for?