National Institute of Technology, Rourkela
Department of Electronics and Communication Engineering
Autumn Examination (Supp), March 2011

B.Tech, 5th Semester
Dept. Of Electronics & Communication Eng. (EC/ EI)
Sub: Microprocessor-I (Subject Code : EC-301)
Full Marks: 58 (Maximum Marks-50)
Duration of Examination: 3hrs

Instruction:-

1. *Answer as many questions you can.*
2. *Answer all questions. Marks scored above 50 will be rounded to 50.*
3. *Figures in right hand side indicate mark.*
4. *Datasheet as needed has been supplied at the end of the question paper.*

1.	What is wait state in 8088 microprocessor? Why is it necessary? Differentiate wait state operation for memory interfacing and IO interfacing.	***(3)***
2.	An interfacing peripheral device is connected to 8086 processor. The device uses 2 address bits for its internal configuration and the remaining 14bits for chip select signal. Design the chip select circuit for the device if the address to be used is 3400H to 340BH.	***(3)***
3.	Write a 8086 program to clear all general purpose registers and flag.	***(3)***
4.	What are functions of segment registers in 8086/ 8088 processors? List the registers and their specific purpose.	***(3)***
5.	It is proposed to connect 8KB of memory to 8086 system (2nos of 4KB chips). Show the process of connecting the memory if A_0 line is not used.	***(3)***
6.	List different signal lines that need to be connected between 8088 processor and 8255PPI. List the characteristic of each line. Draw the chip select logic for 8255 so that the chip is selected for address 1144H. Odd addresses are not used.	***(3)***
7.	Counter-2 in Figure 1 is programmed to work in mode 4 (software triggered strobe). What value should be loaded into the counter to produce strobe signal after 15µsec.What is function of $\overline{WR}$ signal in this scenario.	***(3)***

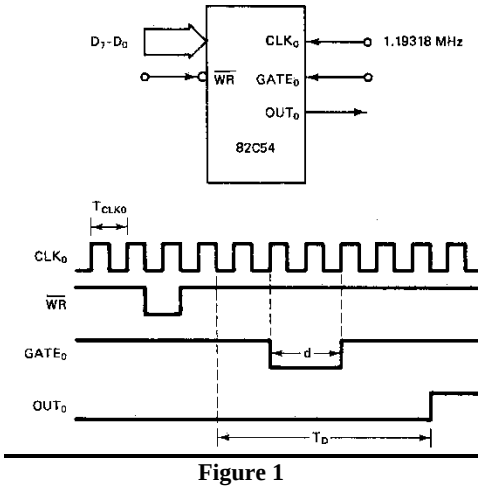
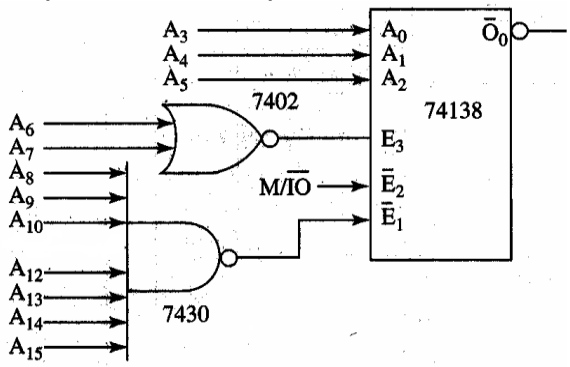


Figure 1

8.	Compare the memory read cycle in 8086 and 8088 processors (byte and word).	***(3)***
9.	With suitable figure discuss how maximum mode control signals are generated in 8088 system.	***(3)***
10.	Write the sequence of instruction that will initialize 8254 timer connected to 8086. Following is the configuration details: a. Counter-0: BCD operation in mode-3 with initial value 0550H b. Counter-1: Binary counter in mode-1 with initial value 4322H c. Counter-2: Binary counter in mode-0 with initial count 1FFFH.	***(3)***
11.	Analyze the activities of SS and SP registers during execution of PUSH and POP instructions.	***(3)***
12.	Write control word for PPI 8255 to configure port A as input and port B as output. Make other necessary assumptions. The output of the circuit O_0 is active low and connected to chip select of 8255. Determine all the input addresses which will prove active chip select to the 8255. (Refer to Figure 2)  **Figure 2**	***(3)***
13.	The ISR for a specific interrupt with type number $(45)_{10}$ starts at physical memory address 33320H. Show the interrupt vector table corresponding to this interrupt. Provide 3 sets of CS:IP values with which the ISR can be accessed (The three code segments should be non-overlapping) .	***(3)***
14.	List the functions of CSA0-CAS2 lines in 82C59A interrupt controller.	***(3)***
15.	With help of suitable diagram discuss the microprocessor bus cycle following an interrupt service request.	***(3)***
16.	Determine ICW1, ICW2, ICW3 and ICW4 for 82C59A in a microprocessor system for following conditions: a. IR0-IR5 are connected directly from interrupting devices. b. IR6 and IR7 are not connected to any interrupt. c. All interrupts are edge sensitive d. Automatic end of Interrupt with buffered mode is selected. Assume other parameters suitably.	***(3)***
17.	A 8086/8088 based system is to be designed to record the number of persons in a mall. Switch-A is pressed by each person while entering and switch-B while leaving. Each of the switches pressed invokes two different interrupts at vector address 51H and 52H (IR0 and IR4 of 8259 respectively). Other interrupts are disabled. The system displays numbers of persons in the mall in decimal number using 4 digits. The 7segment displays are connected to port A and B of 8255. Design the system and write the ISR and the main program to execute the work mentioned above. Show the memory partition.	***(10)***

Reference datasheet information:

8259 Interrupt Controller – ICW Format:

ICW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	A_7	A_6	A_5	1	LTIM	ADI	SNGL	IC4

1 = ICW4 needed
0 = No ICW4 needed

1 = Single
0 = Cascade Mode

CALL address interval
1 = Interval of 4
0 = Interval of 8

1 = Level triggered mode
0 = Edge triggered mode

A_7 - A_5 of Interrupt vector address (MCS-80/85 mode only)

ICW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	A_{15} / T_7	A_{14} / T_6	A_{13} / T_5	A_{12} / T_4	A_{11} / T_3	A_{10}	A_9	A_8

A_{15} - A_8 of interrupt vector address (MCS80/85 mode)

T_7 - T_3 of interrupt vector address (8086/8088 mode)

ICW3 (MASTER DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

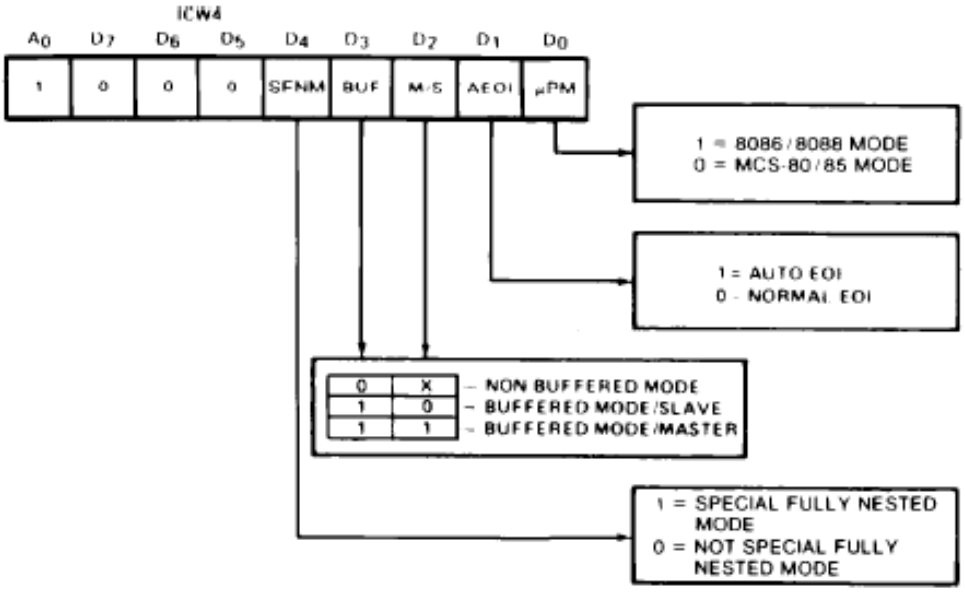
1 = IR INPUT HAS A SLAVE
0 = IR INPUT DOES NOT HAVE A SLAVE

ICW3 (SLAVE DEVICE)

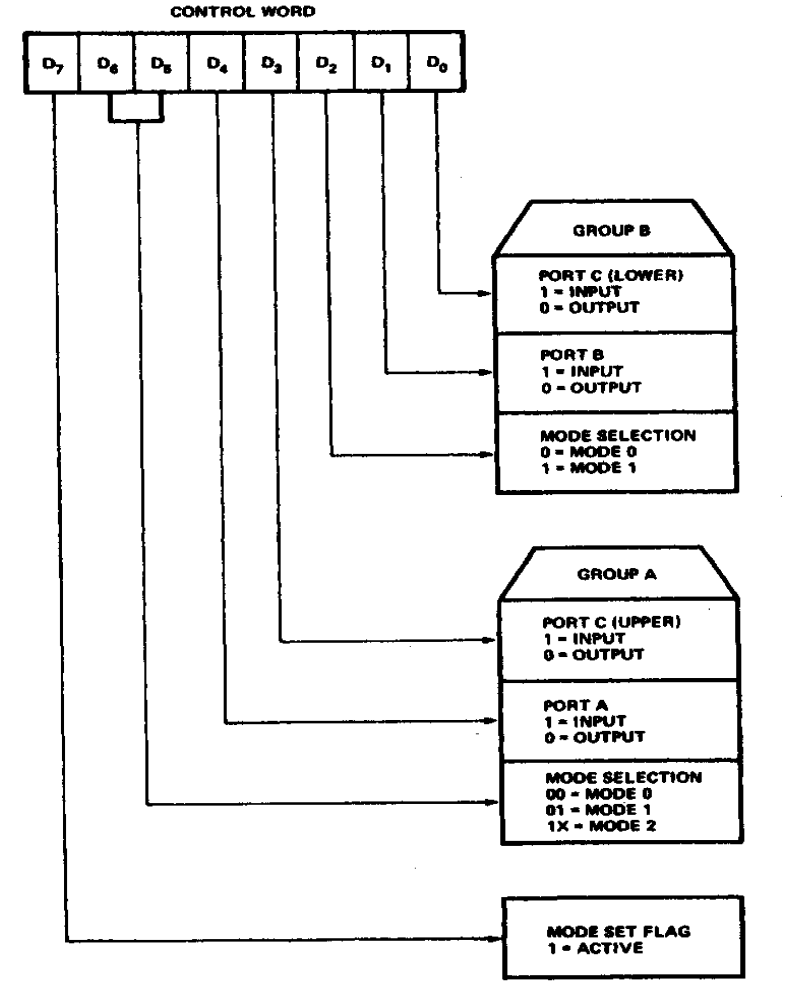
A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

SLAVE ID(1)

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1


ICW4
A0 D7 D6 D5 D4 D3 D2 D1 D0
1 0 0 0 SFNM BUF M/S AEOI μPM
1 = 8086/8088 MODE
0 = MCS-80/85 MODE
1 = AUTO EOI
0 = NORMAL EOI
0 X – NON BUFFERED MODE
1 0 – BUFFERED MODE/SLAVE
1 1 – BUFFERED MODE/MASTER
1 = SPECIAL FULLY NESTED MODE
0 = NOT SPECIAL FULLY NESTED MODE

8255 PPI


CONTROL WORD
D7 D6 D5 D4 D3 D2 D1 D0
GROUP B
PORT C (LOWER)
1 = INPUT
0 = OUTPUT
PORT B
1 = INPUT
0 = OUTPUT
MODE SELECTION
0 = MODE 0
1 = MODE 1
GROUP A
PORT C (UPPER)
1 = INPUT
0 = OUTPUT
PORT A
1 = INPUT
0 = OUTPUT
MODE SELECTION
00 = MODE 0
01 = MODE 1
1X = MODE 2
MODE SET FLAG
1 = ACTIVE

8254 Timer Control Word Format:

CONTROL WORD FORMAT

A1, A0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - SELECT COUNTER

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW - READ/WRITE

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M - MODE

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - BINARY CODED DECIMAL

0	Binary Counter 16-bit
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.