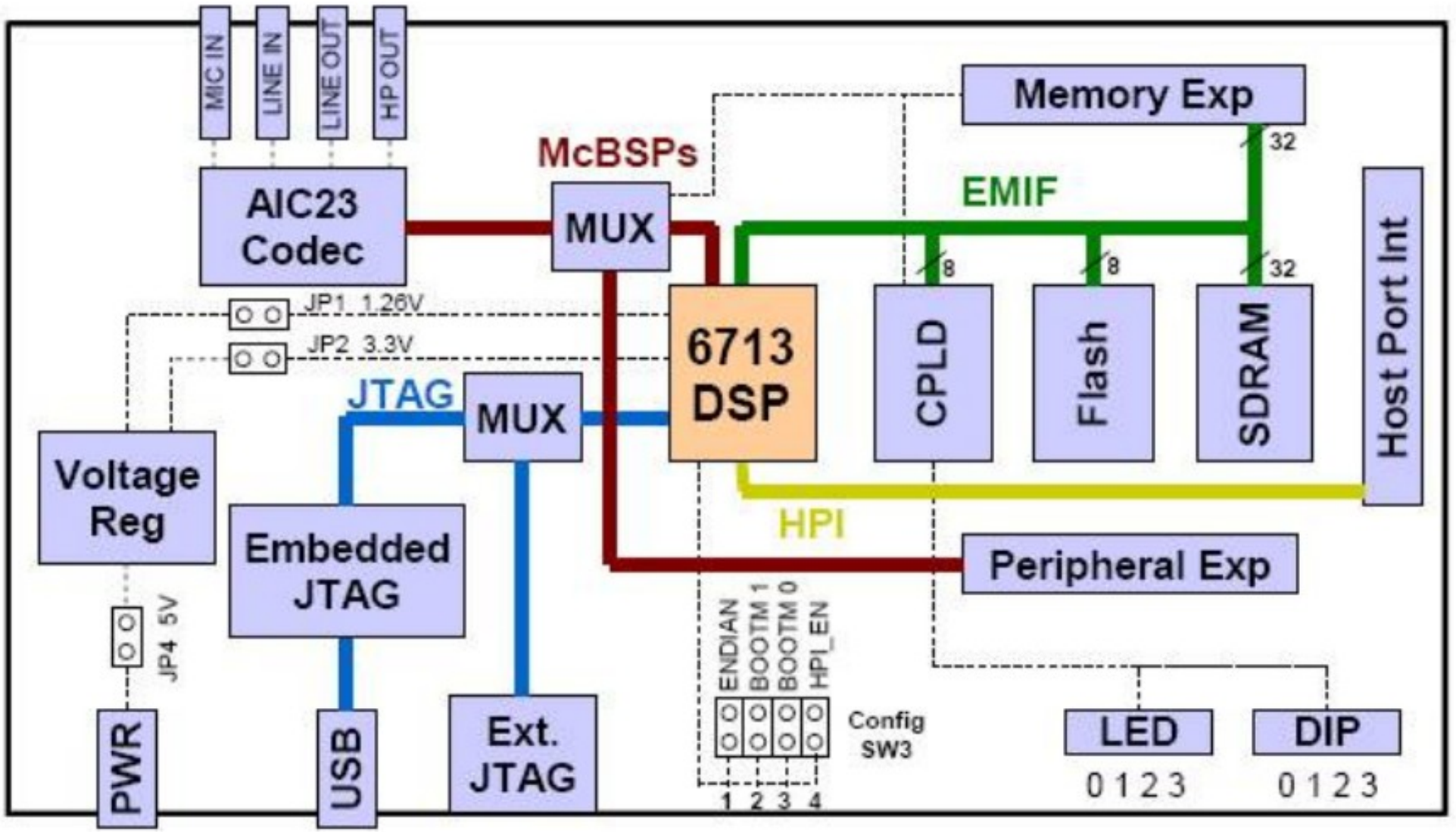
C6713 DSP and Kit

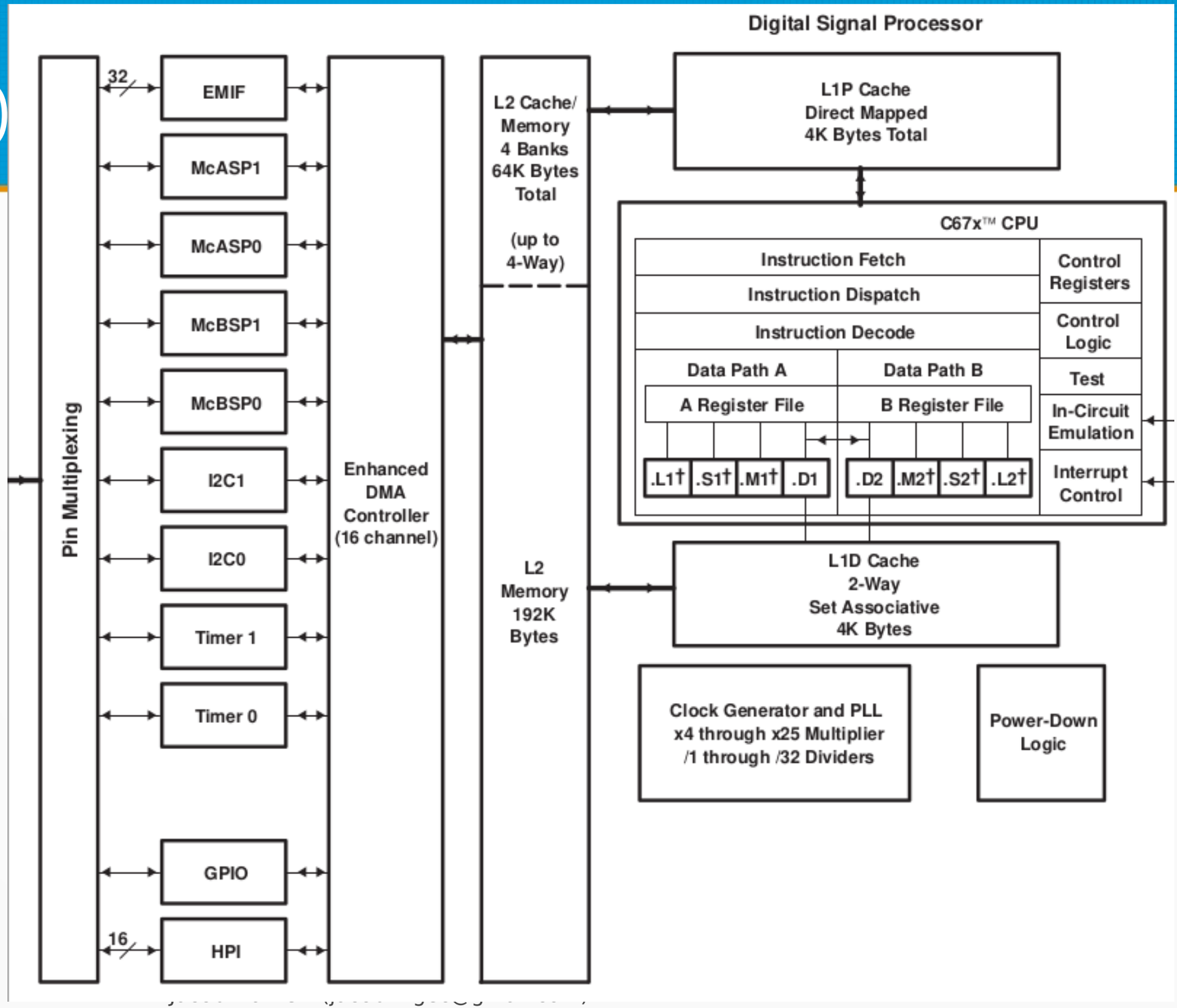
Overview

Kit Overview



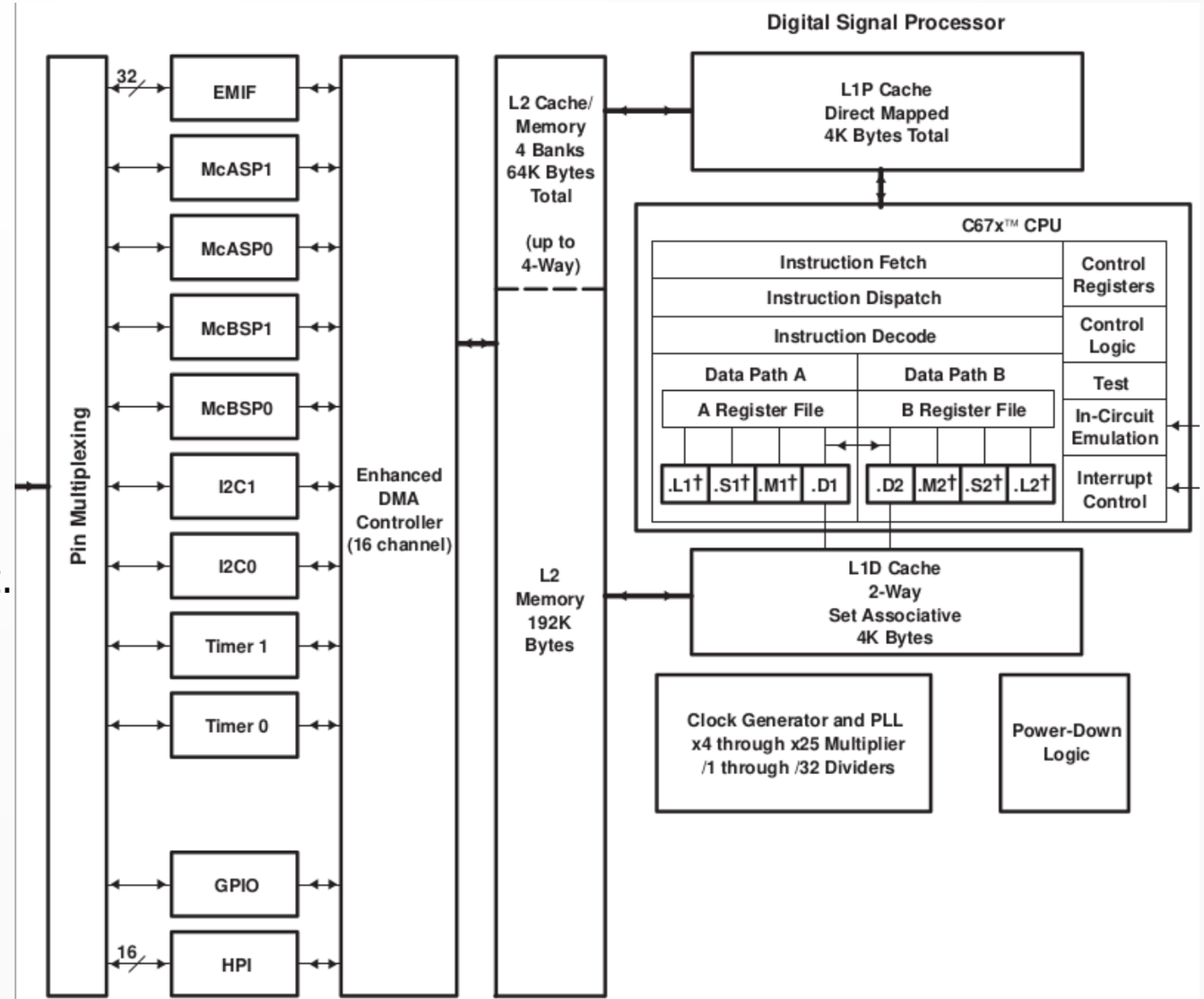
Block D

- VLIW with 8 instruction fetch
  - 256 bit wide fetch packet
  - Each instruction 32 bit long
  - Upto 8 instructions can be executed in parallel in the 8 functional units.
- L – Logical/Arithmetic
- S – Shift
- M – Multiply
- D - Data



Block Diagram

- Each fetch Packet is 256 bits wide..
  - Contains 8 instructions.
    - Can be executed in parallel as 1 execute packet
    - Or sequentially as multiple execute packet.
    - LSB of instruction is used to chain the instructions of an execute packet.
  - Can contain 1 to 8 execute packets.
  - If multiple execute packets in one fetch packet,
    - Dispatch unit will sequentially dispatch the execute packets.



Functional Units

Table 2–2. Functional Units and Operations Performed

Functional Unit	Fixed-Point Operations	Floating-Point Operations
.L unit (.L1, .L2)	32/40-bit arithmetic and compare operations 32-bit logical operations Leftmost 1 or 0 counting for 32 bits Normalization count for 32 and 40 bits	Arithmetic operations DP → SP, INT → DP, INT → SP conversion operations
.S unit (.S1, .S2)	32-bit arithmetic operations 32/40-bit shifts and 32-bit bit-field operations 32-bit logical operations Branches Constant generation Register transfers to/from control register file (.S2 only)	Compare Reciprocal and reciprocal square-root operations Absolute value operations SP → DP conversion operations SPand DP adds and subtracts SP and DP reverse subtracts (src2 – src1)
.M unit (.M1, .M2)	16 × 16-bit multiply operations 32 × 32-bit multiply operations	Floating-point multiply operations Mixed-precision multiply operations
.D unit (.D1, .D2)	32-bit add, subtract, linear and circular address calculation Loads and stores with 5-bit constant offset Loads and stores with 15-bit constant offset (.D2 only)	Load doubleword with 5-bit constant offset

CPU vs DSP

	CPU	**DSP**
Instructions	CISC/RISC	SIMD/VLIW
ALU	Regular	Regular + Multiply Accumulate
Addressing Modes	Regular	Regular + Circular Addressing Modes
ALU Overflows	Truncation	Truncation/Saturation Arithmetic

References

- https://www.ti.com/lit/ds/symlink/tms320c6713b.pdf
- https://e2e.ti.com/cfs-file/__key/communityserver-discussions-components-files/115/8611.Lab.pdf