RAPOR

mips32.v:

It is where the modules are called respectively. At the end of the module, the operations are printed on the screen and PC transfer is made.

instruction_memory.v:

- Read infos from “instructions.txt”, assign them to instruction_mem (2d reg).

- At posedge clock, assign instruction_mem[PC] (new instruction) to instruction.

instruction_decoder.v:

Fragmentation of instruction. (opcode, rs, rt, rd, func, immediate)

input: [15:0] instruction;

outputs: [3:0] opcode; [2:0] Rs, Rt, Rd, func; [5:0] immediate;

mips_registers.v:

- Generate zero signal for not to write to zero register.

- Read infos from “registers.txt”, assign them to registers (2d reg).

- Datas can always be read from registers. <---> always @(*)

- At posedge clock, if signal_reg_write is 1 and write_reg is not equal to zero reg, assign write_data to registers[write_reg].

- At negedge clock, if signal_reg_write is 1, write registers to “registers.txt”.

data_memory.v:

- Read infos from “data.txt”, assign them to data_mem (2d reg).

- If MemRead signal is 1, assign data_mem[address] to read_data.

- If MemWrite signal is 1, assign write_data to data_mem[address].

- Write data memory to “data.txt”

zero_extender.v:

Convert 6 bit immediate to 32 bit with zero extension.

sign_extender.v:

Convert 6 bit immediate to 32 bit with sign extension.

program_counter.v:

This module is not used. Although it gives the correct result, PC gives an error when assigning new PC to the old PC. So that, I made a manual assignment to old PC.

alu_32.v:

ALU from previous homework. (Just added equal signal for branch instructions)

ALU_control.v:

Generates 3-bit control signal with incoming opcode and function. (boolean expressions come from the table)

control_unit.v:

It generates the necessary signals with given opcode.(boolean expressions come from the table)

opcode	**0000**	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1000**	**1001**
	R-type	addi	andi	ori	nori	beq	bne	slti	lw	sw
RegDst	1	0	0	0	0	X	X	0	0	X
ALUSrc	0	1	1	1	1	0	0	1	1	1
MemtoReg	0	0	0	0	0	X	X	X	1	X
RegWrite	1	1	1	1	1	0	0	1	1	0
MemRead	0	0	0	0	0	0	0	0	1	0
MemWrite	0	0	0	0	0	0	0	0	0	1
Branch	0	0	0	0	0	1	0	0	0	0
BranchNotEqual	0	0	0	0	0	0	1	0	0	0
ALUop	R-type	Add	And	Or	Nor	Sub	Sub	Slt	Add	Add
ALUop0	0	1	0	0	1	1	1	1	1	1
ALUop1	0	0	1	1	0	1	1	1	0	0
ALUop2	0	0	0	1	1	0	0	1	0	0

R-type = op3’ op2’ op1’ op0’

addi = op3’ op2’ op1’ op0

andi = op3’ op2’ op1 op0’

ori = op3’ op2’ op1 op0

nori = op3’ op2 op1’ op0’

beq = op3’ op2 op1’ op0

bne = op3’ op2 op1 op0’

slti = op3’ op2 op1 op0

lw = op3 op2’ op1’ op0’

sw = op3 op2’ op1’ op0

RegDst = R-type

ALUSrc = addi + andi + ori + nori + slti + lw + sw

MemtoReg = lw

RegWrite = R-type + addi + andi + ori + nori + slti + lw

MemRead = lw

MemWrite = sw

Branch = beq

BranchNotEqual = bne

ALUop2	**ALUop1**	**ALUop0**	**F2**	**F1**	**F0**	**Operation**
0	0	0	0	0	0	110
0	0	0	0	0	1	000
0	0	0	0	1	0	010
0	0	0	0	1	1	001
0	0	0	1	0	0	101
0	0	0	1	0	1	111
0	0	1	X	X	X	000
0	1	0	X	X	X	110
0	1	1	X	X	X	010
1	0	1	X	X	X	101
1	1	0	X	X	X	111
1	1	1	X	X	X	100

ALUctr2 = ALUop1ALUop0’ + ALUop2ALUop0 + ALUop1’ALUop0’F2F1’ + ALUop1’ALUop0’F1’F0’

ALUctr1 = ALUop2’ALUop1 + ALUop2ALUop0’ + ALUop1’ALUop0’F2F0

+ ALUop1’ALUop0’ F2’F0’

ALUctr0 = ALUop1’ALUop0’F2F1’ + ALUop1’ALUop0’F2’F1F0 + ALUop2ALUop1 ALUop0’ + ALUop2ALUop1’ALUop0

ZERO EXTENDER

```
VSIM 5> step -current
# time =  0, a = 011110, result = 00000000000000000000000000011110 <--> ZERO EXTENDER TEST
# time = 20, a = 111101, result = 00000000000000000000000000111101 <--> ZERO EXTENDER TEST
```

SIGN EXTENDER

```
VSIM 5> step -current
# time =  0, a = 011110, result = 00000000000000000000000000011110 <--> SIGN EXTENDER TEST
# time = 20, a = 111101, result = 11111111111111111111111111111101 <--> SIGN EXTENDER TEST
```

ALU

```
VSIM 5> step -current
# time= 0, a =00000000000000000000000010001001, b=11111111111111000111000000000001, carry_in=0, result=11111111111111000111000010001010, equal=0
# time=20, a =00000000000000000000000010001001, b=11111111111111000111000000000001, carry_in=0, result=11111111111111000111000010001000, equal=0
# time=40, a =00000000000000000000000000101001, b=00000000000000000000000000000011, carry_in=0, result=00000000000000000000000000100110, equal=0
# time=80, a =00000000000000000000000010001001, b=01111111111111000111000000000001, carry_in=0, result=00000000000000000000000000000001, equal=0
# time=100, a =00000000000000000000000010001001, b=11111111111111000111000000000001, carry_in=0, result=00000000000000001110001110110110, equal=0
# time=120, a =00000000000000000000000010001001, b=11111111111111000111000000000001, carry_in=0, result=00000000000000000000000000000001, equal=0
# time=140, a =00000000000000000000000000000000, b=00000000000000000000000000000000, carry_in=0, result=00000000000000000000000000000000, equal=1
```

INSTRUCTION MEMORY

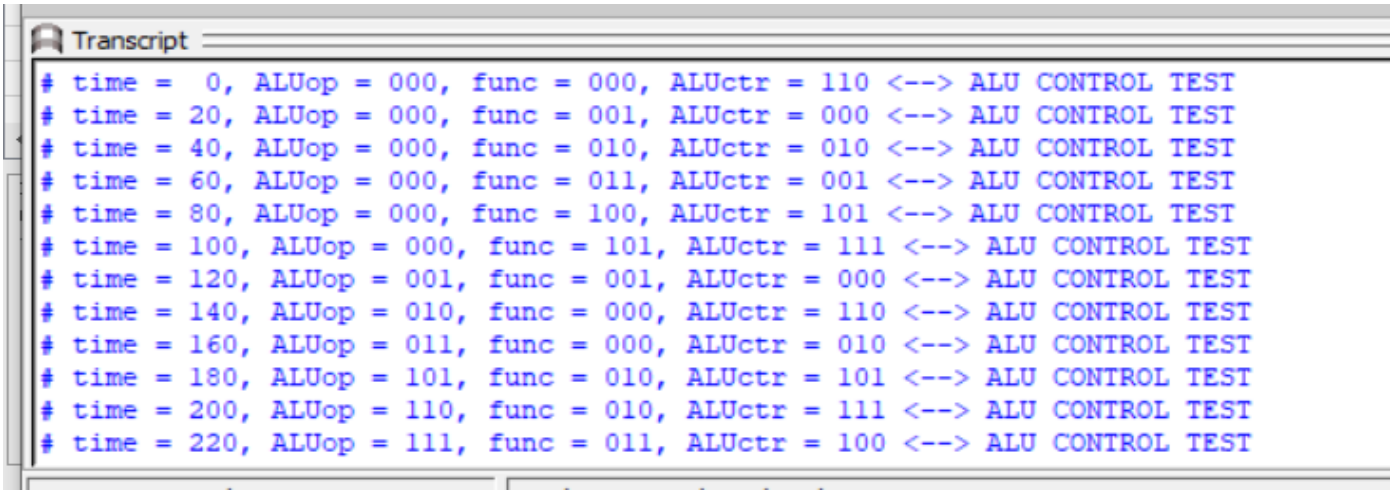
```
VSIM 5> step -current
#  time =  0, PC =     4, instruction = 0001101111010001
#  time = 20, PC =     1, instruction = 1001001011000110
#  time = 40, PC =     2, instruction = 1000001101000110
#  time = 60, PC =     7, instruction = 0001101001011101
#  time = 80, PC =     3, instruction = 0101011101000001
#  time = 100, PC =     5, instruction = 0001101001010001
```

INSTRUCTION DECODER

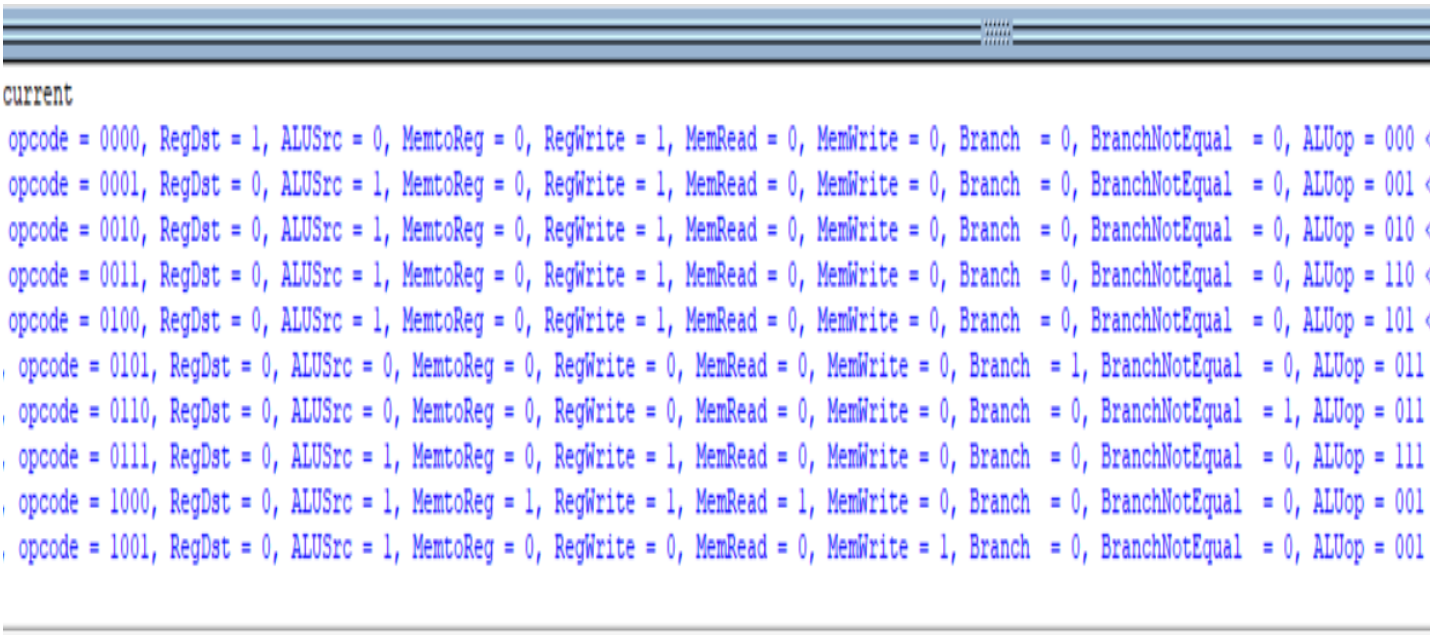
Transcript

```
VSIM 5> step -current
# instruction=0000010000010000, opcode=0000, Rs=010, Rt=000, Rd=010, func=000, immediate=010000
# instruction=0000100110111001, opcode=0000, Rs=100, Rt=110, Rd=111, func=001, immediate=111001
# instruction=0000010100001010, opcode=0000, Rs=010, Rt=100, Rd=001, func=010, immediate=001010
# instruction=0000100010111011, opcode=0000, Rs=100, Rt=010, Rd=111, func=011, immediate=111011
# instruction=0000010110010100, opcode=0000, Rs=010, Rt=110, Rd=010, func=100, immediate=010100
# instruction=0000100110111101, opcode=0000, Rs=100, Rt=110, Rd=111, func=101, immediate=111101
# instruction=0001010100001110, opcode=0001, Rs=010, Rt=100, Rd=001, func=110, immediate=001110
# instruction=0010010101011000, opcode=0010, Rs=010, Rt=101, Rd=011, func=000, immediate=011000
# instruction=0011010101011000, opcode=0011, Rs=010, Rt=101, Rd=011, func=000, immediate=011000
# instruction=0100010001011110, opcode=0100, Rs=010, Rt=001, Rd=011, func=110, immediate=011110
# instruction=0101010000011011, opcode=0101, Rs=010, Rt=000, Rd=011, func=011, immediate=011011
```

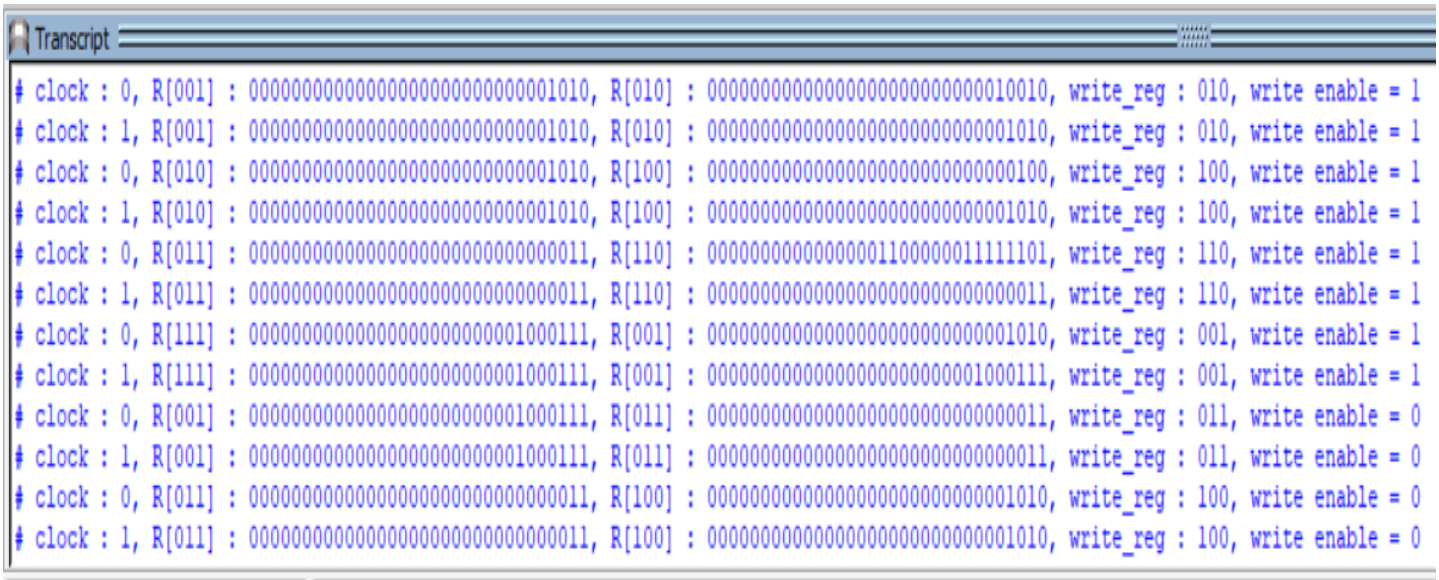
ALU CONTROL



CONTROL UNIT



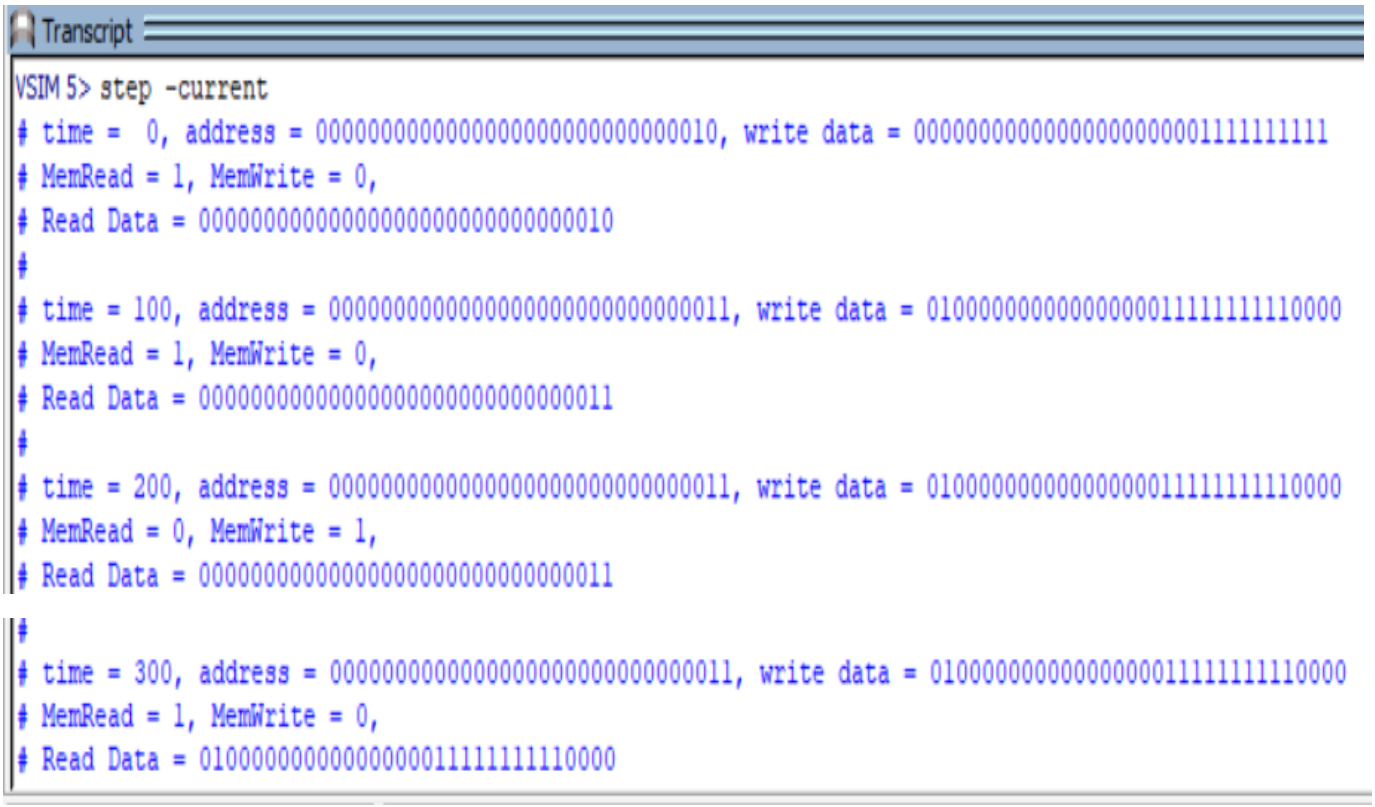
MIPS REGISTER



DATA MEMORY

time = 0 -> LW

time = 300 -> SW (time = 100, 200 -> display old value)



EXAMPLE

Transcript

File Edit View Bookmarks Window Help

Transcript

```
#  Instruction: 0000001010011000
#  Opcode: 0000, Rs: 001, Rt: 010, Rd:011, func: 000, immediate: 011000 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 110, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address: 00000000000000000000000000000010, write_data: 00000000000000000000000000010010
#  Register: read_data_1: 00000000000000000000000000001010, read_data_2: 00000000000000000000000000010010, write_data: 00000000000000000000000000000010
#
#  Instruction: 0000001010011000
#  Opcode: 0000, Rs: 001, Rt: 010, Rd:011, func: 000, immediate: 011000 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 110, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address: 00000000000000000000000000000010, write_data: 00000000000000000000000000010010
#  Register: read_data_1: 00000000000000000000000000001010, read_data_2: 00000000000000000000000000010010, write_data: 00000000000000000000000000000010
#
#  Instruction: 1001001011000110
#  Opcode: 1001, Rs: 001, Rt: 011, Rd:000, func: 110, immediate: 000110 , equal: 0
#  sig_reg_write: 0, sig_mem_write: 1, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 1
#  Memory: read_data: xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address: 00000000000000000000000000010000, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000000001010, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000000010000
#
#  Instruction: 1001001011000110
#  Opcode: 1001, Rs: 001, Rt: 011, Rd:000, func: 110, immediate: 000110 , equal: 0
#  sig_reg_write: 0, sig_mem_write: 1, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 0
#  Memory: read_data: xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx, address: 00000000000000000000000000010000, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000000001010, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000000010000
#
#  Instruction: 1000001101000110
#  Opcode: 1000, Rs: 001, Rt: 101, Rd:000, func: 110, immediate: 000110 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 1, Branch: 0, BranchNotEqual: 0, MemtoReg: 1, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000010000, write_data: 00000000000000000000000100101
#  Register: read_data_1: 00000000000000000000000000001010, read_data_2: 00000000000000000000000100101, write_data: 00000000000000000000000000000010
#
#  Instruction: 1000001101000110
#  Opcode: 1000, Rs: 001, Rt: 101, Rd:000, func: 110, immediate: 000110 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 1, Branch: 0, BranchNotEqual: 0, MemtoReg: 1, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000010000, write_data: 00000000000000000000000100101
#  Register: read_data_1: 00000000000000000000000000001010, read_data_2: 00000000000000000000000100101, write_data: 00000000000000000000000000000010
#
#  Instruction: 0101011101000001
#  Opcode: 0101, Rs: 011, Rt: 101, Rd:000, func: 001, immediate: 000001 , equal: 1
#  sig_reg_write: 0, sig_mem_write: 0, sig_mem_read: 0, Branch: 1, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 010, RegDst: 0, ALUop: 011, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000000000000
#
#  Instruction: 0101011101000001
#  Opcode: 0101, Rs: 011, Rt: 101, Rd:000, func: 001, immediate: 000001 , equal: 1
#  sig_reg_write: 0, sig_mem_write: 0, sig_mem_read: 0, Branch: 1, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 010, RegDst: 0, ALUop: 011, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000000000000
```

```
#  Instruction: 0110011101000001
#  Opcode: 0110, Rs: 011, Rt: 101, Rd:000, func: 001, immediate: 000001 , equal: 1
#  sig_reg_write: 0, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 1, MemtoReg: 0, ALUSrc: 0, ALUctr: 010, RegDst: 0, ALUop: 011, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000000000000
#
#  Instruction: 0110011101000001
#  Opcode: 0110, Rs: 011, Rt: 101, Rd:000, func: 001, immediate: 000001 , equal: 1
#  sig_reg_write: 0, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 1, MemtoReg: 0, ALUSrc: 0, ALUctr: 010, RegDst: 0, ALUop: 011, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000000000000
#
#  Instruction: 0001101110000001
#  Opcode: 0001, Rs: 101, Rt: 110, Rd:000, func: 001, immediate: 000001 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000011, write_data: 00000000000000001100000011111101
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000001100000011111101, write_data: 00000000000000000000000000000011
#
#  Instruction: 0001101110000001
#  Opcode: 0001, Rs: 101, Rt: 110, Rd:000, func: 001, immediate: 000001 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000011, write_data: 00000000000000001100000011111101
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000001100000011111101, write_data: 00000000000000000000000000000011
#
#  Instruction: 0000110010100000
#  Opcode: 0000, Rs: 110, Rt: 010, Rd:100, func: 000, immediate: 100000 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 110, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000010, write_data: 00000000000000000000000000010010
#  Register: read_data_1: 00000000000000000000000000000011, read_data_2: 00000000000000000000000000010010, write_data: 00000000000000000000000000000010
#
#  Instruction: 0000110010100000
#  Opcode: 0000, Rs: 110, Rt: 010, Rd:100, func: 000, immediate: 100000 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 110, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000010, write_data: 00000000000000000000000000010010
#  Register: read_data_1: 00000000000000000000000000000011, read_data_2: 00000000000000000000000000010010, write_data: 00000000000000000000000000000010
#
#  Instruction: 0000100010011001
#  Opcode: 0000, Rs: 100, Rt: 010, Rd:011, func: 001, immediate: 011001 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 000, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000010100, write_data: 00000000000000000000000000010010
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000010010, write_data: 00000000000000000000000000010100
#
#  Instruction: 0000100010011001
#  Opcode: 0000, Rs: 100, Rt: 010, Rd:011, func: 001, immediate: 011001 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 000, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000010100, write_data: 00000000000000000000000000010010
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000010010, write_data: 00000000000000000000000000010100
```

```
#  Instruction: 0000100011001001
#  Opcode: 0000, Rs: 100, Rt: 011, Rd:001, func: 001, immediate: 001001 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 000, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000010110, write_data: 00000000000000000000000000010100
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000010100, write_data: 00000000000000000000000000010110
#
#  Instruction: 0000100011001001
#  Opcode: 0000, Rs: 100, Rt: 011, Rd:001, func: 001, immediate: 001001 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 000, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000010110, write_data: 00000000000000000000000000010100
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000010100, write_data: 00000000000000000000000000010110
#
#  Instruction: 0000101100010010
#  Opcode: 0000, Rs: 101, Rt: 100, Rd:010, func: 010, immediate: 010010 , equal: 1
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 010, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000000000000
#
#  Instruction: 0000101100010010
#  Opcode: 0000, Rs: 101, Rt: 100, Rd:010, func: 010, immediate: 010010 , equal: 1
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 010, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000000000010, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000000000000
#
#  Instruction: 0000111100011010
#  Opcode: 0000, Rs: 111, Rt: 100, Rd:011, func: 010, immediate: 011010 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 010, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001000101, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000001000101
#
#  Instruction: 0000111100011010
#  Opcode: 0000, Rs: 111, Rt: 100, Rd:011, func: 010, immediate: 011010 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 010, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001000101, write_data: 00000000000000000000000000000010
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000000000010, write_data: 00000000000000000000000001000101
#
#  Instruction: 0000111011010011
#  Opcode: 0000, Rs: 111, Rt: 011, Rd:010, func: 011, immediate: 010011 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 001, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000010, write_data: 00000000000000000000000001000101
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000001000101, write_data: 00000000000000000000000000000010
#
#  Instruction: 0000111011010011
#  Opcode: 0000, Rs: 111, Rt: 011, Rd:010, func: 011, immediate: 010011 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 001, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000010, write_data: 00000000000000000000000001000101
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000001000101, write_data: 00000000000000000000000000000010
```

```
#  Instruction: 0000111001110011
#  Opcode: 0000, Rs: 111, Rt: 001, Rd:110, func: 011, immediate: 110011 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 001, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001010001, write_data: 00000000000000000000000000010110
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000000010110, write_data: 00000000000000000000000001010001
#
#  Instruction: 0000111001110011
#  Opcode: 0000, Rs: 111, Rt: 001, Rd:110, func: 011, immediate: 110011 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 001, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001010001, write_data: 00000000000000000000000000010110
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000000010110, write_data: 00000000000000000000000001010001
#
#  Instruction: 0000111011100100
#  Opcode: 0000, Rs: 111, Rt: 011, Rd:100, func: 100, immediate: 100100 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 101, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110111000, write_data: 00000000000000000000000001000101
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000001000101, write_data: 11111111111111111111111110111000
#
#  Instruction: 0000111011100100
#  Opcode: 0000, Rs: 111, Rt: 011, Rd:100, func: 100, immediate: 100100 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 101, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110111000, write_data: 00000000000000000000000001000101
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000001000101, write_data: 11111111111111111111111110111000
#
#  Instruction: 0000111001101100
#  Opcode: 0000, Rs: 111, Rt: 001, Rd:101, func: 100, immediate: 101100 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 101, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110101000, write_data: 00000000000000000000000000010110
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000000010110, write_data: 11111111111111111111111110101000
#
#  Instruction: 0000111001101100
#  Opcode: 0000, Rs: 111, Rt: 001, Rd:101, func: 100, immediate: 101100 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 101, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110101000, write_data: 00000000000000000000000000010110
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 00000000000000000000000000010110, write_data: 11111111111111111111111110101000
#
#  Instruction: 0000001110010101
#  Opcode: 0000, Rs: 001, Rt: 110, Rd:010, func: 101, immediate: 010101 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 111, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001010111, write_data: 00000000000000000000000001010001
#  Register: read_data_1: 00000000000000000000000000010110, read_data_2: 00000000000000000000000001010001, write_data: 00000000000000000000000001010111
#
#  Instruction: 0000001110010101
#  Opcode: 0000, Rs: 001, Rt: 110, Rd:010, func: 101, immediate: 010101 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 111, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001010111, write_data: 00000000000000000000000001010001
#  Register: read_data_1: 00000000000000000000000000010110, read_data_2: 00000000000000000000000001010001, write_data: 00000000000000000000000001010111
```

```
#  Instruction: 0000001011111101
#  Opcode: 0000, Rs: 001, Rt: 011, Rd:111, func: 101, immediate: 111101 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 111, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001010111, write_data: 00000000000000000000000001000101
#  Register: read_data_1: 00000000000000000000000000010110, read_data_2: 00000000000000000000000001000101, write_data: 00000000000000000000000001010111
#
#  Instruction: 0000001011111101
#  Opcode: 0000, Rs: 001, Rt: 011, Rd:111, func: 101, immediate: 111101 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 111, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001010111, write_data: 00000000000000000000000001000101
#  Register: read_data_1: 00000000000000000000000000010110, read_data_2: 00000000000000000000000001000101, write_data: 00000000000000000000000001010111
#
#  Instruction: 0010101001111111
#  Opcode: 0010, Rs: 101, Rt: 001, Rd:111, func: 111, immediate: 111111 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 110, RegDst: 0, ALUop: 010, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001010000, write_data: 00000000000000000000000000010110
#  Register: read_data_1: 11111111111111111111111110101000, read_data_2: 00000000000000000000000000010110, write_data: 00000000000000000000000001010000
#
#  Instruction: 0010101001111111
#  Opcode: 0010, Rs: 101, Rt: 001, Rd:111, func: 111, immediate: 111111 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 110, RegDst: 0, ALUop: 010, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001010000, write_data: 00000000000000000000000000010110
#  Register: read_data_1: 11111111111111111111111110101000, read_data_2: 00000000000000000000000000010110, write_data: 00000000000000000000000001010000
#
#  Instruction: 0010001011110111
#  Opcode: 0010, Rs: 001, Rt: 011, Rd:110, func: 111, immediate: 110111 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 110, RegDst: 0, ALUop: 010, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000100000, write_data: 00000000000000000000000001000101
#  Register: read_data_1: 00000000000000000000000000101000, read_data_2: 00000000000000000000000001000101, write_data: 00000000000000000000000000100000
#
#  Instruction: 0010001011110111
#  Opcode: 0010, Rs: 001, Rt: 011, Rd:110, func: 111, immediate: 110111 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 110, RegDst: 0, ALUop: 010, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000100000, write_data: 00000000000000000000000001000101
#  Register: read_data_1: 00000000000000000000000000101000, read_data_2: 00000000000000000000000001000101, write_data: 00000000000000000000000000100000
#
#  Instruction: 0011101001111000
#  Opcode: 0011, Rs: 101, Rt: 001, Rd:111, func: 000, immediate: 111000 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 111, RegDst: 0, ALUop: 110, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110111000, write_data: 00000000000000000000000001010000
#  Register: read_data_1: 11111111111111111111111110101000, read_data_2: 00000000000000000000000001010000, write_data: 11111111111111111111111110111000
#
#  Instruction: 0011101001111000
#  Opcode: 0011, Rs: 101, Rt: 001, Rd:111, func: 000, immediate: 111000 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 111, RegDst: 0, ALUop: 110, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110111000, write_data: 00000000000000000000000001010000
#  Register: read_data_1: 11111111111111111111111110101000, read_data_2: 00000000000000000000000001010000, write_data: 11111111111111111111111110111000
```

```
#  Instruction: 0011001011101010
#  Opcode: 0011, Rs: 001, Rt: 011, Rd:101, func: 010, immediate: 101010 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 111, RegDst: 0, ALUop: 110, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110111010, write_data: 00000000000000000000000000100000
#  Register: read_data_1: 11111111111111111111111110111000, read_data_2: 00000000000000000000000000100000, write_data: 11111111111111111111111110111010
#
#  Instruction: 0011001011101010
#  Opcode: 0011, Rs: 001, Rt: 011, Rd:101, func: 010, immediate: 101010 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 111, RegDst: 0, ALUop: 110, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110111010, write_data: 00000000000000000000000000100000
#  Register: read_data_1: 11111111111111111111111110111000, read_data_2: 00000000000000000000000000100000, write_data: 11111111111111111111111110111010
#
#  Instruction: 0100101001111000
#  Opcode: 0100, Rs: 101, Rt: 001, Rd:111, func: 000, immediate: 111000 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 101, RegDst: 0, ALUop: 101, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001000111, write_data: 11111111111111111111111110111000
#  Register: read_data_1: 11111111111111111111111110101000, read_data_2: 11111111111111111111111110111000, write_data: 00000000000000000000000001000111
#
#  Instruction: 0100101001111000
#  Opcode: 0100, Rs: 101, Rt: 001, Rd:111, func: 000, immediate: 111000 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 101, RegDst: 0, ALUop: 101, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000001000111, write_data: 11111111111111111111111110111000
#  Register: read_data_1: 11111111111111111111111110101000, read_data_2: 11111111111111111111111110111000, write_data: 00000000000000000000000001000111
#
#  Instruction: 0100001011100010
#  Opcode: 0100, Rs: 001, Rt: 011, Rd:100, func: 010, immediate: 100010 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 101, RegDst: 0, ALUop: 101, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110011000, write_data: 11111111111111111111111110111010
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 11111111111111111111111110111010, write_data: 11111111111111111111111110011000
#
#  Instruction: 0100001011100010
#  Opcode: 0100, Rs: 001, Rt: 011, Rd:100, func: 010, immediate: 100010 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 101, RegDst: 0, ALUop: 101, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 11111111111111111111111110011000, write_data: 11111111111111111111111110111010
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 11111111111111111111111110111010, write_data: 11111111111111111111111110011000
#
#  Instruction: 0111001100111000
#  Opcode: 0111, Rs: 001, Rt: 100, Rd:111, func: 000, immediate: 111000 , equal: 1
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 100, RegDst: 0, ALUop: 111, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 11111111111111111111111110111000
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 11111111111111111111111110111000, write_data: 00000000000000000000000000000000
#
#  Instruction: 0111001100111000
#  Opcode: 0111, Rs: 001, Rt: 100, Rd:111, func: 000, immediate: 111000 , equal: 1
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 100, RegDst: 0, ALUop: 111, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 11111111111111111111111110111000
#  Register: read_data_1: 00000000000000000000000001000111, read_data_2: 11111111111111111111111110111000, write_data: 00000000000000000000000000000000
```

```
#  Instruction: 0111100101100010
#  Opcode: 0111, Rs: 100, Rt: 101, Rd:100, func: 010, immediate: 100010 , equal: 1
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 100, RegDst: 0, ALUop: 111, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 11111111111111111111111110101000
#  Register: read_data_1: 00000000000000000000000000000000, read_data_2: 11111111111111111111111110101000, write_data: 00000000000000000000000000000000
#
#  Instruction: 0111100101100010
#  Opcode: 0111, Rs: 100, Rt: 101, Rd:100, func: 010, immediate: 100010 , equal: 1
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 100, RegDst: 0, ALUop: 111, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000000, write_data: 11111111111111111111111110101000
#  Register: read_data_1: 00000000000000000000000000000000, read_data_2: 11111111111111111111111110101000, write_data: 00000000000000000000000000000000
#
#  Instruction: 1001101111000111
#  Opcode: 1001, Rs: 101, Rt: 111, Rd:000, func: 111, immediate: 000111 , equal: 0
#  sig_reg_write: 0, sig_mem_write: 1, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 1
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000111, write_data: 00000000000000000000000001010111
#  Register: read_data_1: 00000000000000000000000000000000, read_data_2: 00000000000000000000000001010111, write_data: 00000000000000000000000000000111
#
#  Instruction: 1001101111000111
#  Opcode: 1001, Rs: 101, Rt: 111, Rd:000, func: 111, immediate: 000111 , equal: 0
#  sig_reg_write: 0, sig_mem_write: 1, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 0
#  Memory: read_data: 00000000000000000000000000000010, address: 00000000000000000000000000000111, write_data: 00000000000000000000000001010111
#  Register: read_data_1: 00000000000000000000000000000000, read_data_2: 00000000000000000000000001010111, write_data: 00000000000000000000000000000111
#
#  Instruction: 1000101001000111
#  Opcode: 1000, Rs: 101, Rt: 001, Rd:000, func: 111, immediate: 000111 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 1, Branch: 0, BranchNotEqual: 0, MemtoReg: 1, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 1
#  Memory: read_data: 00000000000000000000000001010111, address: 00000000000000000000000000000111, write_data: 00000000000000000000000001000111
#  Register: read_data_1: 00000000000000000000000000000000, read_data_2: 00000000000000000000000001000111, write_data: 00000000000000000000000001010111
#
#  Instruction: 1000101001000111
#  Opcode: 1000, Rs: 101, Rt: 001, Rd:000, func: 111, immediate: 000111 , equal: 0
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 1, Branch: 0, BranchNotEqual: 0, MemtoReg: 1, ALUSrc: 1, ALUctr: 000, RegDst: 0, ALUop: 001, clock: 0
#  Memory: read_data: 00000000000000000000000001010111, address: 00000000000000000000000000000111, write_data: 00000000000000000000000001000111
#  Register: read_data_1: 00000000000000000000000000000000, read_data_2: 00000000000000000000000001000111, write_data: 00000000000000000000000001010111
#
#  Instruction: 0000000000000000
#  Opcode: 0000, Rs: 000, Rt: 000, Rd:000, func: 000, immediate: 000000 , equal: 1
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 110, RegDst: 1, ALUop: 000, clock: 1
#  Memory: read_data: 00000000000000000000000001010111, address: 00000000000000000000000000000000, write_data: 00000000000000000000000000000000
#  Register: read_data_1: 00000000000000000000000000000000, read_data_2: 00000000000000000000000000000000, write_data: 00000000000000000000000000000000
#
#  Instruction: 0000000000000000
#  Opcode: 0000, Rs: 000, Rt: 000, Rd:000, func: 000, immediate: 000000 , equal: 1
#  sig_reg_write: 1, sig_mem_write: 0, sig_mem_read: 0, Branch: 0, BranchNotEqual: 0, MemtoReg: 0, ALUSrc: 0, ALUctr: 110, RegDst: 1, ALUop: 000, clock: 0
#  Memory: read_data: 00000000000000000000000001010111, address: 00000000000000000000000000000000, write_data: 00000000000000000000000000000000
#  Register: read_data_1: 00000000000000000000000000000000, read_data_2: 00000000000000000000000000000000, write_data: 00000000000000000000000000000000
```