RAPOR

and_module.v, or_module.v, xor_module.v, nor_module.v:

I used and, or, xor, nor operators in their files with for loops.

half_adder.v, full_adder.v:

These are used for adder.v. (They are operating 1 bit.)

adder.v:

I made both subtraction and addition in this file.

“sub” is used to select subtraction operation. Subtraction aluop code is 010. After generating sub, I xor’ed sub with second number. Finally, I called 1 bit full adders in for loop.

slt.v:

I subtracted the numbers (called adder.v with appropriate select signal – 010 for sub) and putting the most significant bit into the result.

alu32.v: (Instead of multiplying, I call set less than 2 times in a row.)

I call all modules in order and I transferred return value to another value. After this, I send results (came from modules) with appropriate signals to 8:3 mux.

mult32.v: (NOT COMPLETED)

I call control.v and operate adding and shifting process with “write_enable” and “shift” signals. I use 2:1 mux seperately for these processes. Unfortunately, that's it.

control.v: (NOT COMPLETED)

According to Karnough map, I assigned next state, present state, write, srl and done. States change according to the clock cycle.

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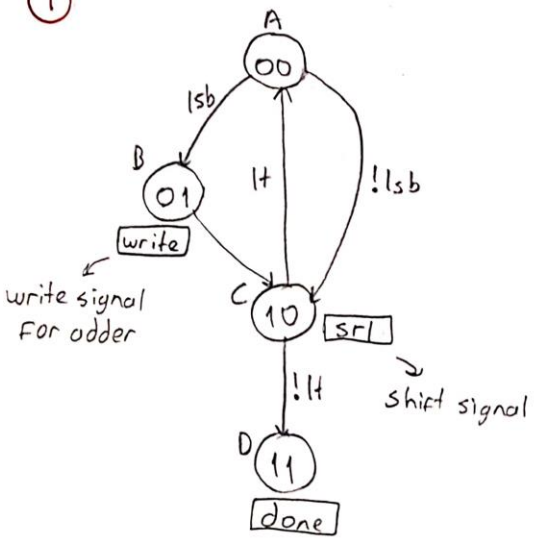
(1)



lsb: least significant bit
lt: less than 32

(2)

	s1	s0	lsb	lt	write	srl	done	n1	n0
A	0	0	0	0	0	0	0	1	0
	0	0	0	1	0	0	0	1	0
	0	0	1	0	0	0	0	0	1
	0	0	1	1	0	0	0	0	1
B	0	1	0	0	1	0	0	1	0
	0	1	0	1	1	0	0	1	0
	0	1	1	0	1	0	0	1	0
	0	1	1	1	1	0	0	1	0
C	1	0	0	0	0	1	0	1	1
	1	0	0	1	0	1	0	0	0
	1	0	1	0	0	1	0	1	1
	1	0	1	1	0	1	0	0	0
D	1	1	0	0	0	0	1	X	X
	1	1	0	1	0	0	1	X	X
	1	1	1	0	0	0	1	X	X
	1	1	1	1	0	0	1	X	X

(3) Karnough map is not required for write, srl and done, because expression can be easily acquired by truth table.

write = s1's0

srl = s1s0'

done = s1s0

n1

s1s0 \ lsblt	00	01	11	10
00	1	1	0	0
01	1	1	1	1
11	0	0	0	0
10	1	0	0	1

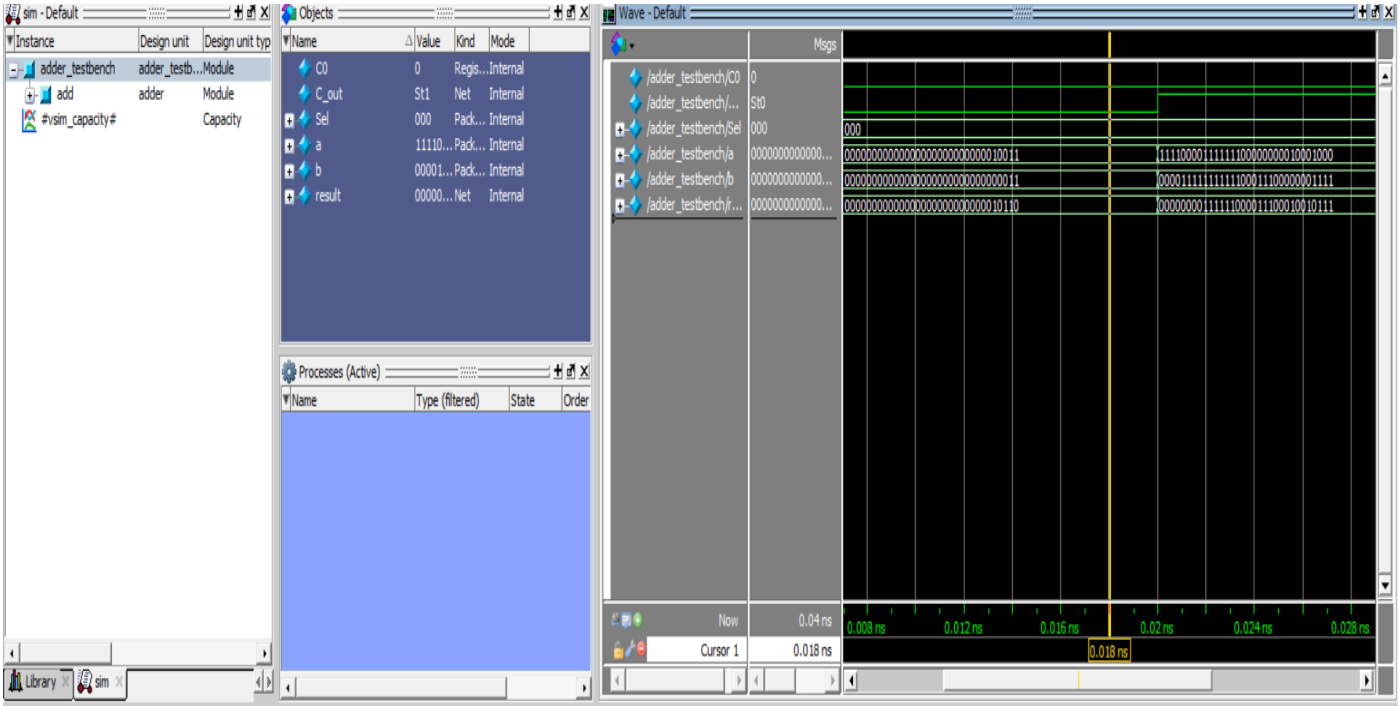
n1 = s1'lsb' + s1's0 + s1s0'lt'

n0

s1s0 \ lsblt	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

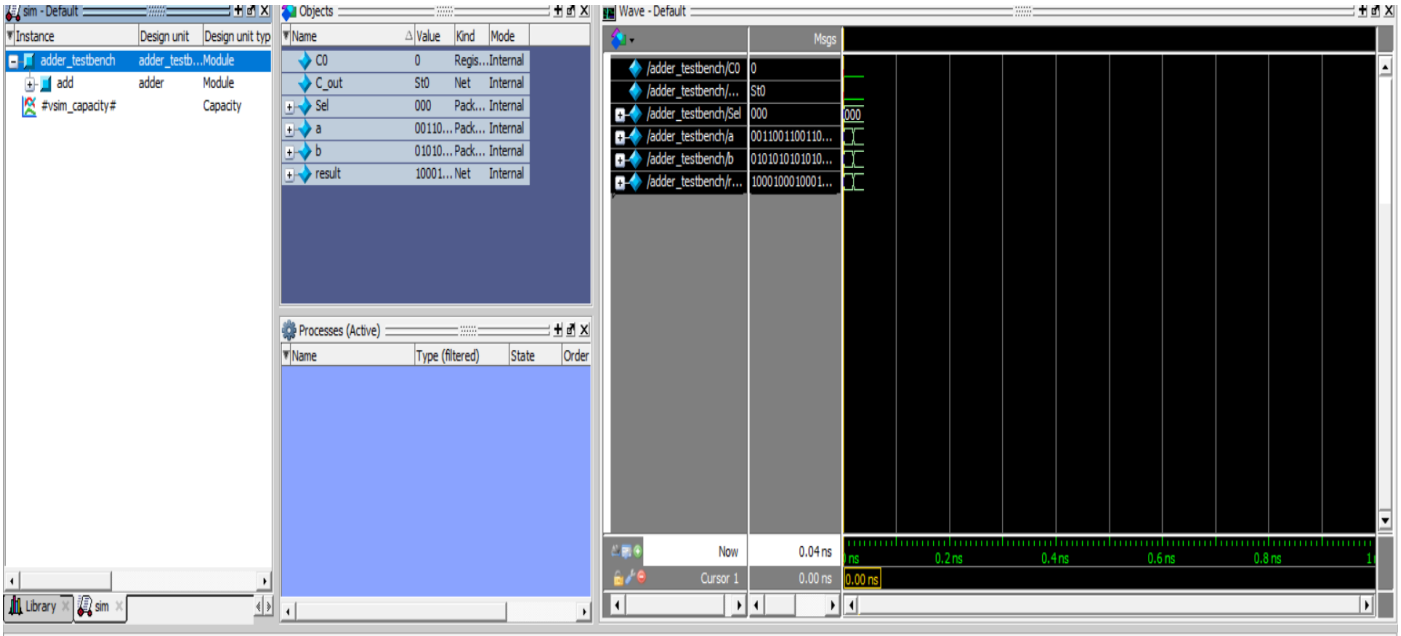
n0 = s1's0'lsb + s1s0'lt'

ADD



Transcript

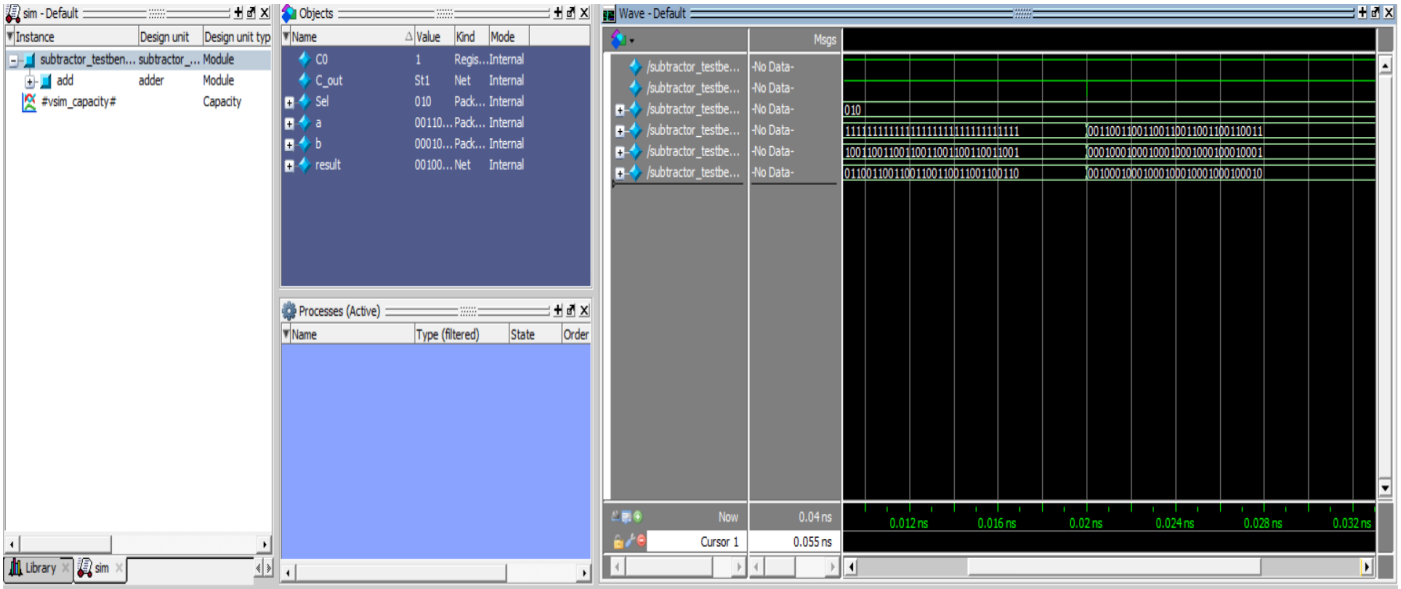
```
sim:/adder_testbench/C_out \
sim:/adder_testbench/Sel \
sim:/adder_testbench/a \
sim:/adder_testbench/b \
sim:/adder_testbench/result
VSIM 5> step -current
# time =  0, a =00000000000000000000000000010011, b=00000000000000000000000000000011, carry_in=0, carry_out=0, result=00000000000000000000000000010110  <--> ADDING TEST
# time = 20, a =11110000111111100000000010001000, b=00001111111111110001110000001111, carry_in=0, carry_out=1, result=00000000111111000011100010010111  <--> ADDING TEST
```

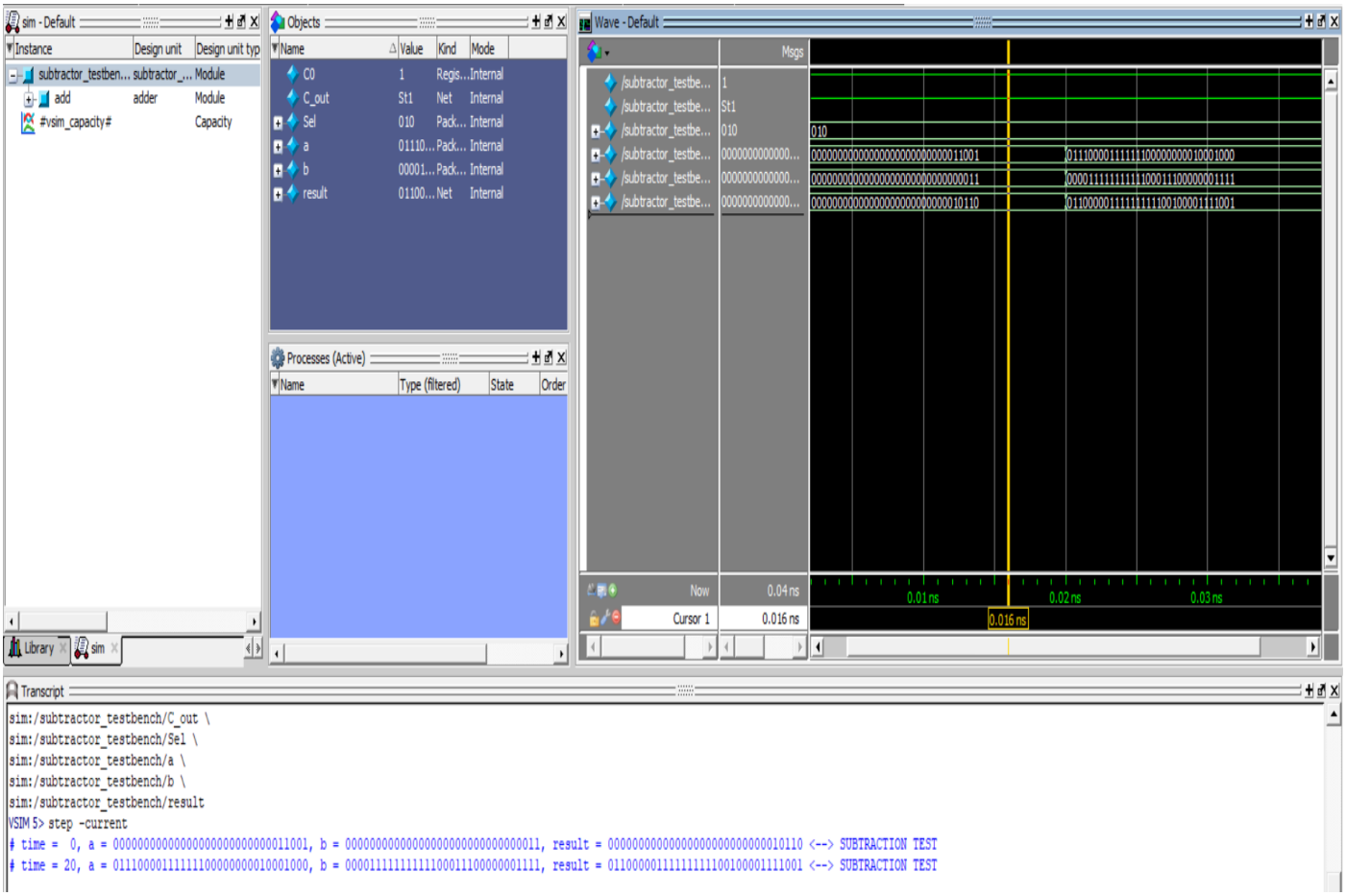


Transcript

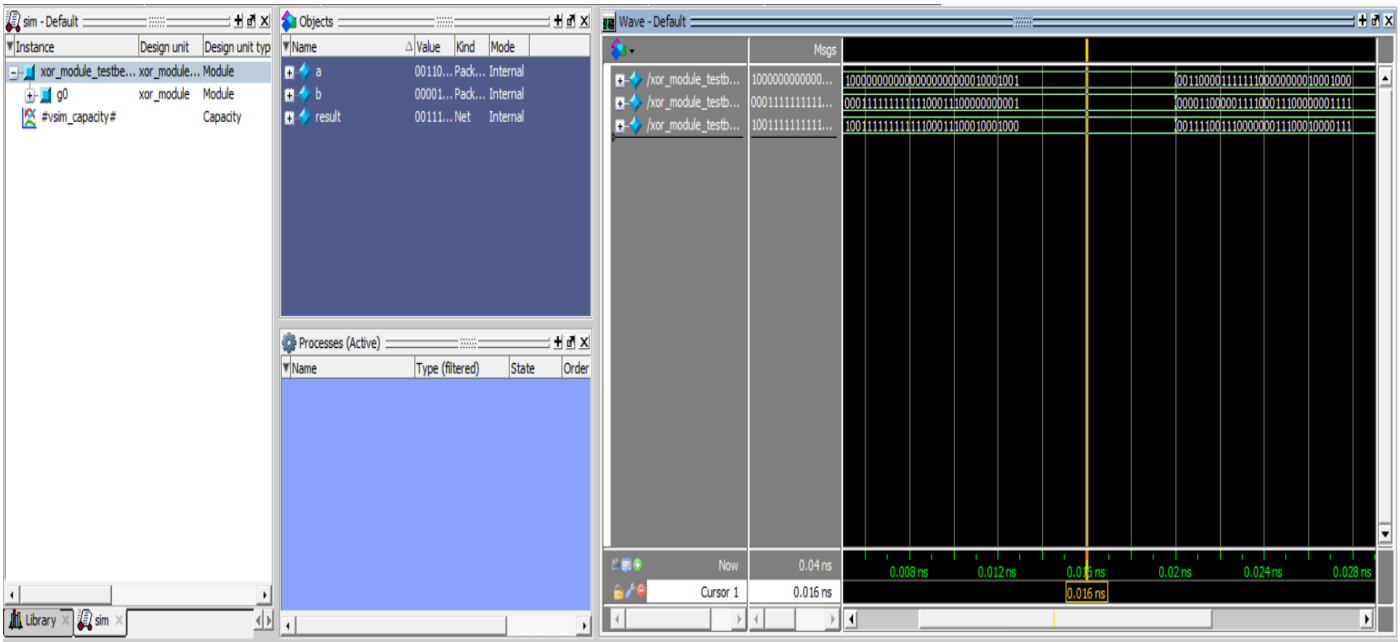
```
sim:/adder_testbench/C_out \
sim:/adder_testbench/Sel \
sim:/adder_testbench/a \
sim:/adder_testbench/b \
sim:/adder_testbench/result
VSIM 5> step -current
# time =  0, a =                   22222222, b=                   11111111, carry_in=0, carry_out=0, result=                   33333333  <--> ADDING TEST
# time = 20, a =                   33333333, b=                   55555555, carry_in=0, carry_out=0, result=                   88888888  <--> ADDING TEST
```

SUB

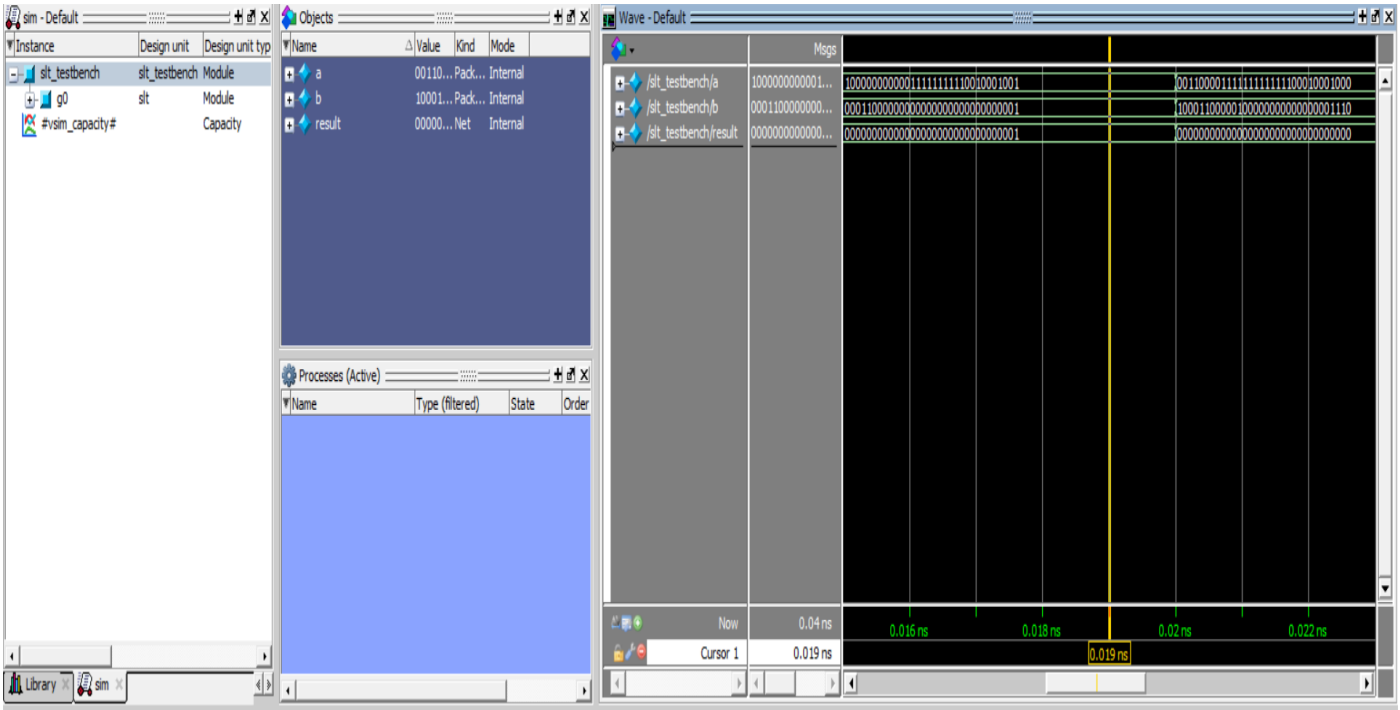

sim - Default
Instance
Design unit
Design unit typ
subtractor_testben...
subtractor_...
Module
add
adder
Module
#vsim_capacity#
Capacity
Objects
Name
Value
Kind
Mode
C0
1
Regis...
Internal
C_out
St1
Net
Internal
Sel
010
Pack...
Internal
a
00110...
Pack...
Internal
b
00010...
Pack...
Internal
result
00100...
Net
Internal
Processes (Active)
Name
Type (filtered)
State
Order
Wave - Default
Msgs
/subtractor_testbe...
-No Data-
010
Now
0.04 ns
Cursor 1
0.055 ns
0.012 ns
0.016 ns
0.02 ns
0.024 ns
0.028 ns
0.032 ns
Library
sim
Transcript
sim:/subtractor_testbench/C_out \
sim:/subtractor_testbench/Sel \
sim:/subtractor_testbench/a \
sim:/subtractor_testbench/b \
sim:/subtractor_testbench/result
VSIM 5> step -current
time = 0, a = ffffffff, b = 99999999, result = 66666666 <--> SUBTRACTION TEST
time = 20, a = 33333333, b = 11111111, result = 22222222 <--> SUBTRACTION TEST
VSIM 6>


sim - Default
Instance
Design unit
Design unit typ
subtractor_testben...
subtractor_...
Module
add
adder
Module
#vsim_capacity#
Capacity
Objects
Name
Value
Kind
Mode
C0
1
Regis...
Internal
C_out
St1
Net
Internal
Sel
010
Pack...
Internal
a
01110...
Pack...
Internal
b
00001...
Pack...
Internal
result
01100...
Net
Internal
Processes (Active)
Name
Type (filtered)
State
Order
Wave - Default
Msgs
/subtractor_testbe...
1
St1
010
Now
0.04 ns
Cursor 1
0.016 ns
0.01 ns
0.02 ns
0.03 ns
0.016 ns
Library
sim
Transcript
sim:/subtractor_testbench/C_out \
sim:/subtractor_testbench/Sel \
sim:/subtractor_testbench/a \
sim:/subtractor_testbench/b \
sim:/subtractor_testbench/result
VSIM 5> step -current
time = 0, a = 00000000000000000000000011001, b = 00000000000000000000000000011, result = 00000000000000000000000010110 <--> SUBTRACTION TEST
time = 20, a = 01110000111111100000000010001000, b = 00001111111111110001110000001111, result = 01100000111111111001000011111001 <--> SUBTRACTION TEST

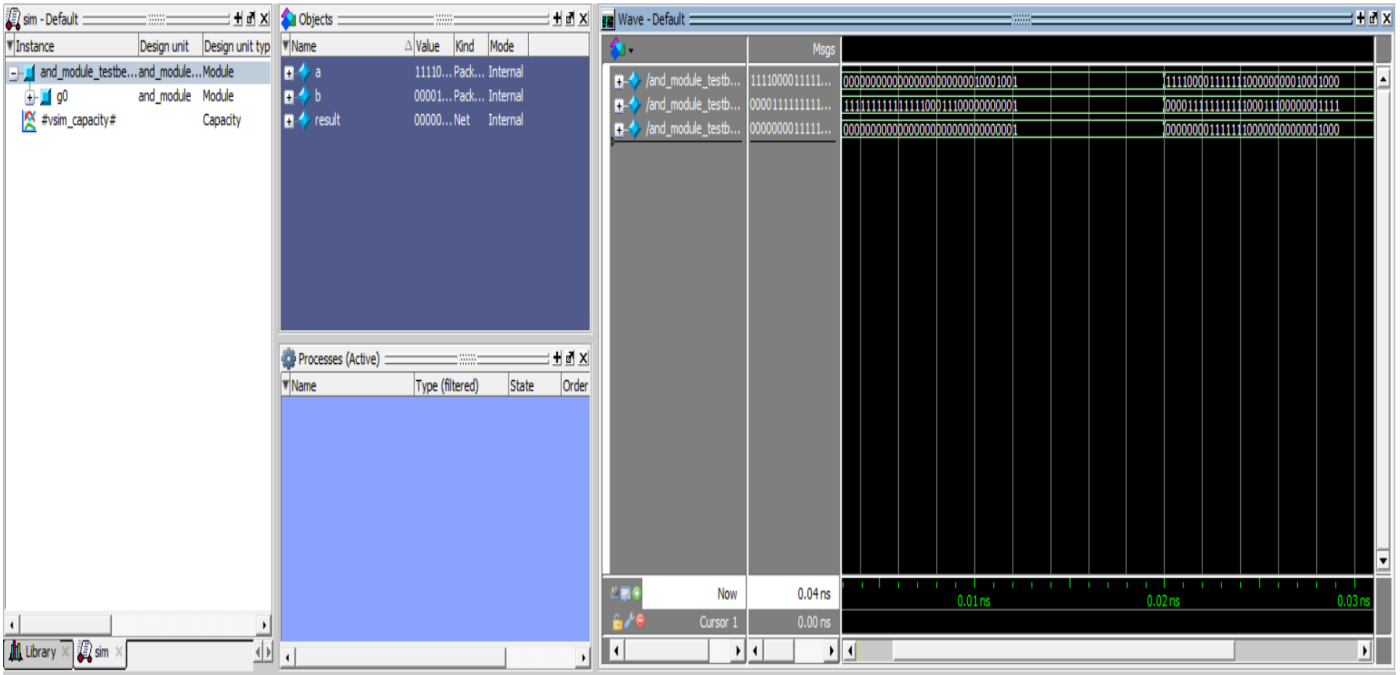
XOR


sim - Default
Instance
Design unit
Design unit typ
xor_module_testbe...
xor_module...
Module
g0
xor_module
Module
#vsim_capacity#
Capacity
Objects
Name
Value
Kind
Mode
a
00110...
Pack...
Internal
b
00001...
Pack...
Internal
result
00111...
Net
Internal
Processes (Active)
Name
Type (filtered)
State
Order
Wave - Default
Msgs
/xor_module_testb...
/xor_module_testb...
/xor_module_testb...
Now
0.04 ns
Cursor 1
0.016 ns
0.008 ns
0.012 ns
0.016 ns
0.02 ns
0.024 ns
0.028 ns
Library
sim
Transcript
Loading work.xor_module
add wave -position insertpoint \
sim:/xor_module_testbench/a \
sim:/xor_module_testbench/b \
sim:/xor_module_testbench/result
VSIM 5> step -current
time = 0, a =10000000000000000000000010001001, b=00011111111111110001110000000001, result=10011111111111110001110010001000 <--> XOR MODULE TEST
time = 20, a =00110000111111100000000010001000, b=00001100000111100011100000001111, result=00111100111000000011100010000111 <--> XOR MODULE TEST

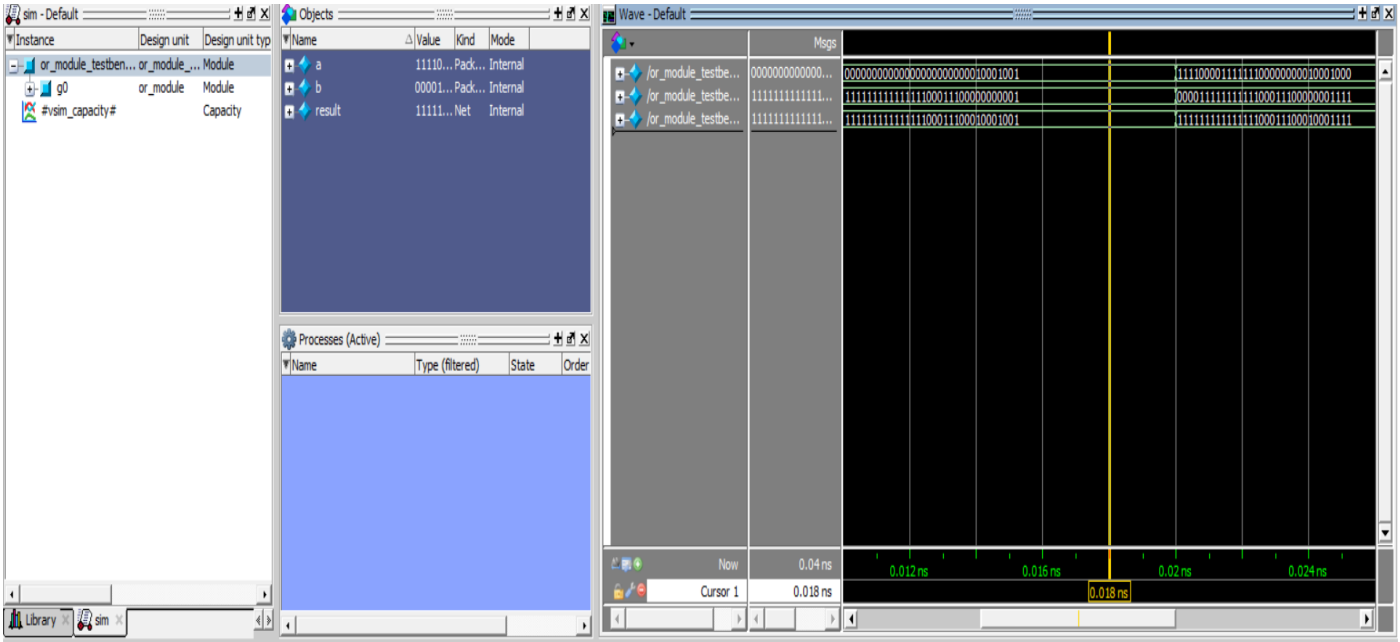
SLT


sim - Default
Instance
Design unit
Design unit typ
slt_testbench
slt_testbench
Module
g0
slt
Module
#vsim_capacity#
Capacity
Objects
Name
Value
Kind
Mode
a
00110...
Pack...
Internal
b
10001...
Pack...
Internal
result
00000...
Net
Internal
Processes (Active)
Name
Type (filtered)
State
Order
Wave - Default
Msgs
/slt_testbench/a
/slt_testbench/b
/slt_testbench/result
Now
0.04 ns
Cursor 1
0.019 ns
0.016 ns
0.018 ns
0.019 ns
0.02 ns
0.022 ns
Library
sim
Transcript
Loading work.half_adder
add wave -position insertpoint \
sim:/slt_testbench/a \
sim:/slt_testbench/b \
sim:/slt_testbench/result
VSIM 5> step -current
time = 0, a =10000000000111111111110010001001, b=00011000000000000000000000000001, result=00000000000000000000000000000001 <--> SET LESS THAN TEST
time = 20, a =00110000111111111111110001001000, b=10001100000100000000000000001110, result=00000000000000000000000000000000 <--> SET LESS THAN TEST

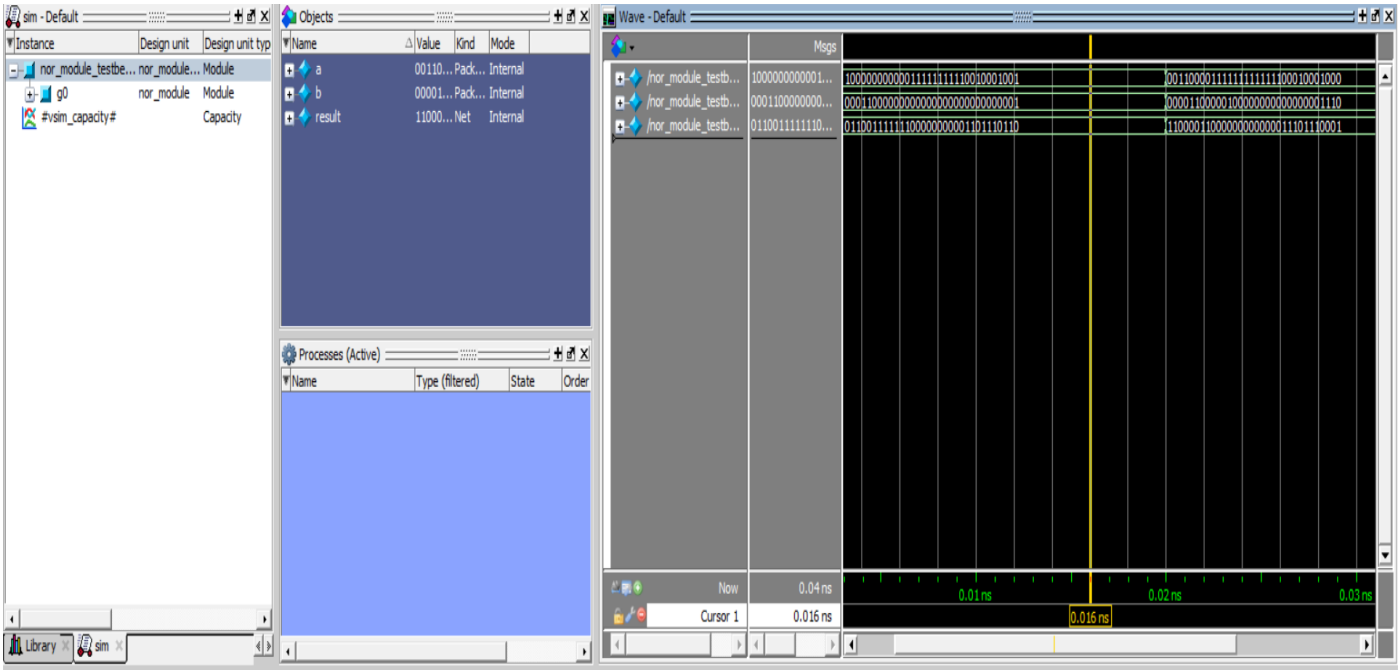
AND


sim - Default
Instance
Design unit
Design unit typ
and_module_testbe...
and_module...
Module
g0
and_module
Module
#vsim_capacity#
Capacity
Objects
Name
Value
Kind
Mode
a
11110...
Pack...
Internal
b
00001...
Pack...
Internal
result
00000...
Net
Internal
Processes (Active)
Name
Type (filtered)
State
Order
Wave - Default
Msgs
/and_module_testb...
1111000011111...
0000111111111...
0000000011111...
Now
0.04 ns
Cursor 1
0.00 ns
0.01 ns
0.02 ns
0.03 ns
Library
sim
Transcript
Loading work.and_module
add wave -position insertpoint \
sim:/and_module_testbench/a \
sim:/and_module_testbench/b \
sim:/and_module_testbench/result
VSIM 5> step -current
time = 0, a =00000000000000000000000010001001, b=11111111111111100011100000000001, result=00000000000000000000000000000001 <--> AND MODULE TEST
time = 20, a =11110000111111110000000010001000, b=00001111111111110001110000001111, result=00000000111111110000000000001000 <--> AND MODULE TEST

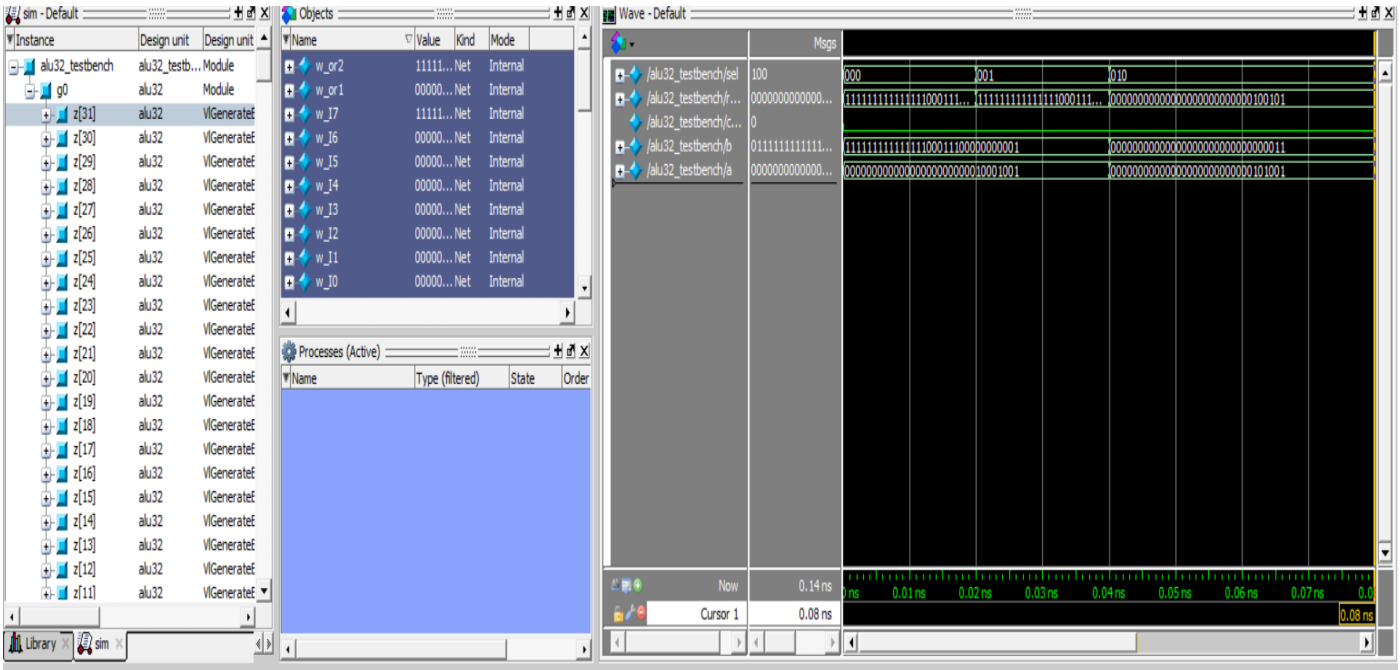
OR


sim - Default
Instance
Design unit
Design unit typ
or_module_testben...
or_module_...
Module
g0
or_module
Module
#vsim_capacity#
Capacity
Objects
Name
Value
Kind
Mode
a
11110...
Pack...
Internal
b
00001...
Pack...
Internal
result
11111...
Net
Internal
Processes (Active)
Name
Type (filtered)
State
Order
Wave - Default
Msgs
/or_module_testbe...
0000000000000...
1111111111111...
Now
0.04 ns
Cursor 1
0.018 ns
0.012 ns
0.016 ns
0.018 ns
0.02 ns
0.024 ns
Library
sim
Transcript
Loading work.or_module
add wave -position insertpoint \
sim:/or_module_testbench/a \
sim:/or_module_testbench/b \
sim:/or_module_testbench/result
VSIM 5> step -current
time = 0, a =00000000000000000000000010001001, b=11111111111111100011100000000001, result=11111111111111100011100010001001 <--> OR MODULE TEST
time = 20, a =11110000111111110000000010001000, b=00001111111111110001110000001111, result=11111111111111100011100010001111 <--> OR MODULE TEST

NOR


sim - Default
Instance
Design unit
Design unit typ
nor_module_testbe...
nor_module...
Module
g0
nor_module
Module
#vsim_capacity#
Capacity
Objects
Name
Value
Kind
Mode
a
00110...
Pack...
Internal
b
00001...
Pack...
Internal
result
11000...
Net
Internal
Processes (Active)
Name
Type (filtered)
State
Order
Wave - Default
Msgs
/nor_module_testb...
/nor_module_testb...
/nor_module_testb...
Now
0.04 ns
Cursor 1
0.016 ns
0.01 ns
0.02 ns
0.03 ns
Library
sim
Transcript
Loading work.nor_module
add wave -position insertpoint \
sim:/nor_module_testbench/a \
sim:/nor_module_testbench/b \
sim:/nor_module_testbench/result
VSIM 5> step -current
time = 0, a =10000000000111111111110010001001, b=00011000000000000000000000000001, result=01100111111100000000001101110110 <--> NOR MODULE TEST
time = 20, a =00110000111111111111111100010001000, b=00001100000100000000000000001110, result=11000011000000000000011101110001 <--> NOR MODULE TEST

ALU


sim - Default
Instance
Design unit
Design unit
alu32_testbench
alu32_testb...
Module
g0
alu32
Module
z[31]
z[30]
z[29]
z[28]
z[27]
z[26]
z[25]
z[24]
z[23]
z[22]
z[21]
z[20]
z[19]
z[18]
z[17]
z[16]
z[15]
z[14]
z[13]
z[12]
z[11]
alu32
VlGenerateE
Objects
Name
Value
Kind
Mode
w_or2
w_or1
w_I7
w_I6
w_I5
w_I4
w_I3
w_I2
w_I1
w_I0
11111...
00000...
Net
Internal
Processes (Active)
Name
Type (filtered)
State
Order
Wave - Default
Msgs
/alu32_testbench/sel
/alu32_testbench/r...
/alu32_testbench/c...
/alu32_testbench/b
/alu32_testbench/a
100
000
001
010
Now
0.14 ns
Cursor 1
0.08 ns
0.01 ns
0.02 ns
0.03 ns
0.04 ns
0.05 ns
0.06 ns
0.07 ns
0.08 ns
Library
sim
Transcript
sim:/alu32_testbench/a
VSIM 5> step -current
time = 0, a =00000000000000000000000010001001, b=11111111111111100011100000000001, carry_in=0, result=11111111111111100011100010001010
time = 20, a =00000000000000000000000010001001, b=11111111111111100011100000000001, carry_in=0, result=11111111111111100011100010001000
time = 40, a =00000000000000000000000000101001, b=00000000000000000000000000000011, carry_in=0, result=00000000000000000000000000100101
time = 80, a =00000000000000000000000010001001, b=01111111111111100011100000000001, carry_in=0, result=00000000000000000000000000000001
time = 100, a =00000000000000000000000010001001, b=11111111111111100011100000000001, carry_in=0, result=00000000000000011100011101110110
time = 120, a =00000000000000000000000010001001, b=11111111111111100011100000000001, carry_in=0, result=00000000000000000000000000000001
time = 140, a =00000000000000000000000010001001, b=11111111111111100011100000000001, carry_in=0, result=11111111111111100011100010001001