Assignment 1 "Best CPU Setup"

Group - SS05

Memory: 2048 locations of 1 bytes each (mem[2048]) = 2KB of memory

1. OS memory: 256 locations of 4 bytes each (mem[0] to mem[511])

2. Instruction memory: 256 locations of 4 bytes each (mem[512] to mem[1023])

3. Data memory: 512 locations of 4 bytes each (mem[1024] to mem[2047])

Instruction size: 4 bytes = 32 bits

Opcode: 8bits
 Operand 1: 8 bits
 Operand 2: 8 bits
 Operand 3: 8 bits

Instructions:

1. lw r0,0400,0

It will load the contents at memory location 0x0400 into register r0.

Opcode for lw is 0x00

Operand 1 r0 is 0x00

Memory location 0x0400 is divided into two parts (8 bits each)

Operand 2 is bits from d8 to d15

Operand 3 is bits from d0 to d7

Initially,

Content at memory location 0x0400h = 0x11

Content of register r0 is 0x00

After execution

Content at memory location 0x0400h = 0x11

Content of register r0 is 0x11

2. sw r1,0401,0

It will load the contents at memory location 0x0401 into register r0.

Opcode for sw is 0x01

Operand 1 r1 is 0x01

Memory location 1025 is divided into two parts (8 bits each)

Operand 2 is bits from d8 to d15

Operand 3 is bits from d0 to d7

Initially,

Content of register r1 is 0x12

Content at memory location 0x0401h = 0x00

After execution

Screen Shots

1. Initial CPU state (Without any Instructions)

```
Cpu state initially

Content of instruction Memory:

Addr Value Addr Value Addr Value Addr Value Addr Value 200 ff 201 ff 202 ff 203 ff 204 ff 205 ff 206 ff 207 ff 208 ff 209 ff 20a ff 20b ff 20c ff 20d ff 20e ff 20f ff 210 ff 211 ff 212 ff 213 ff 214 ff 215 ff 216 ff 217 ff 218 ff 219 ff 21a ff 21b ff 21c ff 21d ff 21e ff 21f ff 220 ff 221 ff 222 ff 223 ff 224 ff 225 ff 226 ff 227 ff 228 ff 227 ff 224 ff 227 ff
```

Content of Data Memory:											
Addr	Value	Addr	Value	Addr	Value	Addr	Value	Addr	Value	Addr	Value
400	ff	401	ff	402	ff	403	ff	404	ff	405	ff
406	ff	407	ff	408	ff	409	ff	40A	ff	40B	ff
40C	ff	40D	ff	40E	ff	40F	ff	410	ff	411	ff
412	ff	413	ff	414	ff	415	ff	416	ff	417	ff
418	ff	419	ff	41A	ff	41B	ff	41C	ff	41D	ff
41E	ff	41F	ff	420	ff	421	ff	422	ff	423	ff
424	ff	425	ff	426	ff	427	ff	428	ff	429	ff
42A	ff	42B	ff	42C	ff	42D	ff	42E	ff	42F	ff

```
Content of General Purpose Register:

R0 = 0    R1 = 0    R2 = 0    R3 = 0    R4 = 0    R5 = 0    R6 = 0    R7 = 0    R8 = 0    R9 = 0    R10 = 0   R11 = 0   R12 = 0   R13 = 0   R14 = 0   R15 = 0   Content of flag register:

Content of Program Counter:

Content of Stack Pointer:

0000

Content of Base Pointer:

0400
```

2. Initial contents of General purpose registers and memory locations done for assignment 1

Content of Data Memory:											
Addr 400 406 40C 412 418 41E 424	Value 11 ff ff ff ff ff	Addr 401 407 40D 413 419 41F 425	Value ff ff ff ff ff ff	Addr 402 408 40E 414 41A 420 426	Value ff ff ff ff ff ff	Addr 403 409 40F 415 41B 421 427	Value ff ff ff ff ff ff	Addr 404 40A 410 416 41C 422 428	Value ff ff ff ff ff ff	Addr 405 40B 411 417 41D 423 429	Value ff ff ff ff ff ff
42A	ff	42B	ff	42C	ff	42D	ff	42E	ff	42F	ff

```
Content of General Purpose Register:

R0 = 0 R1 = 12 R2 = 0 R3 = 0 R4 = 0 R5 = 0 R6 = 0 R7 = 0
R8 = 0 R9 = 0 R10 = 0 R11 = 0 R12 = 0 R13 = 0 R14 = 0 R15 = 0

Content of flag register: 0 0 0 0 0 0 0

Content of Program Counter: 0000

Content of Stack Pointer: 0000

Content of Base Pointer: 0400
```

3. CPU state after loading all instructions (load 200-203 and store 204-207)

```
Cpu state after loading instructions into memory
Content of instruction Memory:
                           Addr
201
207
20d
213
219
                                                       Addr
202
208
20e
214
21a
                                                                                   Addr
203
209
20f
215
21b
                                                                                                              Addr
204
20a
210
216
21c
Addr
200
                                                                                                                                          Addr
205
20b
211
217
                                        Value
                                                                    Value
                                                                                                Value
                                                                                                                                                       Value
            Value
                                                                                                                           Value
              00
04
ff
ff
ff
                                                                      04
ff
ff
ff
                                                                                                                             01
ff
ff
ff
                                                                                                                                                         01
ff
ff
ff
                                          00
01
ff
ff
ff
                                                                                                  00
206
206
20c
212
                                                                                                  66
66
66
66
```

4. CPU state after executing first instruction (Loading data from memory to register)

Content of Data Memory:											
Addr	Value	Addr	Value	Addr	Value	Addr	Value	Addr	Value	Addr	Value
400	11	401	ff	402	ff	403	ff	404	ff	405	ff
406	ff	407	ff	408	ff	409	$\mathbf{f}\mathbf{f}$	40A	$\mathbf{f}\mathbf{f}$	40B	ff
40C	ff	40D	ff	40E	ff	40F	ff	410	ff	411	ff
412	ff	413	ff	414	ff	415	ff	416	$\mathbf{f}\mathbf{f}$	417	ff
418	ff	419	ff	41A	ff	41B	ff	41C	ff	41 D	ff
41E	ff	41F	ff	420	ff	421	ff	422	ff	423	ff

```
Content of General Purpose Register:

R0 = 11 R1 = 12 R2 = 0 R3 = 0 R4 = 0 R5 = 0 R6 = 0 R7 = 0
R8 = 0 R9 = 0 R10 = 0 R11 = 0 R12 = 0 R13 = 0 R14 = 0 R15 = 0

Content of flag register: 0 0 0 0 0 0 0

Content of Program Counter: 0204

Content of Stack Pointer: 0400

Content of Base Pointer: 04400
```

5. CPU state after executing second instruction (Storing data from register to memory

```
Content of General Purpose Register:

R0 = 11 R1 = 12 R2 = 0 R3 = 0 R4 = 0 R5 = 0 R6 = 0 R7 = 0
R8 = 0 R9 = 0 R10 = 0 R11 = 0 R12 = 0 R13 = 0 R14 = 0 R15 = 0

Content of flag register: 0 0 0 0 0 0 0

Content of Program Counter: 0204

Content of Stack Pointer: 0400

Content of Base Pointer: 0400
```

Content of Data Memory:											
Addr	Value	Addr	Value	Addr	Value	Addr	Value	Addr	Value	Addr	Value
400	11	401	12	402	ff	403	ff	404	ff	405	ff
406	ff	407	ff	408	ff	409	ff	40A	ff	40B	ff
40C	ff	40D	ff	40E	$\mathbf{f}\mathbf{f}$	40F	$\mathbf{f}\mathbf{f}$	410	ff	411	$\mathbf{f}\mathbf{f}$
412	ff	413	ff	414	ff	415	ff	416	ff	417	ff
418	ff	419	ff	41A	ff	41 B	ff	41 C	ff	41 D	ff
41 E	$\mathbf{f}\mathbf{f}$	41F	$\mathbf{f}\mathbf{f}$	420	$\mathbf{f}\mathbf{f}$	421	$\mathbf{f}\mathbf{f}$	422	$\mathbf{f}\mathbf{f}$	423	ff