**Assignment 1 “Best CPU Setup”**

**Group - SS05**

**Memory:** 2048 locations of 1 bytes each (mem[2048]) = 2KB of memory

1. **OS memory:** 256 locations of 4 bytes each (mem[0] to mem[511])
2. **Instruction memory:** 256 locations of 4 bytes each (mem[512] to mem[1023])
3. **Data memory:** 512 locations of 4 bytes each (mem[1024] to mem[2047])

**Instruction size:** 4 bytes = 32 bits

1. **Opcode:** 8bits
2. **Operand 1:** 8 bits
3. **Operand 2:** 8 bits
4. **Operand 3:** 8 bits

**Instructions:**

**1. lw r0,0400,0**

It will load the contents at memory location 0x0400 into register r0.

Opcode for lw is 0x00

Operand 1 r0 is 0x00

Memory location 0x0400 is divided into two parts (8 bits each)

Operand 2 is bits from d8 to d15

Operand 3 is bits from d0 to d7

Initially,

Content at memory location 0x0400h = 0x11

Content of register r0 is 0x00

After execution

Content at memory location 0x0400h = 0x11

Content of register r0 is 0x11

**2. sw r1,0401,0**

It will load the contents at memory location 0x0401 into register r0.

Opcode for sw is 0x01

Operand 1 r1 is 0x01

Memory location 1025 is divided into two parts (8 bits each)

Operand 2 is bits from d8 to d15

Operand 3 is bits from d0 to d7

Initially,

Content of register r1 is 0x12

Content at memory location 0x0401h = 0x00

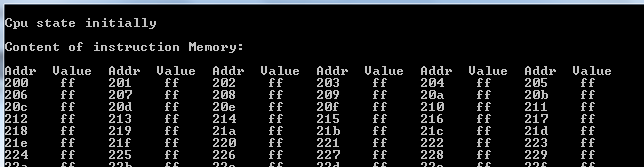
After execution

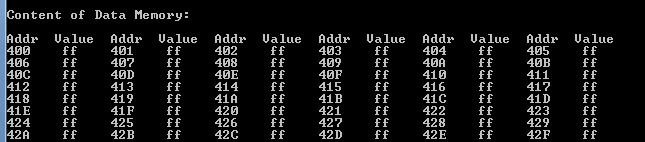
Content of register r1 is 0x12

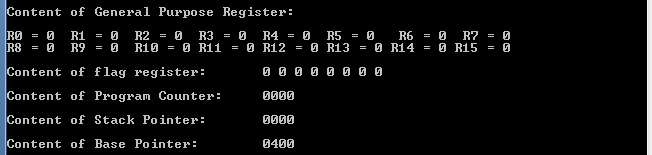
Content at memory location 0x0401h = 0x12

**Screen Shots**

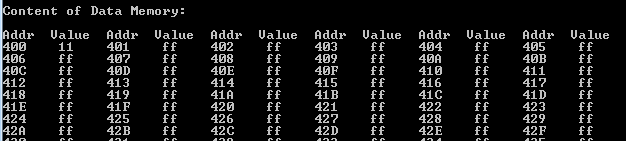
1. Initial CPU state (Without any Instructions)

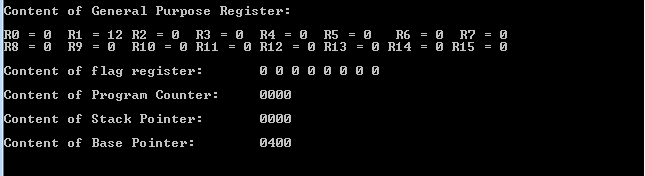




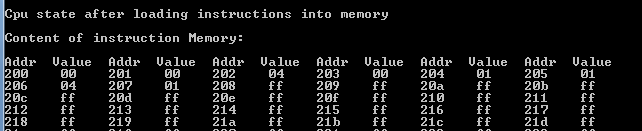


1. Initial contents of General purpose registers and memory locations done for assignment 1

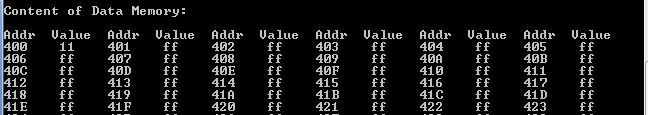


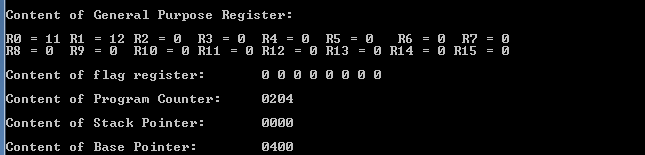


1. CPU state after loading all instructions (load 200-203 and store 204-207)



1. CPU state after executing first instruction (Loading data from memory to register)





1. CPU state after executing second instruction (Storing data from register to memory

