

faulty

### Schema

$$\begin{matrix} t_1 & & & & \\ \cdot & & & & \\ \cdot & & \bullet & \bullet & \bullet \\ \cdot & & & & \\ t_5 & & & & \end{matrix}$$
$$\begin{matrix} t_6 \\ \vdots \\ t_9 \end{matrix} \quad \bullet \quad \bullet \quad \bullet$$

Figure 1 illustrates the evolution of a 4-bit register over four time steps,  $t_{11}$  to  $t_{14}$ . Each time step shows a sequence of 8-bit values (represented in rounded rectangles) that evolve from an initial state. The values are grouped into two rows of four rectangles each. The first row of rectangles for each time step represents the state of the register, and the second row represents the state of the environment. The values are as follows:

- $t_{11}$ : 0000, -0--, -00-, -0-0, -0--0, --0-, --00, ---0
- $t_{12}$ : 1100, 1---, 11--, 1-0-, 1--0, 110-, 11-0, 1-00, 1100, -1--, -10-, -1-0, -100, --0-, --00, ---0
- $t_{13}$ : 1010, 1---, 10--, 1-1-, 1--0, 101-, 10-0, 1-10, 1010, -0--, -01-, -0-0, -010, --1-, --10, ---0
- $t_{14}$ : 1011, 1---, 10--, 1-1-, 1--1, 101-, 10-1, 1-11, 1011, -0--, -01-, -0-1, -011, --1-, --11, ---1

The values are represented in rounded rectangles. Some rectangles are solid, some are dashed, and some are shaded dark gray. The dark gray rectangles represent the final state of the register at each time step.

$t_{15}$  0100

1 - - -	1 0 - -	1 - 1 -	1 - - 1	1 0 1 -	1 0 - 1	1 - 1 1	1 0 1 1
- 0 - -	- 0 1 -	- 0 - 1	- 0 1 1	- - 1 -	- - 1 1	- - - 1	

$t_5$

1 0 1 1	1 - - -	1 0 - -	1 - 1 -	1 - - 1	1 0 1 -	1 0 - 1	1 - 1 1	1 0 1 1
- 0 - -	- 0 1 -	- 0 - 1	- 0 1 1	- - 1 -	- - 1 1	- - - 1		