ELECENG 2EI4 – Electronic Devices and Circuits I

Project 1 Report

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Summary

The goal of this project was to design and build a DC power supply that delivered 3.0 ± 0.1 V at 10 mA from a source that was 120 V (rms) at 1 kHz . For the project, a 120 V source was not used. The AD3 function generator will be used to produce the transformer secondary voltage.

The project was designed as a full-wave, center-tapped rectifier followed by an RC filter and resistive load [2]. A regulator was not used. The center-tapped full-wave topology was chosen to reduce diode conduction loss, which is best for a low-voltage supply, which in our case was a 3 V supply. From calculations, the required AD3 input sinusoid amplitude was chosen to make sure the filtered output maintained an average near 3.0 V with ripple small enough to remain within ± 0.1 V of the supply voltage, under the 10 mA load [1].

Design

Transformer

The design for the DC power supply consisted of a transformer, rectifier, filter, and regulator. For the project, a transformer was not used, but instead a secondary voltage produced from the AD3 acted as the transformer voltage. To emulate the center-tapped transformer, two sine sources at 1 kHz, 0 V offset, equal amplitudes, and a 180° phase shift were used [1].

The load current at 3.0 V was 10 mA. This required the equivalent load to be:

$$R = \frac{V}{I} = \frac{3.0\,V}{0.010\,A} = 300\,\Omega$$

With full-wave rectification, the ripple frequency is:

$$f_r = 2f = 2(1kHz) = 2\,kHz$$

To estimate the capacitor ripple, the standard approximation below was used:

$$V_{pp} \approx \frac{I_L}{f_r C}$$

Using the values of $V_{pp} = 0.2$, $I_L = 10$ mA, $f_r = 2$ kHz, the capacitor value required can be calculated:

$$V_{pp} = \frac{I_L}{f_r C}$$

$$0.2\,V = \frac{0.010\,A}{(2000\,Hz)C}$$

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$$C = 25\,\mu F$$

For a center-tapped full-wave rectifier, there is only one diode that conducts per half-cycle:

$$V_{Peak} = V_{Half\ peak} - V_D$$

The output voltage can be approximated to:

$$V_{out} \approx (V_{Half\ peak} - V_D) - \frac{V_{pp}}{2}$$

Solve for $V_{Half\ peak}$ with respect to $V_{Out} = 3.0\,V$:

$$V_{Half\ peak} = V_{Out} + V_D + \frac{V_{pp}}{2}$$

$$V_{Half\ peak} = 3.0\,V + 0.7\,V + 0.10 = 3.8\,V$$

Therefore, the secondary transformer voltages from the AD3 are ≈ 3.8 V, with one source having phase shift of 180°.

The theoretical transformer turns ratio from a 120 V (rms) source, at 1 kHz can be calculated as:

$$V_{Half,\,rms} = \frac{V_{pp}}{\sqrt{2}} \approx 2.72\,V\,(rms)$$

The end-to-end secondary RMS for a center-tapped winding approximates to:

$$V_{i,\,rms} = 2V_{Half,\,rms} \approx 5.44\,V\,(rms)$$

Using the provided V (rms) and the secondary RMS, the turns ratio equates to:

$$a = \frac{V_g}{V_i} = \frac{120}{5.44} \approx 22.1 \Rightarrow 22{:}\,1\ ratio$$

Rectifier

The topology of the chosen rectifier is a full-wave, center-tapped rectifier, which consists of two diodes, where one is conducting, per half-cycle. This was chosen as it provides full-wave rectification while minimizing the forward conduction. This improves the headroom for a 3V output. The diodes are two identical 1N4148 diodes, with voltages ~0.7 V and current ~10 mA [2].

Filter

The filter chosen for this project was a capacitor (25 **μ**F) connected in parallel with a 300 **Ω** resistor. This provides a ripple of ~0.20 V peak-to-peak at the load, with a ripple frequency of 2 kHz [1]. The time constant for the filter is:

$$\tau = R_L C = 300\,\Omega\,(25 \times 10^{-6}) = 7.5\,ms$$

This is larger than the ripple period, meaning the ripple is reduced effectively:

$$T = \frac{1}{f_r} = \frac{1}{2000\,Hz} = 0.5\,ms$$

Regulator

A regulator was not used for this project, as the output values required were achieved through the effective design of the other components [1].

Circuit schematic

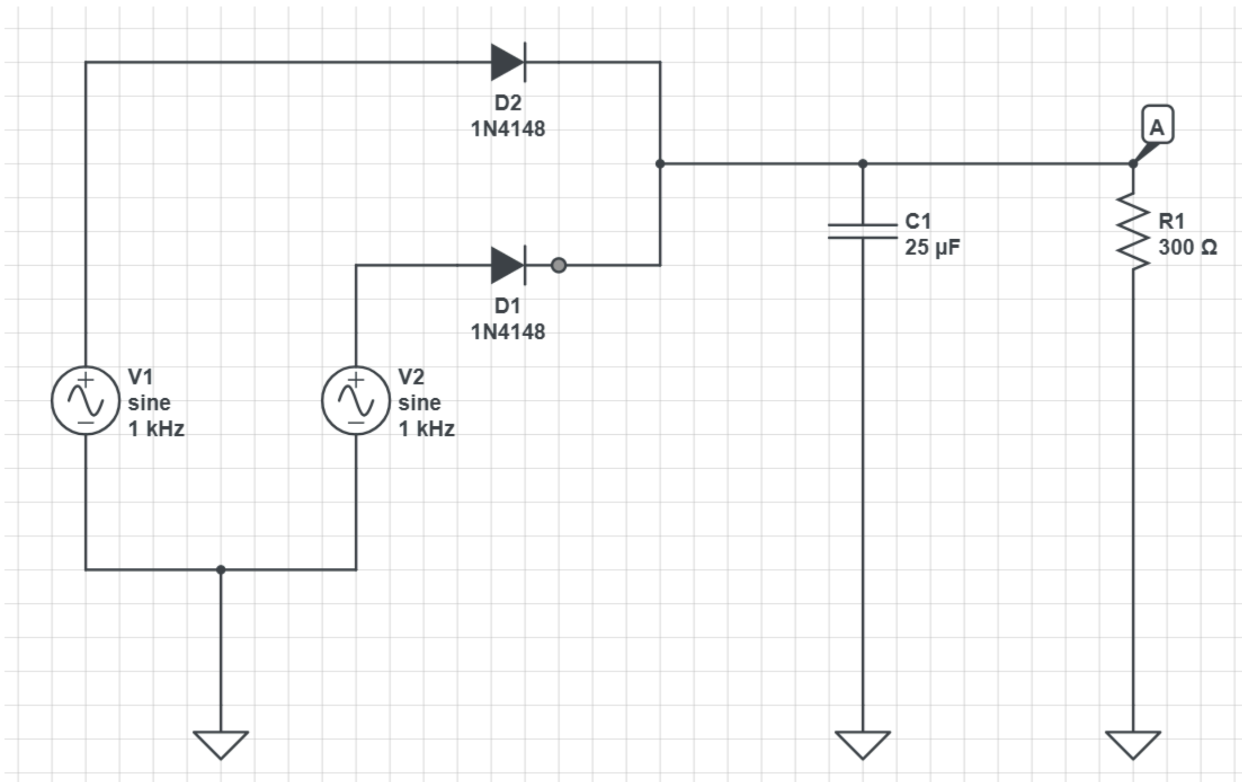

Figure 1: Image of circuit schematic drawn using CircuitLab. Image shows all required components of circuit, including 2 sinusoidal voltage sources (transformer), 2 diodes (rectifier), and the capacitor and load resistor connected in parallel (filter).

Expected performance, design tradeoffs, margins, component ratings and safety

The expected performance of the circuit should yield the following:

- $I_L \approx 10$ mA with $R_L = 300\ \Omega$ at $V_{out} = 3.0$ V
- The ripple $V_{pp} \approx 0.20$ V at full load
- The output stays approximately within 3.0 ± 0.1 V

Design tradeoffs/margins include:

- Center-tapped full-wave rectification reduces diode losses which improves low-voltage performance

- The ripple decreases if the capacitance increases, or if the load current decreases. This means that at minimum the value of the capacitance should be 25 **μ**F, but it can be higher if there are any components lacing
- The output depends on the forward drop of the diode and the charging behaviour of the capacitor [2]. Amplitude of the voltage sources provided by the AD3 may need to be adjusted to meet the tolerance band.
- The required resistive load for the circuit is 300 Ω to satisfy the 10 mA at 3 V output requirement. However, a 300 Ω resistor is not available for use within the circuit components provided. Therefore, a 330 Ω resistor was used in replacement. This change in resistive loads requires a change in the voltage source, with amplitudes around 3.8-4.0 V. For the simulation as well as the physical test, the amplitudes used was 3.9 V [1].

General safety practices for the project include simulating before building, verifying parts and their parameters, ensuring current/voltage limits are not exceeded, and to heed the project warning at all times.

Measurement and Analysis

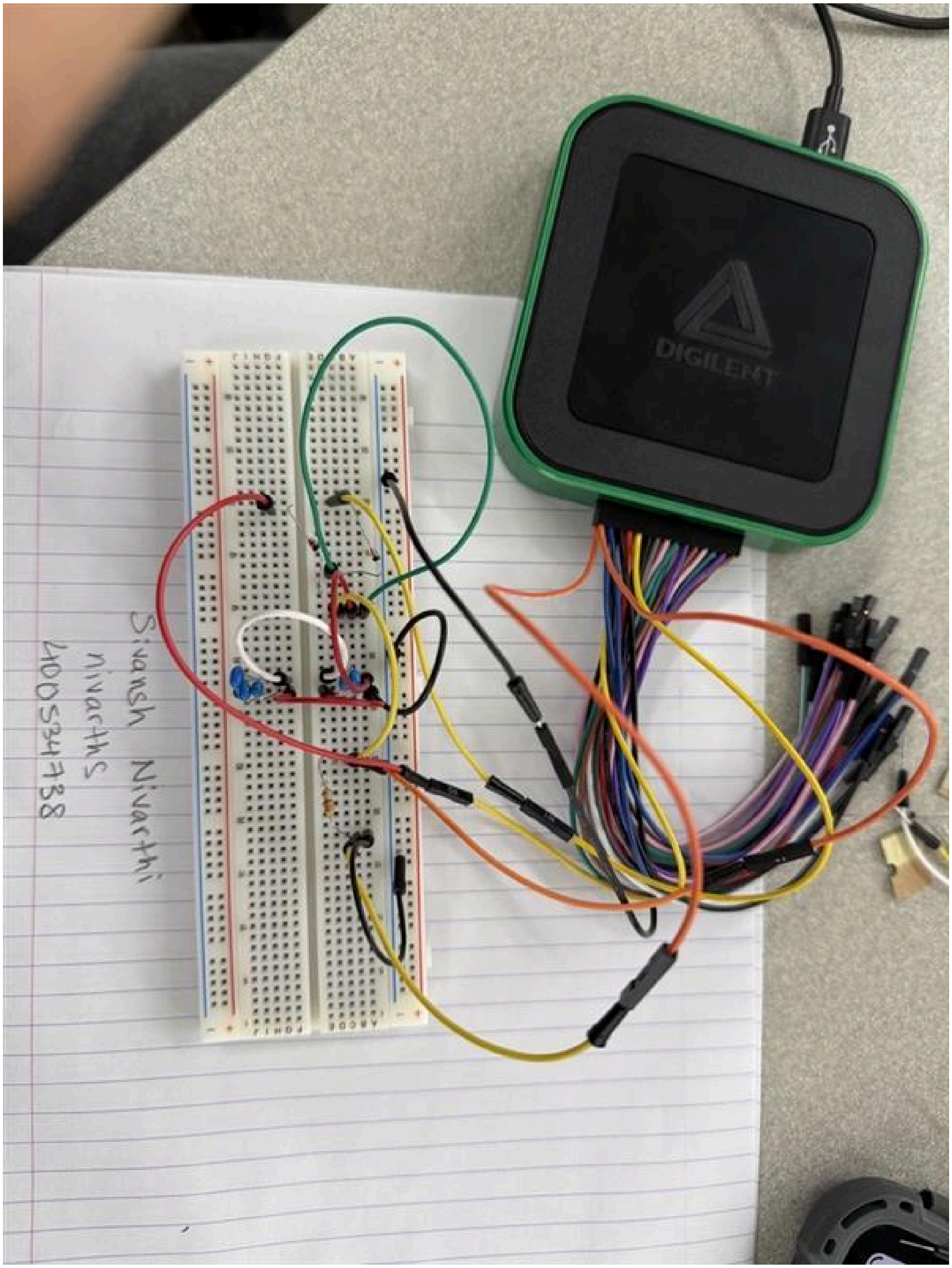

Figure 2: Image shows the breadboard implementation of the circuit with a 25 µF filter capacitor and a 330 Ω load, voltage sources provided by the AD3.

Measurement procedure

To evaluate the performance of the DC supply, the circuit was measured using the AD3 and Waveforms software. Wavegen channels 1 and 2 were used as the voltage sources, configured as sine waves at 1 kHz, 0 V offset, equal amplitudes of 3.9 V and 180° out of phase. The scope of the AD3 measured the output node voltage and the math channel was used to plot the current across the load.

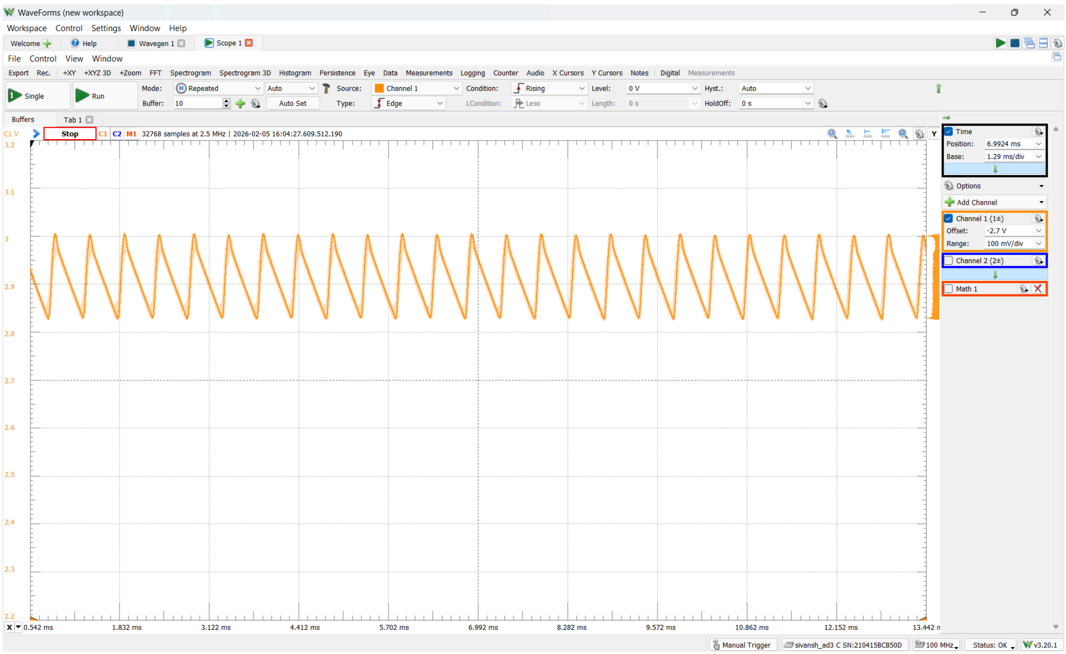

Figure 3: Image showing the output node voltage measured using the scope. The voltage waveform oscillates between ~2.85 and ~3 V.

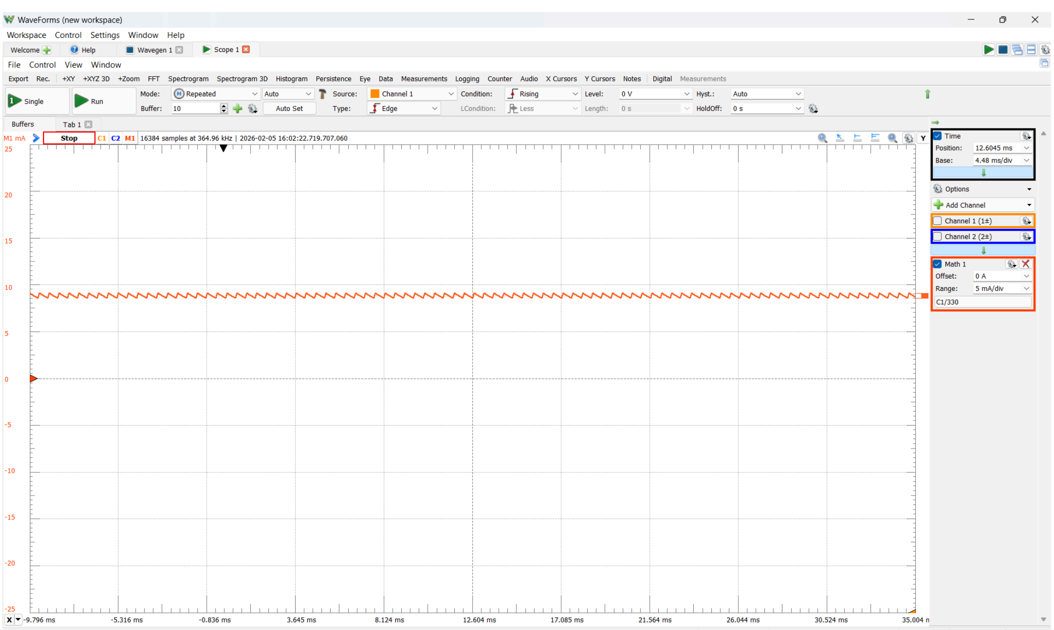

Figure 4: Image showing the output load current measured using the math channel on Waveforms.

Simulation

Simulation circuit schematic

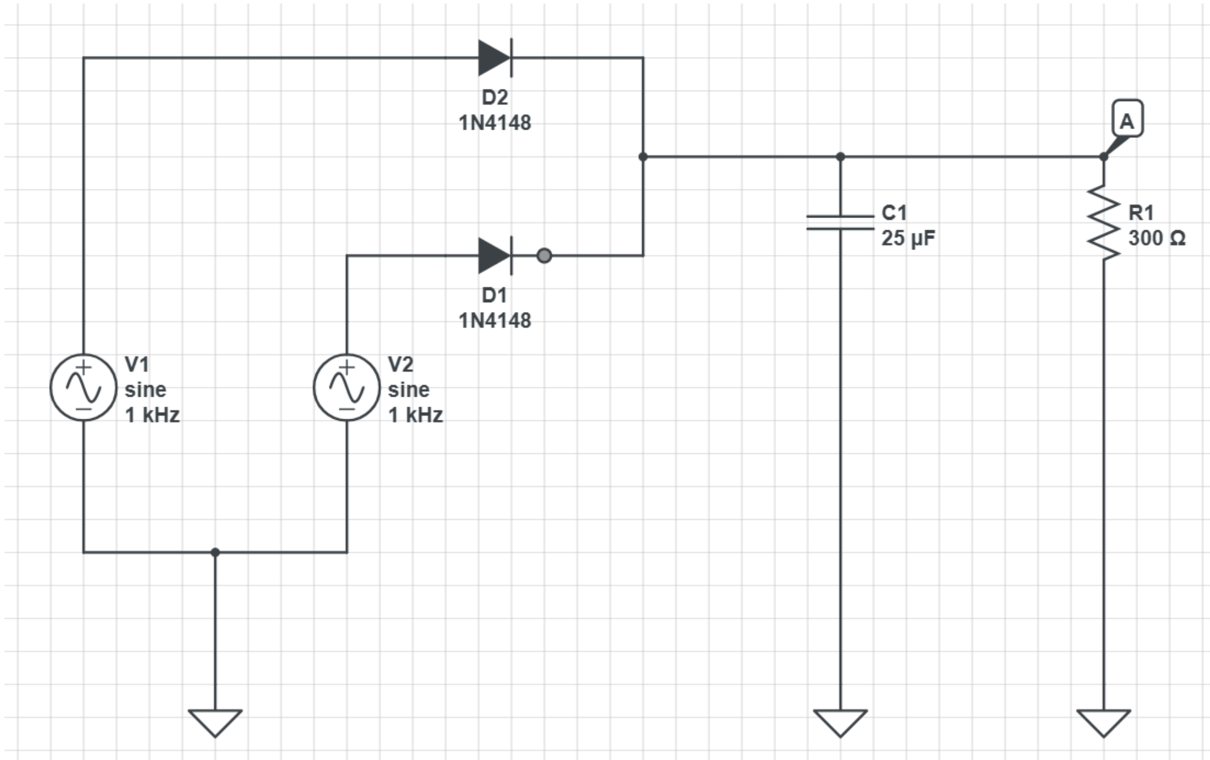

Figure 5: Image of simulation circuit schematic drawn using CircuitLab. Image shows all required components of circuit, including 2 sinusoidal voltage sources (transformer), 2 diodes (rectifier), and the capacitor and load resistor connected in parallel (filter).

Netlist

- V1
    - Sine source
    - 1 kHz
    - Peak-to-peak voltage: 3.9 V
    - Phase 0°
- V2
    - Sine source
    - 1 kHz
    - Peak-to-peak voltage: 3.9 V
    - Phase 180°
- D1, D2: 1N4148
- C1: 25 **µ**F
- R1: 330 Ω
- Output node: node A

Simulation Conditions

A time-domain (transient) simulation was performed to view the output results/plots, the capacitor charging, and steady-state ripple:

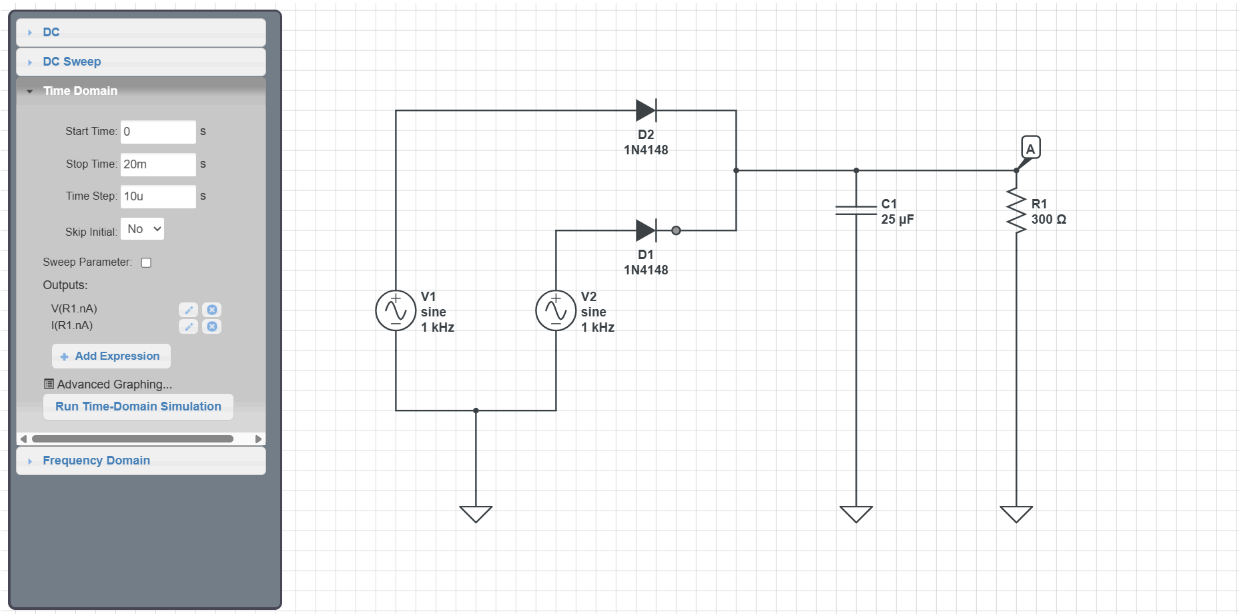

Figure 6: Image of simulation circuit schematic and simulation conditions, implemented using CircuitLab. Simulation conditions include a start time of 0 s, stop time of 20 ms, and a step time of 10 **µ**s.

Simulation Output

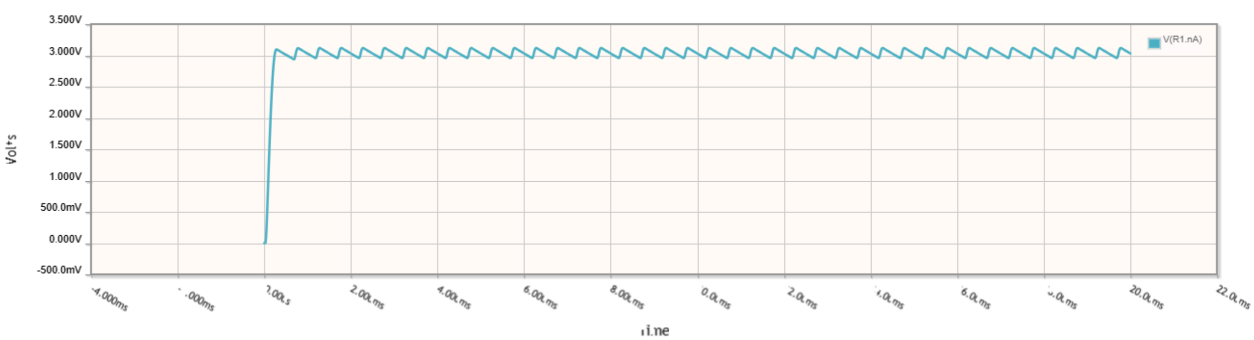

Figure 7: Image of simulation voltage plot through CircuitLab. Simulation shows the capacitor charging, the voltage oscillations and the ripple

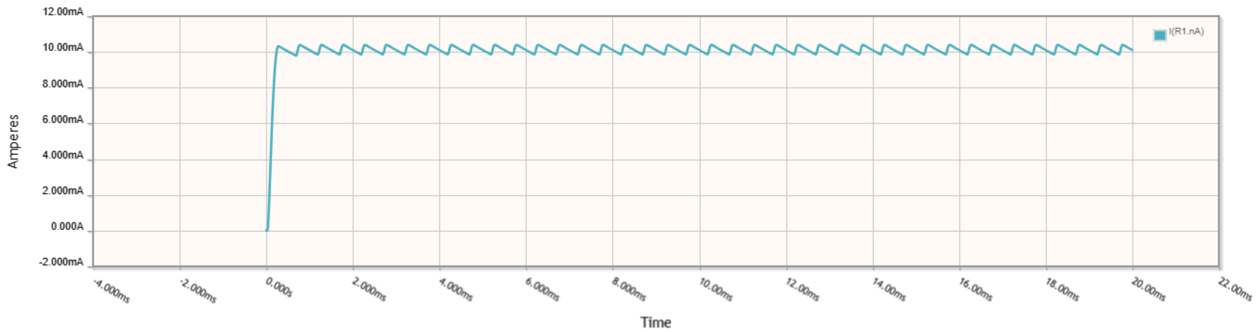

Figure 8: Image of simulation current plot through CircuitLab. Simulation shows the capacitor charging, the current oscillations and the ripple

Discussion

The full-wave center-tapped rectifier circuit was designed to provide a low-voltage DC output using two diodes, a capacitive filter, and a resistive load [2]. No regulator was used, and no transformer was explicitly used, but the voltage was modified to account for a transformer. Circuit design tradeoffs, component ratings, and safety considerations were evaluated to ensure reliable and safe operation of the circuit [1].

Comparison of Design, Simulation, and Measurement Results

From calculations, the expected DC output voltage was 3.0 V. The ripple voltage was predicted to be small due to the full-wave rectification.

Simulation results were very similar to the design predictions. CircuitLab simulations showed an average output voltage of approximately 2.9–3.0 V across the 300 Ω load, with a small triangular ripple consistent with capacitor discharge, between the peaks. The simulated output current, obtained using Ohm's law, was ~10 mA, which aligned with theoretical expectations.

Experimental measurements also produced a DC output of 2.8-3.0 V with visible ripple at twice the input frequency. The measured voltage and current waveforms were consistent with both design calculations and simulation, in terms of shape and magnitude, confirming correct circuit design.

Discrepancies Observed

Minor discrepancies were observed between the expected results, simulation results and physical design results. The measured output voltage was slightly lower than the simulated value, which can be attributed to non-ideal component behavior, such as the diodes, resistors, and capacitors, as they all may not be the exact values as marketed. Additional voltage drops due to breadboard contact resistance and wiring were also present.

Design and Measurement Limitations

One limitation of the design is variance in the voltage. The output voltage varies slightly with load current and input amplitude, and ripple remains present at the output.

The measurement process also introduced limitations. Oscilloscope probing affected the precision of ripple measurements. Additionally, current was not measured directly but was instead calculated and plotted from the measured voltage using Ohm's law, which assumes the exact resistor value. Furthermore, the circuit design needed a 300 Ω resistor, but the only available one similar was a 330 Ω resistor, causing design changes in the values of the components [1].

Measurement Challenges and Troubleshooting

During measurements, unstable waveforms were observed due to incorrect grounding and probe placement. This was fixed by ensuring a common ground reference between the waveform generator, oscilloscope, and circuit ground.

References

[1] A. S. . Sedra, K. C. . Smith, T. Chan. Carusone, and V. C. . Gaudet, Microelectronic circuits. Oxford University Press, 2020.

[2] 1, https://uomus.edu.iq/img/lectures21/MUCLecture_2024_11411910.pdf (accessed Feb. 8, 2026).