Vending Machine Design and Simulation - Status Report

Completed Tasks

Task	Description
Verilog Design (Vivado)	Designed and simulated the vending machine using FSM in Vivado (behavioral model)
Cocotb Testbench	Built Python-based testbench using Cocotb for simulation outside Vivado
GTKWave Integration	Successfully generated VCD and visualized waveforms using GTKWave
VCD Generation	$dumpfile configured to produce waveform output

Pending Tasks

Task	Description	Reason / Notes
Flask Backend	Set up Flask app to run test, synthesis, validation, and view logs	In development
HTML/CSS Frontend	Build web interface with buttons, logs, waveform control	Not yet started
Frontend Integration	Connect HTML frontend with Flask backend (routes, rendering)	Needs Flask templates, button action wiring
Yosys Synthesis	Integrate Yosys to generate netlist (write_json) from Verilog	Not yet run
Netlist Validation	Write backend code to validate JSON netlist format	Planned after synthesis setup
Logs	Display simulation/synthesis logs in frontend via SQLite DB	DB setup pending