Software Requirement Specification(SRS)

**Project Title:** Vending Machine Design and Simulation

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**Tools Used:** Verilog , Vivado Simulator

**Duration:** 1 Week

# 1. Introduction

## 1.1 Purpose

The purpose of this project is to design and simulate a vending machine using Verilog . The system accepts money input, allows product selection, returns appropriate change, and handles various user scenarios like overpayment, underpayment, and invalid selections.

## 1.2 Scope

This vending machine supports up to 8 different products. It uses a finite state machine (FSM) logic to dispense the product if sufficient money is inserted, otherwise returns the money. The simulation is performed using Vivado software.

# 2. System Description

## 2.1 Input Signals

- clk: Clock input for synchronization  
- reset: Resets the system  
- money\_in[3:0]: Represents the amount of money inserted (1 to 15)  
- product\_code[2:0]: Selects the product (0 to 7)

## 2.2 Output Signals

- dispense: Indicates whether the product is dispensed (1 = Yes, 0 = No)  
- change[3:0]: Returns the remaining money after a successful purchase

## 2.3 Product Pricing

- Product A (000): ₹4  
- Product B (001): ₹5  
- Product C (010): ₹7  
- Product D (011): ₹3  
- Others: Treated as invalid, assigned price ₹15

# 3. Working Principle

- If the reset is active, all outputs are cleared.  
- For a valid product selection:  
 - If money\_in ≥ price: product is dispensed and change is returned.  
 - If money\_in < price: product is not dispensed; the full amount is returned.  
- Invalid product codes are priced at ₹15 to prevent dispensing.

# 4. Simulation Results

The simulation includes the following test cases:  
- Exact amount inserted  
- Excess amount inserted  
- Insufficient funds  
- Invalid product selection  
  
The waveform shows proper output changes for dispense and change based on inputs, ensuring the logic correctness of the vending machine design.

# 5. Sample Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| money\_in | product\_code | product\_price | dispense | change |
| 4 | 000 | 4 | 1 | 0 |
| 2 | 000 | 4 | 0 | 2 |
| 6 | 001 | 5 | 1 | 1 |
| 7 | 010 | 7 | 1 | 0 |
| 10 | 100 | 15 | 0 | 10 |
| 15 | 100 | 15 | 1 | 0 |

# 6. Conclusion

This project demonstrates the implementation of a simple FSM-based vending machine using Verilog . The system is successfully verified with various test scenarios in Vivado. The design logic is clean, scalable, and adaptable for hardware synthesis or extension to physical FPGA implementation.