Lab 2: Introduction to VHDL

In this lab, you are asked to **debug and test** a combinational circuit on your BASYS3 using VHDL. Combinational logic circuits are time-independent, memoryless circuits whose outputs solely depend on the combination of inputs.

You are asked to debug a combinational VHDL code. The necessary files are available in Moodle. Try to synthesize/implement the code and report the error messages you receive. The Vivado & BASYS References on Moodle will guide you on how to use VHDL and Vivado. Read the tutorials.

Research and try to answer the following questions in your report:

- How does one specify the inputs and outputs of a module in VHDL?
- How does one use a module inside another code/module? What does PORT MAP do?
- What is a constraint file? How does it relate your code to the pins on your FPGA?
- What is the purpose of writing a testbench?

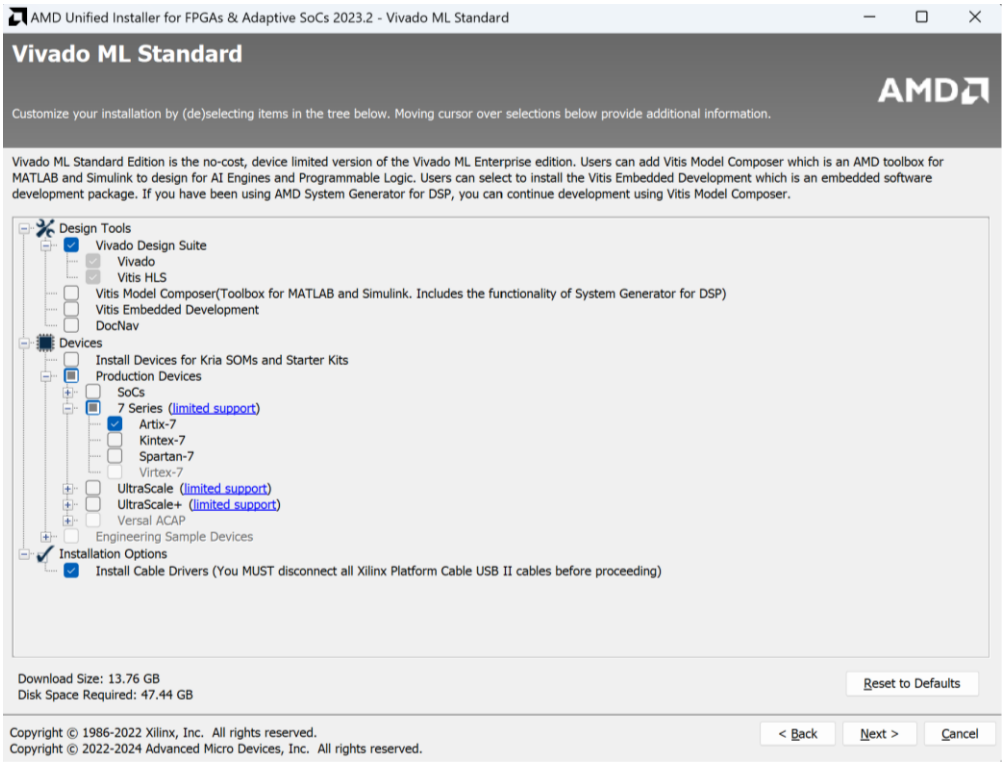
1) Modify the code submodule1.vhd line 14, 15 and 16. Change the logic gates to the corresponding gates given in the table below.
2) Investigate the circuit given, find and fix 6 bugs while taking screenshots of the error messages each bug throw.
3) You are also expected to demonstrate this circuit on your Basys 3 FPGA. The code includes a constraint file that uses the switches as inputs and LEDs as outputs. You can check which pin corresponds to which switch/LED/etc from the Basys 3 Reference Manual, which is also on Moodle. Program your device. Once your device is working, **show it to your TA** and get their approval. In your report, include example photos of your working FPGA (Photos of 5 different inputs/outputs are acceptable).
4) Write a testbench code to simulate the inputs **sequentially** and display the output waveform (Follow the tutorial). Compare the simulation to the implemented design on BASYS3 and confirm the design works as intended. **Show this to your TA** and get their approval. Include a screenshot of the waveform in your report (for 8 inputs there should be all 256 combinations in the waveform). D
5) Draw the RTL schematic in Vivado. Notice that there is two more schematics under "Synthesized Design" and under "Implemented Design". Draw all three schematics and compare them. Explain how those schematics correlate with the simulation results.
6) Do not forget to add all the code that you have **changed** to your report.

For the logic gates in your circuit, you will select them based on the last digit of your ID number.

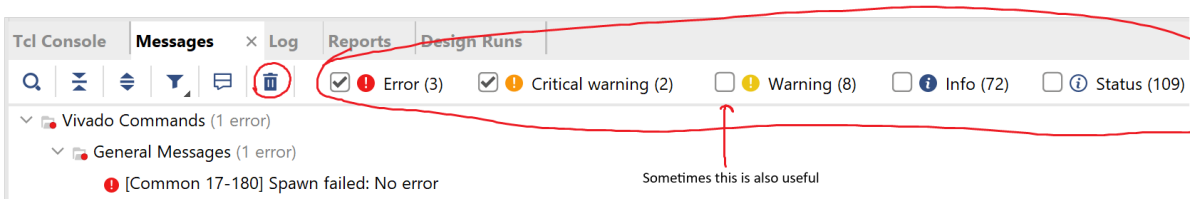
Operations	Last digit of ID number
AND OR XOR	0
XNOR NAND OR	1
XOR XNOR AND	2
AND XOR XNOR	3
OR AND NAND	4
NAND XOR XNOR	5
NAND NAND OR	6
OR OR XOR	7
XOR AND OR	8
XNOR XNOR AND	9

Some hints

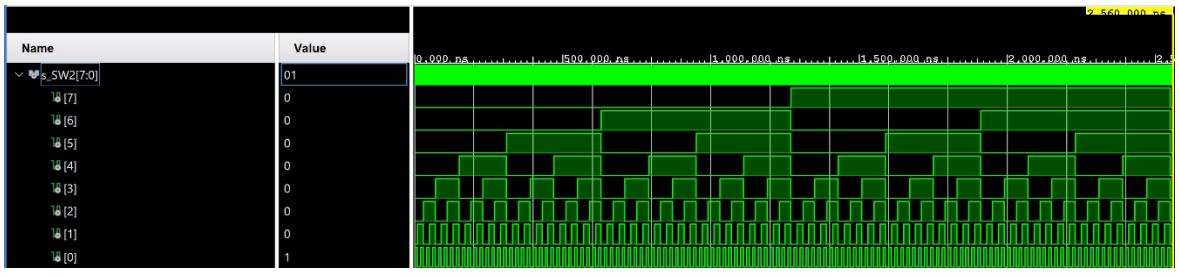
1) Before the lab you have to install Vivado (Standard edition). The minimum required install size is 47GB. You can also use the computers in the labs which have Vivado preinstalled but which are also very slow.



2) While debugging, use the trash can button which deletes the old error messages. Also set it to only report errors and critical warnings. Sometimes warnings can also be useful.



3) Simulating the inputs **sequentially** implies the following:



Note that each value is shown for 10ns and the whole simulation is 2560ns long.