
























 clk  
 reset  
 step\_en  
 ack\_n  
 mdo[31:0]  
 mac\_state[1:0]  
 dlx\_state[4:0]  
 wr\_n  
 as\_n  
 d[31:0]  
 mao[31:0]  
 mdo[31:0]  
 mao[31:0]  
 d[31:0]  
 alu\_o[31:0]  
 aluf[2:0]  
 do[31:0]  
 din[31:0]  
 rd[4:0]  
 mdr[31:0]  
 rs1[4:0]  
 rs2[4:0]  
 rega[31:0]  
 regb[31:0]  
 din\_regc[31:0]  
 pc[31:0]

