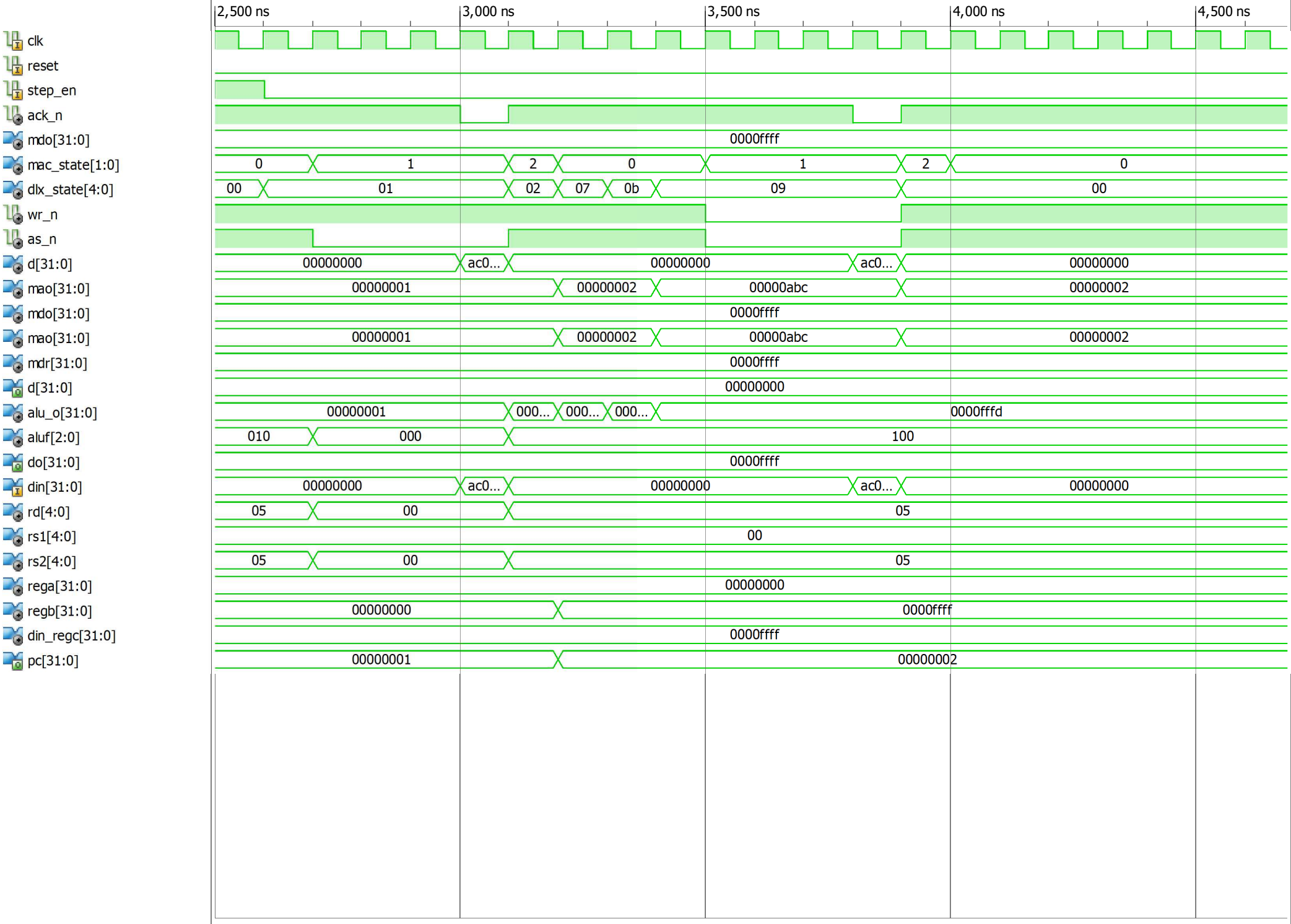
2,500 ns
3,000 ns
3,500 ns
4,000 ns
4,500 ns
clk
reset
step_en
ack_n
mdo[31:0]
mac_state[1:0]
dlx_state[4:0]
wr_n
as_n
d[31:0]
mao[31:0]
mdo[31:0]
mao[31:0]
mdr[31:0]
d[31:0]
alu_o[31:0]
aluf[2:0]
do[31:0]
din[31:0]
rd[4:0]
rs1[4:0]
rs2[4:0]
rega[31:0]
regb[31:0]
din_regc[31:0]
pc[31:0]
0000ffff
0 1 2 0 1 2 0
00 01 02 07 0b 09 00
00000000 ac0... 00000000 ac0... 00000000
00000001 00000002 00000abc 00000002
0000ffff
00000001 00000002 00000abc 00000002
0000ffff
00000000
00000001 000... 000... 000... 0000fffd
010 000 100
0000ffff
00000000 ac0... 00000000 ac0... 00000000
05 00 05
00
05 00 05
00000000
00000000 0000ffff
0000ffff
00000001 00000002