
























 clk
 reset
 step_en
 ack_n
 mdo[31:0]
 mac_state[1:0]
 dlx_state[4:0]
 wr_n
 as_n
 d[31:0]
 mao[31:0]
 mdo[31:0]
 mao[31:0]
 d[31:0]
 alu_o[31:0]
 aluf[2:0]
 do[31:0]
 din[31:0]
 rd[4:0]
 mdr[31:0]
 rs1[4:0]
 rs2[4:0]
 rega[31:0]
 regb[31:0]
 din_regc[31:0]
 pc[31:0]

