Signal	Values
clk	
reset	
step_en	
ack_n	
mac_state[1:0]	0 / 1 / 2 / 0
dlx_state[4:0]	00 / 01 / 02 / 05 / 0d / 00
wr_n	
as_n	
d[31:0]	00000000 / 2c2... / 00000000
mao[31:0]	00000010 / 00000011
mdo[31:0]	0000ffff
mao[31:0]	00000010 / 00000011
mdr[31:0]	0000ffff
d[31:0]	00000000 / 000... / 00000000
alu_o[31:0]	00000009 / 000... / 000... / 000... / 00000000
aluf[2:0]	010 / 000 / 111 / 011 / 111
do[31:0]	0000ffff
din[31:0]	00000000 / 2c2... / 00000000
rd[4:0]	01 / 00 / 01
rs1[4:0]	00 / 01
rs2[4:0]	01 / 00 / 01
rega[31:0]	00000000 / 00000002
regb[31:0]	00000007 / 00000002
din_regc[31:0]	00000002 / 00000001
pc[31:0]	00000010 / 00000011

Time axis: 35,500 ns, 36,000 ns, 36,500 ns, 37,000 ns, 37,500 ns