

OOU-CSC263 Digital Computer Circuitry

Experiments Assignment

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Matric Number: SCI/24/25/0231

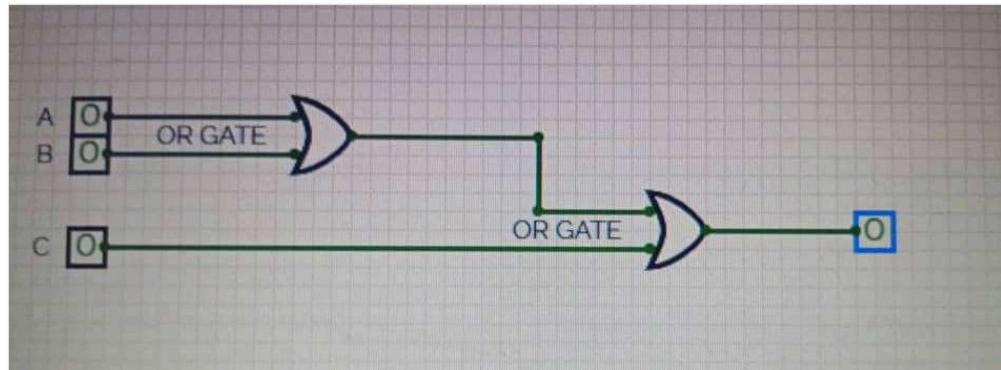
Department: Computer Science

Question 1: Three-Input OR Gate

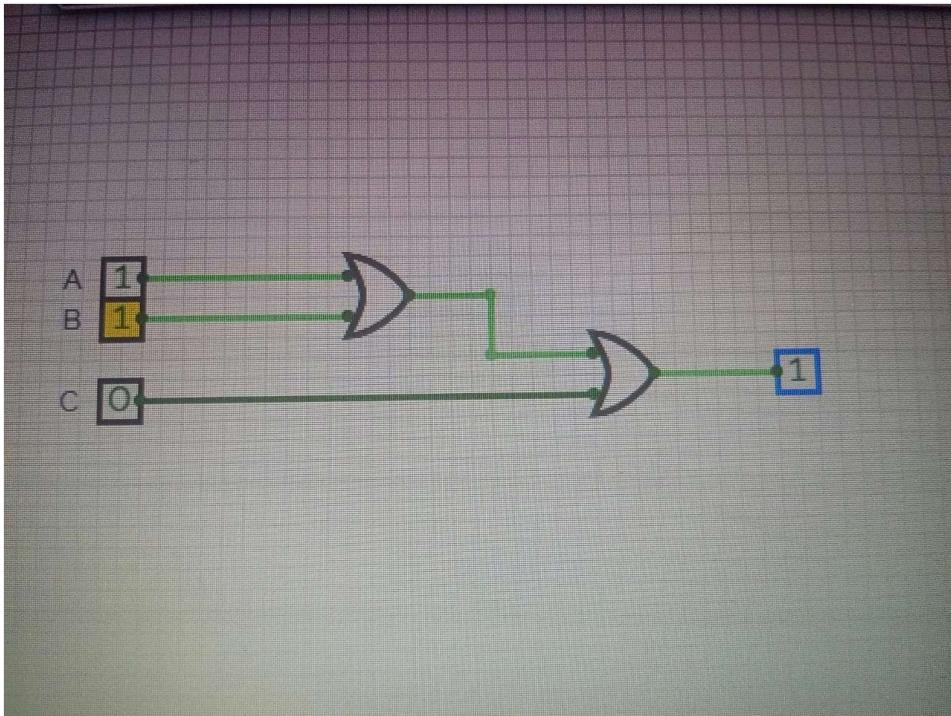
a) Truth Table for Three-Input OR Gate

A	B	C	Output (A+B+C)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

b) Three-Input OR Gate



c) CircuitVerse Implementation



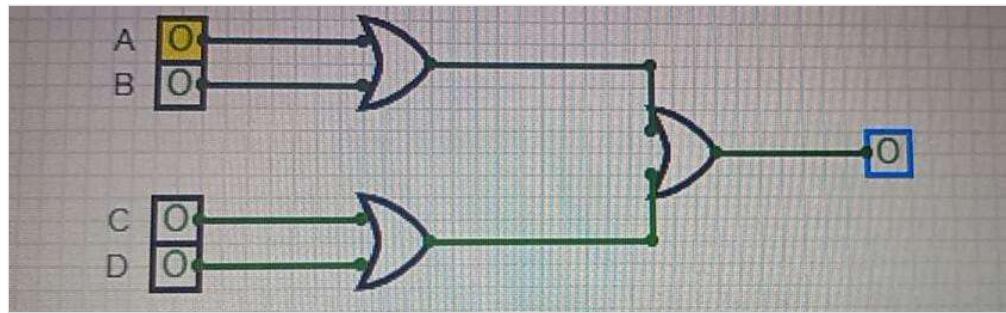
Question 2: Four-Input OR Gate

a) Truth Table for Four-Input OR Gate

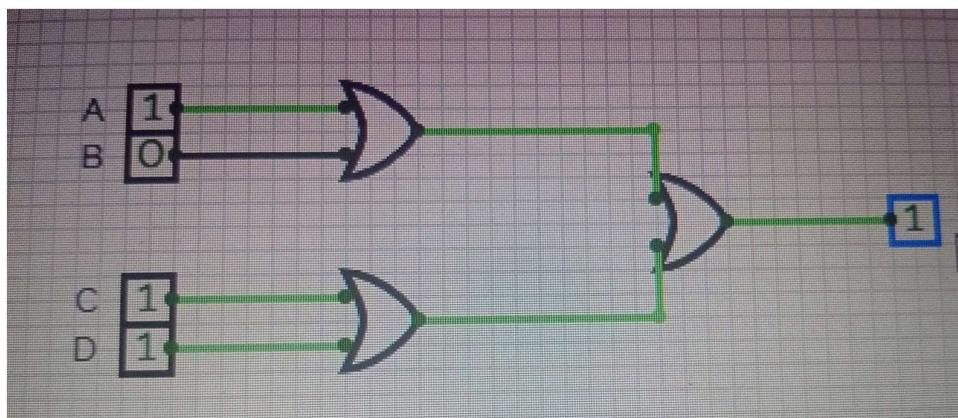
A	B	C	D	Output (A+B+C+D)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1

1	0	1	1		1
1	1	0	0		1
1	1	0	1		1
1	1	1	0		1
1	1	1	1		1

b) Four-Input OR Gate



c) CircuitVerse Implementation



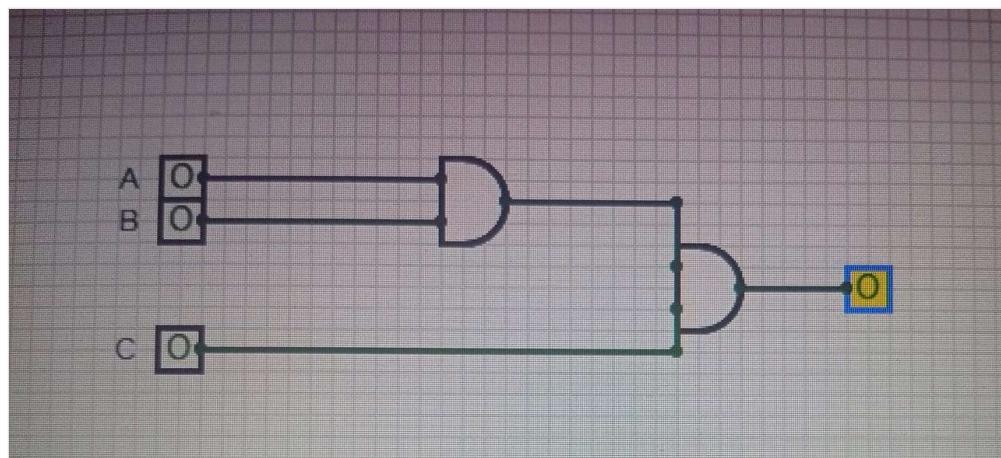
Question 3: Three-Input AND Gate

a) Truth Table for Three-Input AND Gate

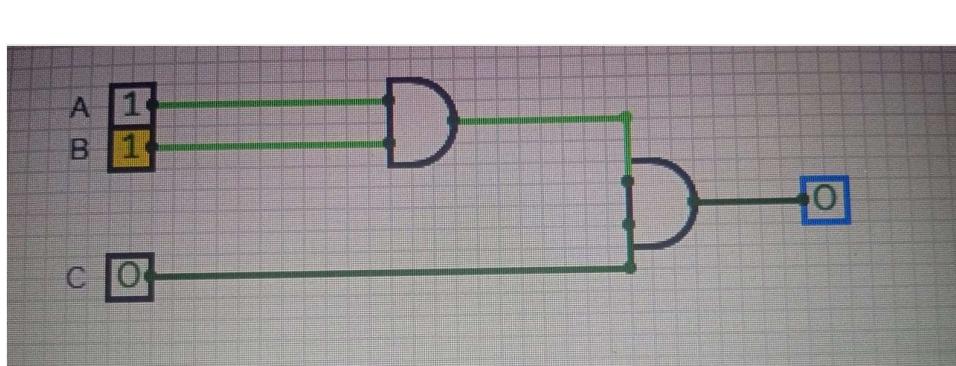
A	B	C	Output (A·B·C)
0	0	0	0
0	0	1	0

0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

b) Three-Input AND Gate



c) CircuitVerse Implementation



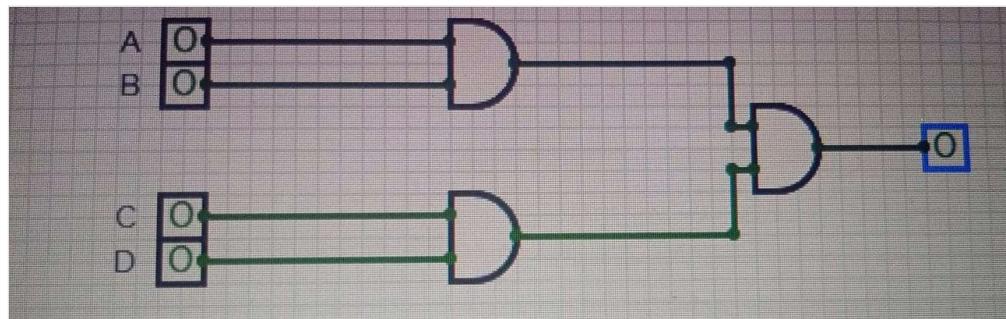
Question 4: Four-Input AND Gate

a) Truth Table for Four-Input AND Gate

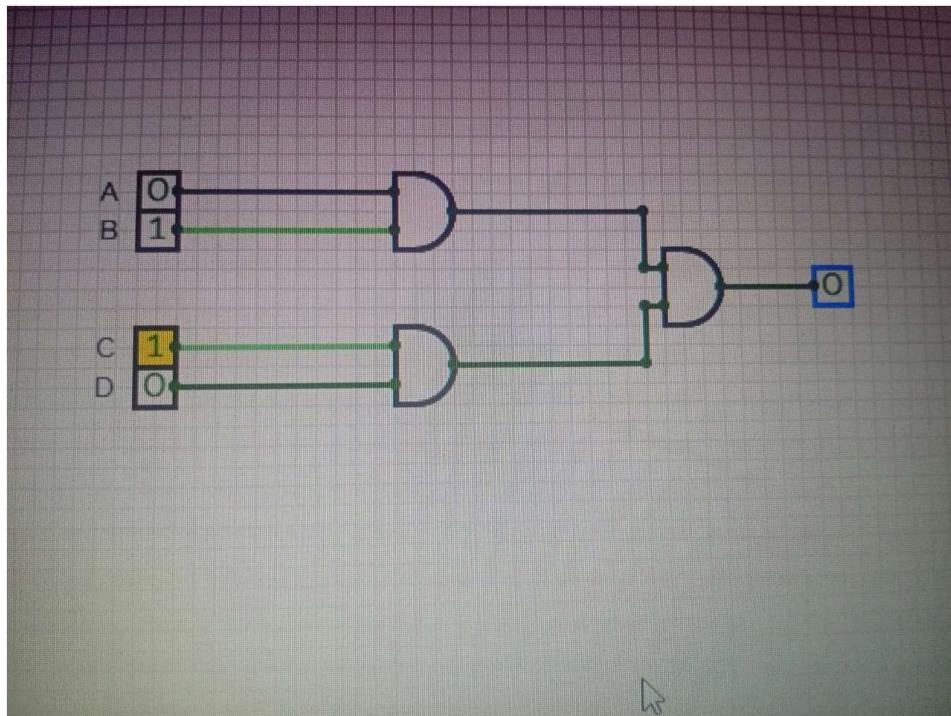
A	B	C	D	Output (A·B·C·D)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

b) Four-Input AND Gate



c) CircuitVerse Implementation



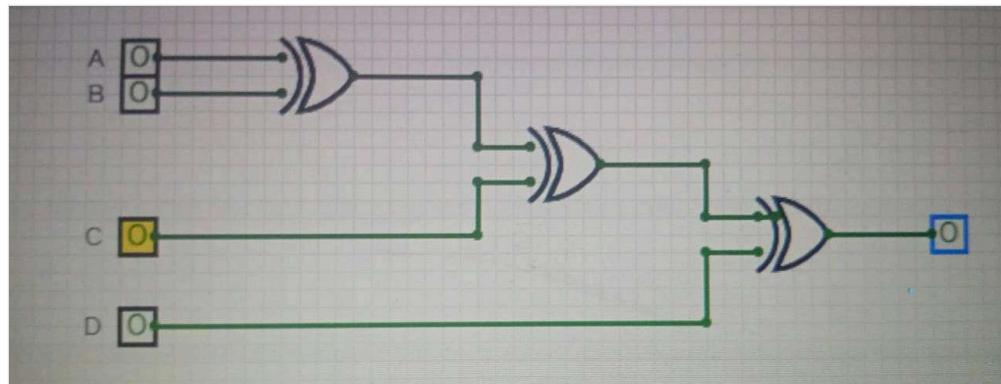
Question 5: Four-Input EXCLUSIVE-OR Gate

a) Truth Table for Four-Input EXCLUSIVE-OR Gate

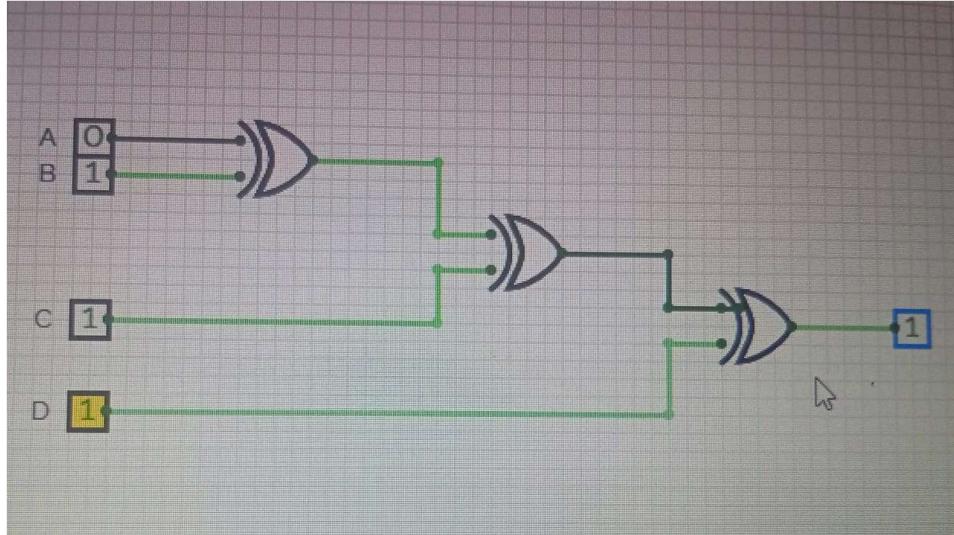
A	B	C	D	Output ($A \oplus B \oplus C \oplus D$)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0

1	0	1	1		1
1	1	0	0		0
1	1	0	1		1
1	1	1	0		1
1	1	1	1		0

b) Four-Input EXCLUSIVE-OR Gate



c) CircuitVerse Implementation



Circuit implemented using cascaded 2-input XOR gates as required by CircuitVerse limitations.