1. Description

1.1. Project

Project Name	FInalCode_SeniorDesign
Board Name	NUCLEO-L476RG
Generated with:	STM32CubeMX 5.0.0
Date	03/05/2019

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476RGTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration

Top pins (left to right): TIM4_CH4, TIM4_CH3, I2C1_SDA, I2C1_SCL, SWO, TCK

VDD	VSS	PB9	PB8	BOO..	PB7	PB6	PB5	PB4 (..	PB3	PD2	PC12	PC11	PC10	PA15..	PA14..

Left side pins:

	VBAT
B1 [Blue PushButton]	PC13
RCC_OSC32_IN	PC14..
RCC_OSC32_OUT	PC15..
RCC_OSC_IN	PH0-..
RCC_OSC_OUT	PH1-..
	NRST
I2C3_SCL	PC0
I2C3_SDA	PC1
	PC2
	PC3
	VSS..
	VDD..
TIM2_CH1	PA0
TIM2_CH2	PA1
USART_TX	PA2

Right side pins:

VDD..	
VSS	
PA13..	TMS
PA12	
PA11	TIM1_CH4
PA10	TIM1_CH3
PA9	TIM1_CH2
PA8	TIM1_CH1
PC9	
PC8	
PC7	
PC6	GPIO_Input
PB15	GPIO_Input
PB14	
PB13	GPIO_Output
PB12	GPIO_Output

STM32L476RGTx
LQFP64

Bottom pins (left to right): PA3, VSS, VDD, PA4, PA5, PA6, PA7, PC4, PC5, PB0, PB1, PB2, PB10, PB11, VSS, VDD

Bottom labels: USART_RX, LD2 [green Led], TIM3_CH1, TIM3_CH2, TIM3_CH3, TIM3_CH4, I2C2_SCL, I2C2_SDA

3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
5	PH0-OSC_IN (PH0) *	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	I2C3_SCL	
9	PC1	I/O	I2C3_SDA	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	TIM2_CH1	
15	PA1	I/O	TIM2_CH2	
16	PA2	I/O	USART2_TX	USART_TX
17	PA3	I/O	USART2_RX	USART_RX
18	VSS	Power		
19	VDD	Power		
21	PA5 **	I/O	GPIO_Output	LD2 [green Led]
22	PA6	I/O	TIM3_CH1	
23	PA7	I/O	TIM3_CH2	
26	PB0	I/O	TIM3_CH3	
27	PB1	I/O	TIM3_CH4	
29	PB10	I/O	I2C2_SCL	
30	PB11	I/O	I2C2_SDA	
31	VSS	Power		
32	VDD	Power		
33	PB12 **	I/O	GPIO_Output	
34	PB13 **	I/O	GPIO_Output	
36	PB15 **	I/O	GPIO_Input	
37	PC6 **	I/O	GPIO_Input	
41	PA8	I/O	TIM1_CH1	
42	PA9	I/O	TIM1_CH2	
43	PA10	I/O	TIM1_CH3	
44	PA11	I/O	TIM1_CH4	
46	PA13 (JTMS-SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
48	VDDUSB	Power		
49	PA14 (JTCK-SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 (JTDO-TRACESWO) *	I/O	SYS_JTDO-SWO	SWO
58	PB6	I/O	I2C1_SCL	
59	PB7	I/O	I2C1_SDA	
60	BOOT0	Boot		
61	PB8	I/O	TIM4_CH3	
62	PB9	I/O	TIM4_CH4	
63	VSS	Power		
64	VDD	Power		

** The pin is affected with an I/O function

 * The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration
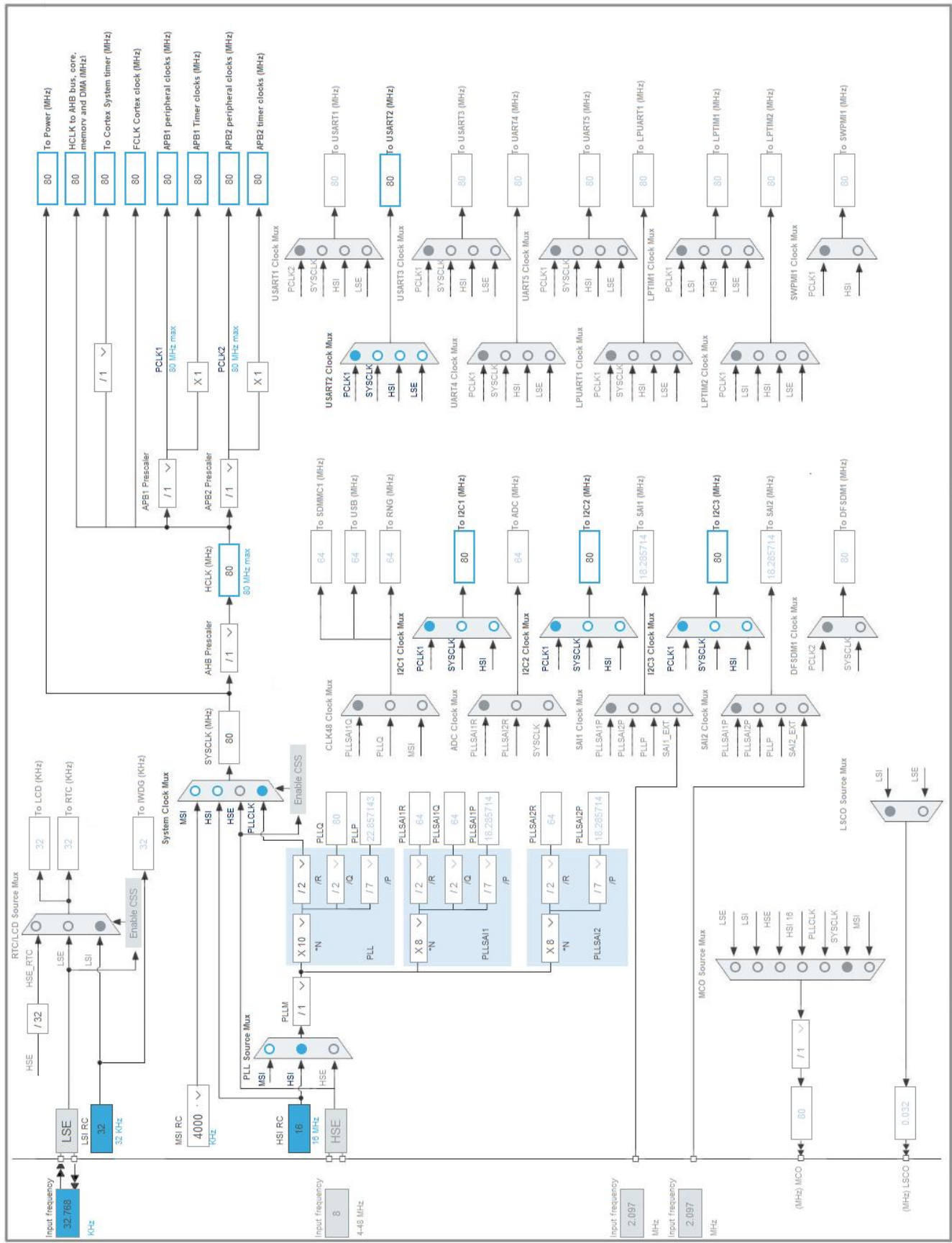
5. Software Project

5.1. Project Settings

Name	Value
Project Name	FInalCode_SeniorDesign
Project Folder	C:\Users\njban\Documents\Nathan\Electronics PDF\Senior Design
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_L4 V1.13.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476RGTx
Datasheet	025976_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. I2C1

I2C: I2C

7.1.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10909CEC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.2. I2C2

I2C: I2C

7.2.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10909CEC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.3. I2C3

I2C: I2C

7.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10909CEC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.4. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.5. SYS

Debug: Serial Wire
Timebase Source: SysTick

7.6. TIM1

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	

- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.7. TIM2

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.8. TIM3

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.9. TIM4

Channel3: PWM Generation CH3
Channel4: PWM Generation CH4
7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.10. USART2

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
I2C3	PC0	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
	PC1	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
RCC	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
SYS	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	USART_TX

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	USART_RX
					*	
Single Mapped Signals	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PB3 (JTDO-TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [green Led]
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PC6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM15 global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM17 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
USART2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		

* User modified value

9. Software Pack Report