ELE 405
HW #2
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1) from rhody.cfg:

```
pdx     3 3 16          { 000001 (0) (1) 0000 (2)      }
pdy     3 3 3 16        { 000010 (0) (1) (2) 0 (3)     }
```

2) Micro-ops:

```
PDX:                                    STATE:
        load I, Rx <= Rx - Ry;          (S3)
        Rx <= I +Rx;                    (S4)
PDY:
        load I, Rx <= Rx + Ry;(S3)
        Rx <= Rx >> 1;                  (S4)
        Rx <= Rz - Rx;                  (S5)
        Rx <= I - Rx;                   (S6)
```

3)

PDX:

0	0	0	0	0	1	Rx	Ry	0	0	0	0	16 bit Immediate

PDY:

0	0	0	0	1	0	Rx	Ry	Rz	0	16 bit Immediate

4) VHDL:

```
elsif (Opcode=PDX) then
        varx0 <= std_logic_vector(signed(register_file(to_integer(unsigned(RX)))) +
signed(register_file(to_integer(unsigned(RY)))));
        varx2 <= (31 downto 16=>I(15)) & std_logic_vector(I);
        CPU_state <= S4;
elsif (Opcode=PDY) then
        vary0 <= std_logic_vector(signed(register_file(to_integer(unsigned(RX)))) +
signed(register_file(to_integer(unsigned(RY)))));
        vary2 <= std_logic_vector(signed(register_file(to_integer(unsigned(RZ)))));
        vary3 <= (31 downto 16=>I(15)) & std_logic_vector(I);
        CPU_state <= S4;


elsif (Opcode=PDX) then
        register_file(to_integer(unsigned(RX))) <= std_logic_vector(signed(varx0) -
signed(varx2));
        CPU_state <= S1;
elsif (Opcode=PDY) then
        vary3 <= std_logic_vector(signed(vary3) - signed(vary2));
        CPU_state <= S5;

elsif (Opcode=PDY) then
        vary0 <= std_logic_vector(signed(vary0) srl 1);
        CPU_state <= S6;

elsif (Opcode=PDY) then
        register_file(to_integer(unsigned(RX))) <= std_logic_vector(signed(vary3) -
signed(vary0));
        CPU_state <= S1;
```

5) See rand3d1.asm

6-8) Code compiled but did not run. Problem found at 1030. Did not revert to S1. Will try tomorow.