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CdS/*p*-Si solar cells made by serigraphy

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CdS/*p*-Si solar cells have been fabricated depositing the CdS layer by serigraphy. Open circuit voltages of 538 mV, short circuit current densities of 32 mA cm^{-2}, fill factors of 0.52, and conversion efficiencies of 8.1% have been measured under 100 mW cm^{-2} (AM1) simulated solar illumination.

Serigraphy, also commonly known as screen printing, is an inexpensive method of low technological complexity which can be used to deposit insulating, resistive, conductive, and semiconducting films to fabricate solid-state devices, including solar cells. The technique is widely used by the semiconductor industry to produce thick-film hybrid circuits and its use in solar cell technology is increasing constantly. Serigraphy is perhaps the simplest method to deposit on large areas the materials of a solar cell. It is frequently used today to deposit front and back contacts, to apply dopants, and to deposit antireflection coatings.[1] Furthermore, it can be extended to the production of integrated solar cell modules using only one process. There have been several reports of CdS/Cu_xS,[2] CdS/CdTe,[3,4] and $CdS/CuInSe_2$,[5] and indium tin oxide (ITO)/Si[6] solar cells produced either partially or entirely by serigraphy. Integrated panels of cell arrays have also been reported by this method.

Other investigators have been working on the development of a CdS on a *p*-Si solar cell which has already shown to be capable of efficiencies in excess of 10%, in spite of the large lattice mismatch between CdS and Si. Different methods for the deposition of the CdS layer on the Si have resulted in efficiencies of 5.5%[7] by single source evaporation, 7%[8] and 9%[9] by electron beam evaporation, 9.5%[10] by coevaporation of CdS and In, and 11.1%[11] by evaporation of sulphur-deficient CdS. The best photovoltaic parameters measured in this last type of cell were open circuit voltages of 510 mV, short circuit current densities of 31 mA cm^{-2}, and fill factors of 0.73. Substitution of the mixed sulfide $Zn_xCd_{1-x}S$ for the CdS has allowed the improvement of the open circuit voltage resulting in cells of 11% efficiency.[9] The first attempt to deposit the CdS by serigraphy on polycrystalline Si has resulted in devices with poor photovoltaic performance: open circuit voltages close to 200 mV, short circuit current densities of 0.15 mA cm^{-2}, and conversion efficiencies under 1% in 2×2 cm devices.[12]

In this letter we report the preliminary results of the first high efficiency CdS/*p*-Si solar cells where the CdS layer is deposited by serigraphy. Our cells were produced depositing a CdS layer onto ⟨100⟩ single-crystal *p*-type silicon wafers of 1.5–2.0 Ω cm nominal resistivity. First, the wafers were fractured into appropriate sizes and were then subjected to a standard cleaning process. Next, the back surfaces were metallized with an air-fireable aluminum paste (ESL 2590) deposited by serigraphy. After a heat treatment to alloy the aluminum to the Si to produce a p^+ layer, the devices were immersed briefly in diluted HF, in order to eliminate the oxide from the front surface. The paste used to print the CdS layer was prepared in-house following a similar procedure as previously reported.[4,5] MARZ grade, 99.999% purity, CdS powder, from MRC, sintered and sifted with a No. 325 Standard Testing Sieve, was mixed with $CdCl_2$ to act as a flux, $InCl_3$ to act as a dopant, and with an appropriate amount of a commercial sharp printing vehicle (ESL 406). Once this paste was printed through a 200 mesh screen, it was dried and sintered for 60 min at 690 °C in a nitrogen ambient. Finally, an unoptimized Ag grid was deposited on the CdS surface by serigraphy of a low firing temperature Ag paste (ESL 590). The thickness of the CdS films deposited to form the various devices varied between 10 and 15 μm and their resistivities, after a heat treatment at 300 °C during 15 min in a vacuum $< 10^{-5}$ Torr, were of the order of 10^{-2} Ω cm.

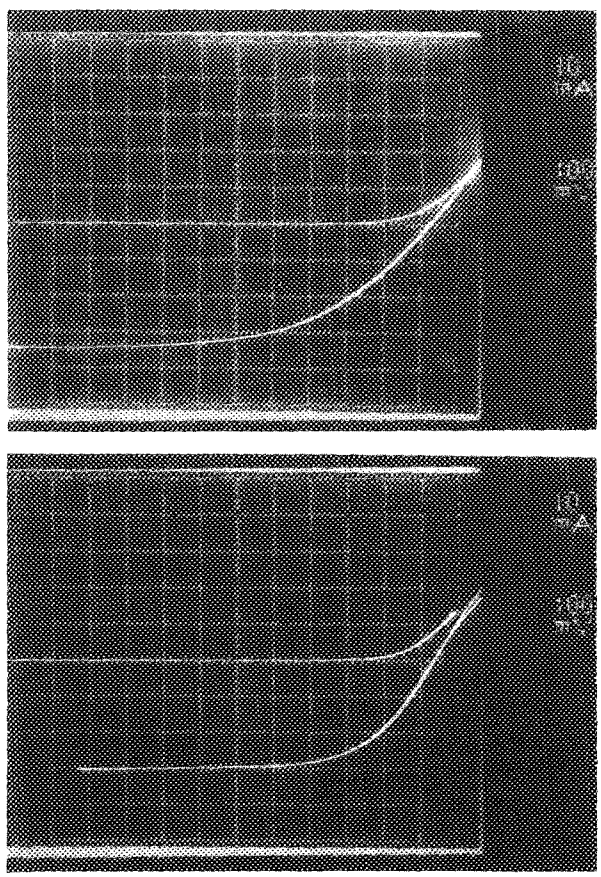

FIG. 1. Two typical dark and illuminated *J-V* characteristics of the CdS/*p*-Si photovoltaic devices fabricated by serigraphic deposition of the CdS layer. The illumination is 100 mW cm^{-2} simulated sunlight (AM1).

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TABLE I. Photovoltaic performance of the CdS/*p*-Si cells fabricated by serigraphy, under 100 mW cm^{-2} (AM1) illumination.

Device No.	J_{sc} (mA cm^{-2})	V_{oc} (mV)	FF (%)	Effic. (%)	Active area (cm^2)
401101	31.4	530	32	5.3	1.234
401102	31.9	538	35	6.0	1.167
401105	31.8	528	39	6.5	1.167
401103	32.0	537	40	6.9	1.134
401104	30.0	534	51	8.1	1.0
401106	30.0	520	52	8.1	0.31

Several devices, with effective areas ranging from 0.310 to 1.234 cm, were fabricated by this method.

The performance of the cells was measured under dark and illuminated conditions. The illumination was simulated sunlight of 100 mW cm^{-2} intensity provided by a Spectrolab Solar Simulator fitted with an AM1 filter and calibrated with a diffused *p/n* junction secondary standard Si cell from NASA-Lewis. The dark and light current voltage (*I-V*) characteristics of typical devices are shown in Fig. 1. Table I presents a comparison of the results obtained from devices with different areas. All the devices present a high series resistance that becomes more apparent as the area of the device increases. For example, device No. 401104 has a series resistance $R_s \approx 3.45\ \Omega$.

As can be seen from the results of Table I, the fill factor (FF) increases with decreasing device area. This is a direct consequence of the higher values of series resistance present in the larger area cells. Figure 2 presents a typical relative spectral response of one of the devices fabricated. The cutoff points correspond to the absorption edges of the CdS frontal layer and of the silicon substrate. Notwithstanding the high interface states density present ($\sim 10^{14}$ cm^{-3}), the interface of this heterojunction does not seem to be a significant recombination path for the photogenerated carriers, as evidenced by the large photocurrent produced, resulting from a high collection of these carriers in the device. Figure 3 shows the light *I-V* characteristic and the power produced by sample cell No. 401104.

Based on the present results it is possible to predict efficiencies higher than 10% with these screen printed cells,

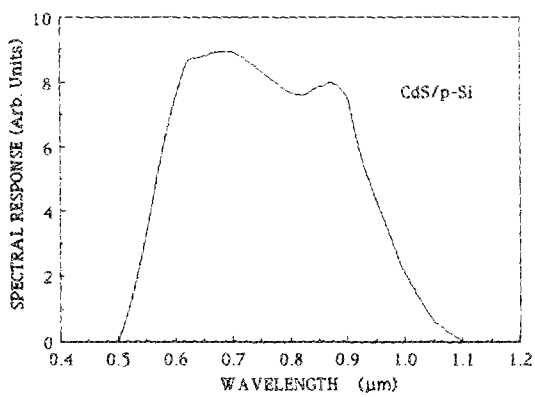

FIG. 2. Spectral response of one of the CdS/*p*-Si devices measured without white light bias.

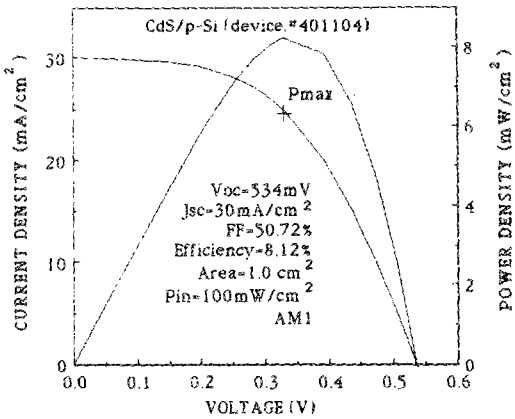

FIG. 3. Illuminated *J-V* characteristics and power generated by device No. 401104 under 100 mW cm^{-2} simulated sunlight (AM1).

once the series resistance is reduced and the frontal surface of the cell is given an antireflection treatment. In spite of the simple serigraphic method used to deposit the CdS, the open circuit voltages of these cells are consistently higher than the values previously reported in similar CdS/*p*-Si cells fabricated by vacuum deposition techniques. The higher values observed are conceivably a consequence of a thin interfacial oxide layer which is likely formed as a result of the serigraphic deposition process used to deposit the CdS, considering the heat treatment given to this layer. Such an oxide would not possibly grow when vacuum deposition is used. In this respect the serigraphic method appears to be advantageous in the formation of a semiconductor-insulator-semiconductor structure instead of a true heterojunction.

In conclusion, CdS/*p*-Si solar cells have been prepared by the inexpensive method of serigraphy. The cells show photovoltaic performance comparable with similar cells fabricated by vacuum deposition techniques. The best conversion efficiencies obtained so far in this preliminary study are 8.1%. However, there seems to be ample room for an overall improvement regarding the device structure itself as well as the window semiconductor. Furthermore, the use of the mixed sulfide $Zn_xCd_{1-x}S$, which could be deposited also by serigraphy, is expected to increase the efficiency by more than 10%.

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