EXPERIMENT NO. 7

Latches and Flip – Flops

Objective:

1) To be able to know what flip-flops are, how they work, and why they are used in many circuits.
2) To be able to construct a flip-flop from NAND gates and from NOR gates.
3) To be able to demonstrate how D and J-K flip-flops react to pulses on their SET, CLEAR, and CLOCK lines
4) To develop digital circuit building and troubleshooting skills

Discussion:

Gates are decision-making logic elements. They can perform the basic functions used in CLCs. But decision-making elements are not enough. A computer also needs memory elements, devices that can store a binary digit.

A **flip – flop** is a device with two stable states; it remains in one of these states until triggered into the other. The **RS latch** is one of the simplest flip-flops. There are two types of RS latch, the NOR and NAND latch. In a NOR latch, when both R and S inputs are low, it gives us the inactive state, the circuit stores or remembers. A low R and a high S represent the set state, while a high R and a low S give the reset state. Finally, a high R and a high S produce a race condition, a limbo or undetermined state.

On the other hand, a NAND latch is the active low version of an RS latch. When both R and S inputs are low, it gives us the limbo or invalid state. If R input is low and S is high then that is the reset state, while S is low and R is high it gives us the set state. When both R and S inputs are high, it gives us the inactive state meaning the circuits stores.

Computers use thousands to millions of flip-flops. To coordinate the overall action, a square-wave signal called the **clock** is sent to each flip-flop. This signal prevents the flip-flops from changing states until the right time. In response to this, clocked latches are introduced. Positive and negative clocking are often called level clocking because the flip-flop responds to the level (high or low) of the clock signal. Level clocking is the simplest way to control flip-flops with a clock.

Race condition is an undesirable condition which may exist in a system when two or more inputs change simultaneously. If the final output depends on which input changes first, a race condition exists. Since the RS flip-flop is susceptible to race condition, the design is modified to eliminate the possibility of a race condition. The result is a new kind of flip-flop known as a D latch. D latches can be made also by NOR and NAND gates. D latch is clocked, meaning while CLK or T input is low, the latch is in the inactive state and the circuit stores or remembers. When T input is high, D input controls the output. A high D input sets the latch, while a low D input resets it. In this case the latch is considered as transparent, meaning that the output follows the value of D while the clock is high. Transparent latches may be all right in some applications but may be a disadvantage in the other way. That is why edge-triggered flip-flops are introduced.

Edge triggering is the changing of output state of a flip-flop on the rising or falling of a clock pulse. Positive-edge triggering is the transition from low to high logic level while negative-edge triggering is the transition from high to low logic level.

The third type of flip-flop is the edge-triggered JK flip-flop. It is considered as the most versatile flip-flop because it can do the function of both RS and D type flip-flop. When it comes to circuit that count, the JK flip-flop is the ideal memory element to use. J & K are the control inputs (they determine what the circuit will do on every positive/negative clock edge) and CLK input is the source of the clock pulse applied to trigger the flip-flop. If J & K are both low, the flip-flop is its inactive state and the flip-flop stores its previous state. When J is low and K is high then output is said to be in reset state. If J is high and K is low the output set. And lastly if both J & K inputs are high the output will be in toggle mode. Toggle means the changing of output to its opposite state in every clock transition. Another way to avoid racing condition is through using a JK master-

slave flip-flop. A master-slave flip-flop is a combination of two clocked latches, the first is called the master and the second is the slave. There are two distinct steps in setting the final output (Q). First, the master is set while the clock is high. Second, the slave is set while the clock is low. This action is sometimes called cocking and triggering. You cock the master during the positive half cycle of the clock, and you trigger the slave during the negative half cycle of the clock.

Material:

- Digital trainer
- Connectors
- Logic Probe
- 1 - 7404 IC
- 1 - 7402 IC
- 1 - 7408 IC
- 3 - 7400 IC
- 1 - 7476 IC

Procedure:

(Before anything else, research and familiarize the pin configurations of all ICs that will be used in this experiment).

1.Construct the circuit shown in Figure 1. Be sure to properly connect the Vcc to pin 14 of 7402 and GND to pin 7. Run the circuit and observe its output. Take note of the proper assignment of output Q and Q. Apply all the possible combinations of RS inputs and tabulate your result in the table assigned as Table1.

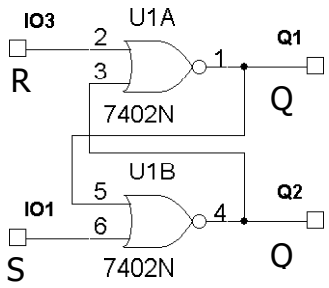


Figure 1

Table 1				
Inputs		Outputs		Output State
X	Y	Q	Q'	
0	0			
0	1			
1	0			
1	1			

What type of flip-flop is Figure 1? _____

2.Construct the circuit in Figure 2. Use 7400 IC for this circuiture. Take note that the setup now of outputs Q and Q is different from Figure 1. Apply what you have done in procedure 1, and record your result in Table2.

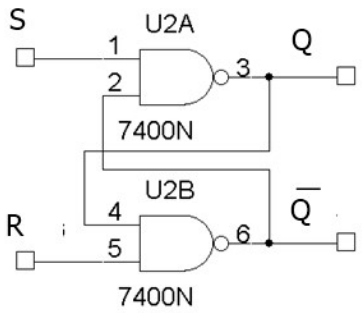
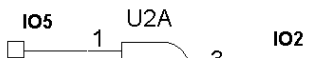


Figure 2

Table 2				
Inputs		Outputs		Output State
X	Y	Q	Q'	
0	0			
0	1			
1	0			
1	1			

What type of flip-flop is Figure 2? _____



3.Construct the circuit shown in Figure 3 and this time you will now use two ICs, the 7408 and 7402. Again be sure to supply the ICs with +5V and GND. Apply all possible combinations of R and S inputs by toggling the CLK input then observe and record the output. Q(t+1) means an output after a logic level transition, in this case consider a positive(low to high) transition.

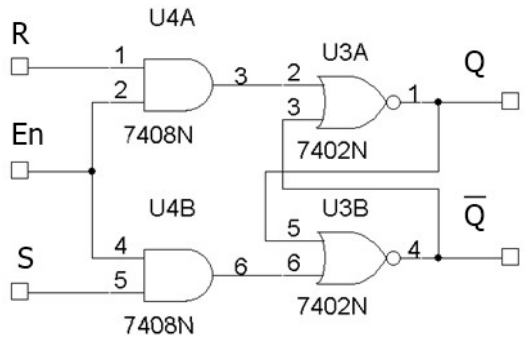


Figure 3

Table 3					
Inputs			Output		Output State
En	S	R	Q	Q(t+1)	

What type of flip-flop is Figure 3?_____

4.Construct the circuit shown in Figure 4 using 7400. Be sure to supply the IC used with +5V and GND.

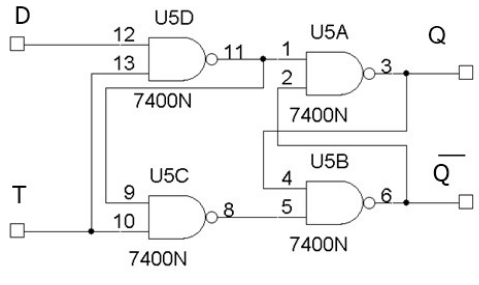


Figure 4

Table 4		
Inputs	Output	Output State

D	T	Q	Q'	

What type of flip-flop is Figure 4? _____

5.Construct the circuit shown in Figure 5 using 7402. Run the circuit and tabulate your result on the table provided.

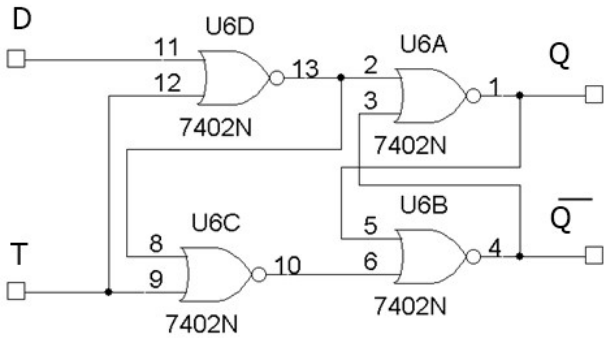


Figure 5

Table 5				
Inputs		Output		Output State
D	T	Q	Q'	

What type of flip-flop is Figure 5? _____

6.Construct the circuit shown in Figure 6 using 7400 and 7404. Run the circuit and tabulate your result in Table6. Always consider output after every leading-edge transition (Q(t+1)).

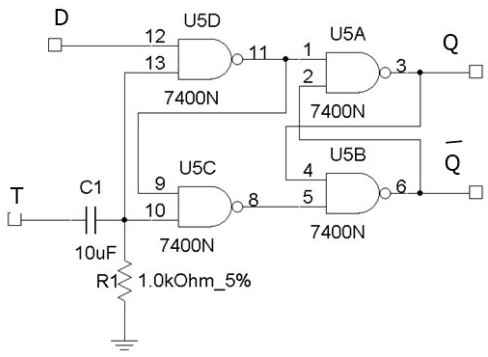


Figure 6

Table 6				
Inputs		Output		Output State
D	T	Q	Q(t+1)	

What type of flip-flop is Figure 6? _____

What is the main difference between Figure 4 and Figure 6 circuit?

_____

_____

_____

7.Implement the circuit shown in Figure 7. Run the circuit and record the result in Table 7. Apply all input combinations as provided in the table and take note each output.

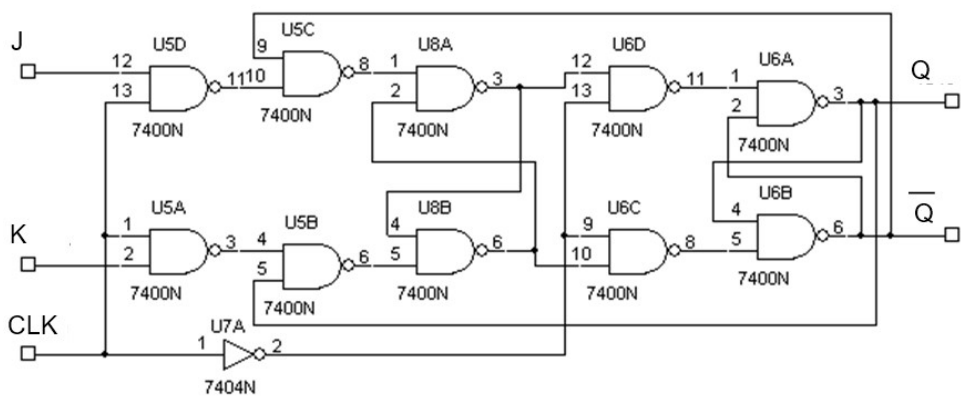


Figure 7

Table 7					
Inputs			Output		Output State
CLK	J	K	Q(T)	Q(T+1)	
↓					
↓					
↓					
↓					

Note : ↓ means a high to low transition

Observation/Conclusion:

EXPERIMENT NO. 8

Designing Counter Circuits

Objective:

1) To understand the operation of an asynchronous counter
2) To implement a mod-10 circuit to an asynchronous counter
3) To develop digital circuit building and troubleshooting skills

Discussion:

A ripple or asynchronous counter is a counter which only the first flip-flop (FF0) is connected to the external clock. The remaining flip-flops are triggered by the falling edge of the output Q of the previous flip-flop. Because of the inherent propagation delay through a flip-flop, the transition of the input clock pulse and a transition of the Q output of a flip-flop can never occur at exactly the same time. Since the flip-flops cannot be triggered simultaneously the counter ends up producing an asynchronous operation. The clock pulse fed into FF0 is rippled through the other counters after the propagation delays (like a ripple on water) hence the name Ripple Counter. The J-K flip-flops are configured in the toggle mode which allows the flip-flop to change states or toggle on every negative going clock pulse.

Figure 1 is an example of a 4-bit ripple counter and therefore it has four flip-flops and 16 different states ($2^4 = 16$). This 4-bit ripple counter is also known as a mod-16 counter for its 16 different states. The mod or modulo number reflects the number of states in the counter.

Another type of counter is the synchronous counter and it eliminates the delay effect that is present with the asynchronous counters. The clock is connected directly to the CLK input of each flip-flop so the outputs change together or synchronously. A synchronous counter does require more circuitry, but in high speed applications the ripple counter delay will be unacceptable.

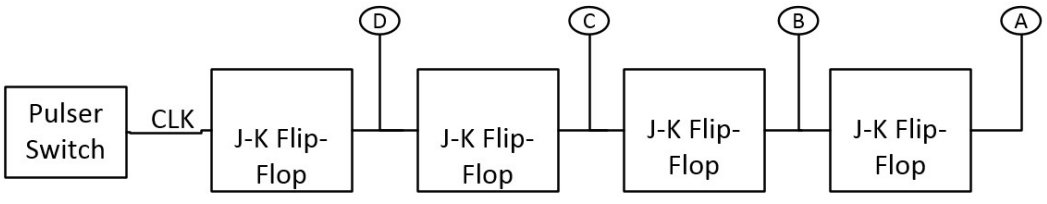


Figure 1

Material:

- Digital trainer
- Connectors
- Logic Probe
- 1 - 7400 IC
- 2 - 7476 IC

Procedure:

1) Build the Asynchronous Up counter circuit as shown in Figure 2.
2) Use the Pulser switches to act as the clock input

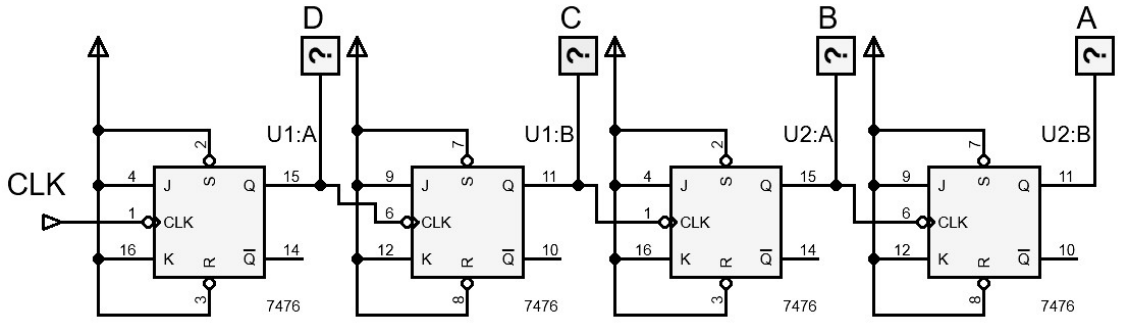


Figure 2 Asynchronous Up Counter

3) Draw the output of the four LEDs for the first 11 clock pulses for the circuit shown in Table 1.

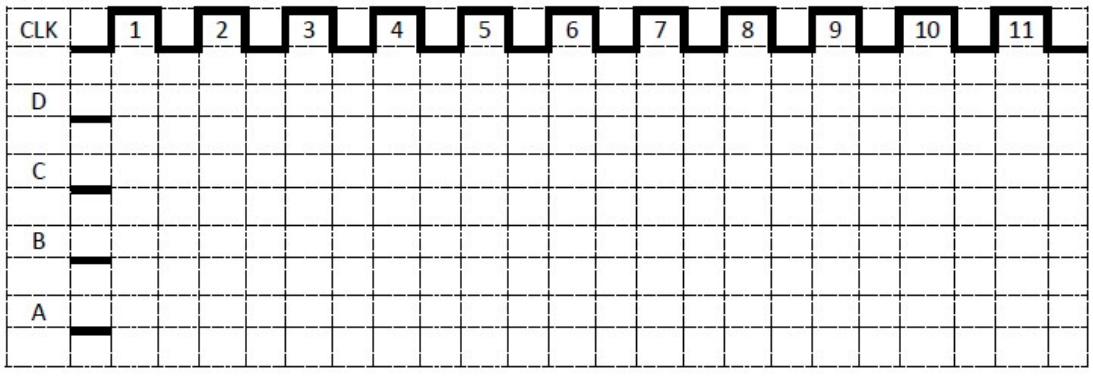


Table 1

4) Modify the circuit to become a down counter.
Draw the circuit here:

5) Draw the output of the four LEDs for the first 11 clock pulses for the circuit shown in Table 2.

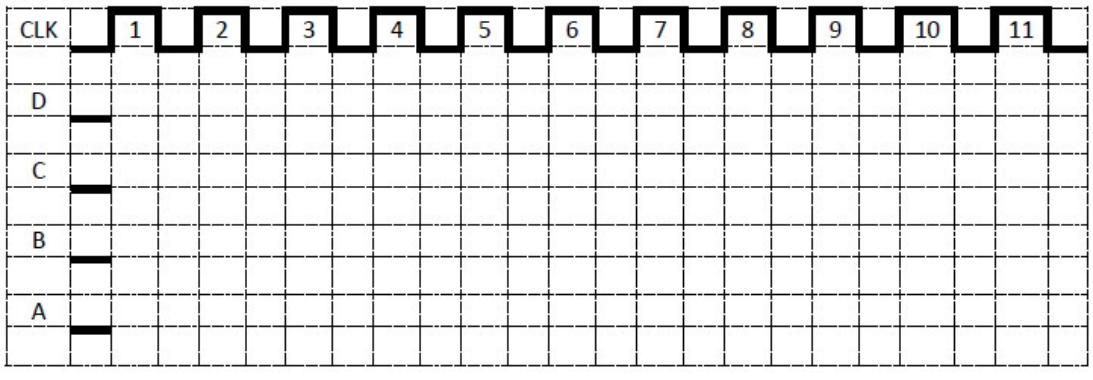


Table 2

6) Modify the circuit back to an Up counter and design the circuitry needed to make the up counter a mod-10 counter with a count sequence that always starts from 0 whenever the circuit is first turned on.
Draw the circuit here:

7) Draw the output of the four LEDs for the first 11 clock pulses for the circuit shown in Table 3.

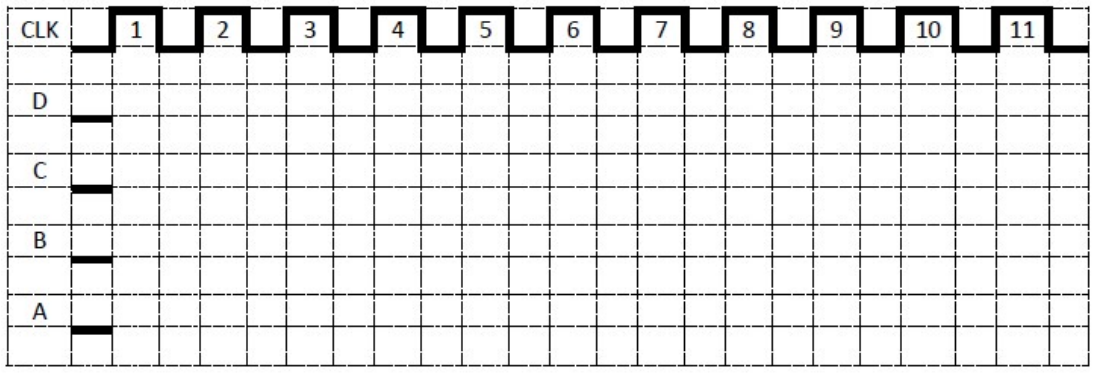


Table 3

Observation/Conclusion: