# Experiment 7

Nitish Kumar Thakur
21531010

14 september, 2021

## 1 Objective

Design and fabricate a frequency multiplier circuit using PLL IC-565

## 2 Components and Equipment Required

IC-565*IC-7474 *DSO *Power supply (variable)*connecting wire *Breadboard *probes *Resistance*Function generator

## 3 Theory

### 3.1 Phase lock loop

Phase-locked loop is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. PLLs operate by producing an oscillator frequency to match the frequency of an input signal. In this locked condition, any slight change in the input signal first appears as a change in phase between the input signal and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match the input signal. The locking-onto-a-phase relationship between the input signal and the local oscillator accounts for the name phase-locked loop. if we analyse the figure there is basically 4 Block.

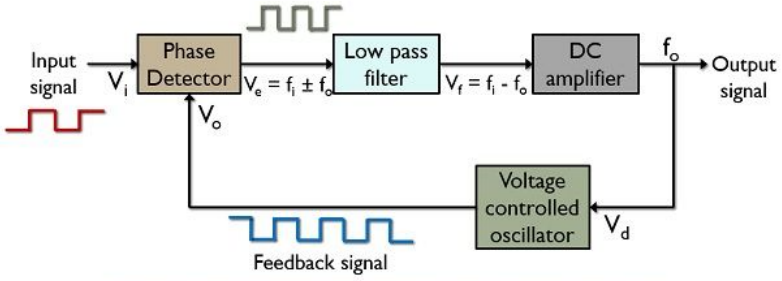



Figure 1: PLL

#### 3.1.1 Phase Detector

A phase detector is nothing but a comparator.It performs a comparison of two frequency component fed at its input and generates a dc voltage.This generated voltage is proportional to the difference in phase of the two frequencies.

#### 3.1.2 Low pass filter

The output of the phase detector is provided to a low pass filter.It eliminates the high-frequency component and noise from the output of the comparator.This low-frequency dc voltage signal is then provided to a dc amplifier which amplifies the signal level.This amplified signal is then provided to the VCO

### 3.1.3 Voltage Controlled Oscillator

Voltage-controlled oscillator is electronic oscillator the work of VCO is when we give variable voltage in VCO it generates varying frequency curve(Linear).This thing shown in below Figure The output of LPF acts as a control signal to the VCO.The VCO generates a dc signal, the amplitude of which is proportional to the amplitude of output of LPF.Here the adjustment in the output frequency of VCO is made until it shows equivalency with the input signal frequency.

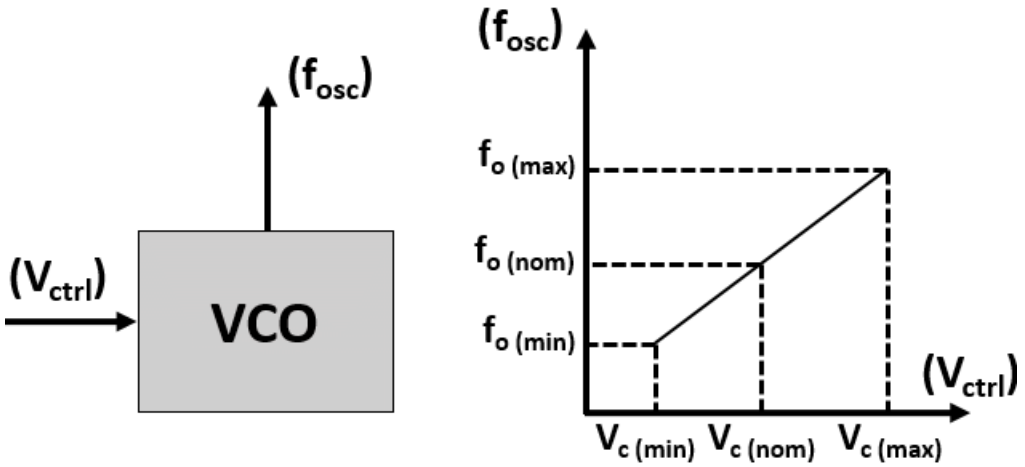



Figure 2: Voltage-controlled oscillator

### 3.1.4 Dc Amplifier

Amount of gain we getting is very-very less so we use DC amplifier.

Phase Lock Loop basically work in two mode

1.Capture range

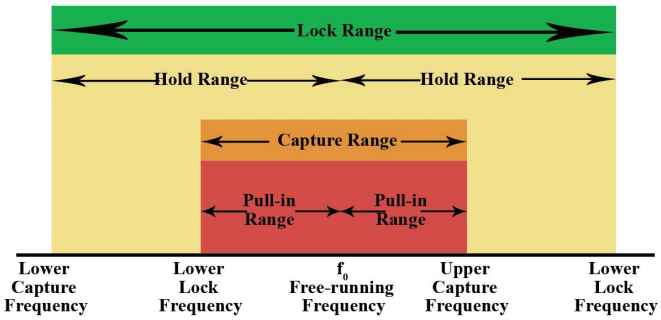
2.Lock range

**1.Capture range**

The process of adjusting the VCO frequency and holding it to incoming signals frequency is called capture.The minimum and maximum input frequencies to which the loop can move the VCO as it captures an input signal is called the capture range.The segments of the capture range above and below fo are called the pull-in range.The pull-in ranges are not necessarily symmetrical.

**2.Lock range**

If the input frequency has moved so far that any further change will cause the control signal to move back and the VCO frequency away from the input signal.The loop is no longer locked and the input and VCO frequencies are no longer the same.The range of input frequencies between the value at which the loop is locked is called the loop's lock range.The lock range above and below f0 are called the loop's hold ranges.The lock range is not always centered on f0




(a) Capture range/ Lock range

Free-running frequency of VCO:

$$f_O \simeq \frac{1.2}{4R_1C_1} \text{ in Hz}$$

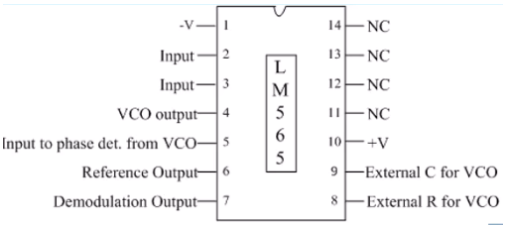
Lock range: $f_L = \pm \frac{8f_O}{V_{CC}}$ in Hz

Capture range: $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

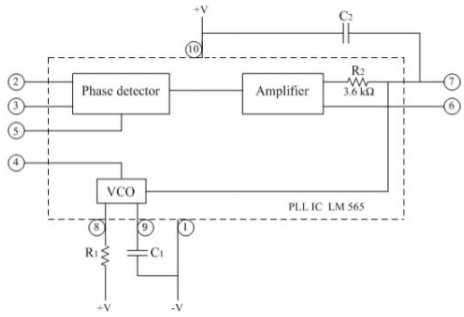
where $\tau = (3.6 \times 10^3) \times C_2$

(b) Free running Frequency of VCO

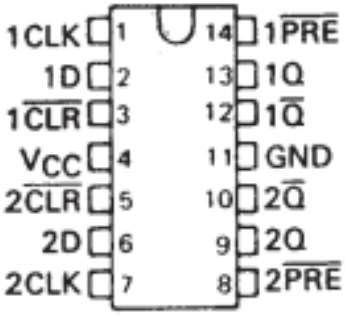
## 3.2 IC Pin diagram/ block diagram



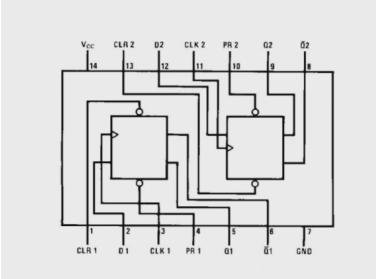

(a) IC LM-565 Pin diagram




(b) Block diagram of IC LM-565




(a) IC 7474 Pin diagram



(b) Block diagram of IC 7474

## 3.3 Frequency division

When we connect D flip flop complement-Q output to input that means D then output Q is mainly divide the frequency of clock f/2 .it is shown in below figure.

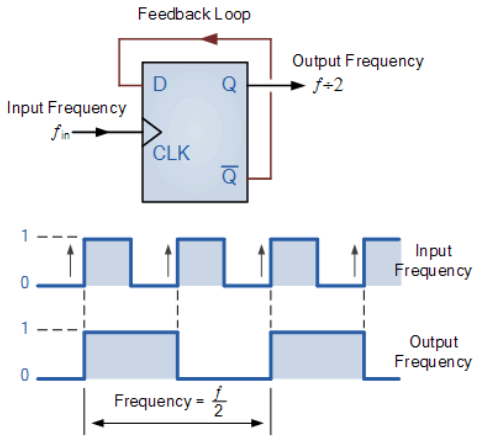
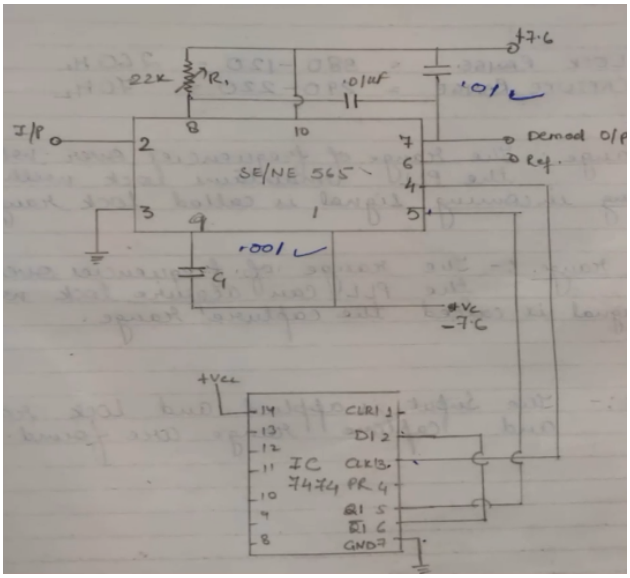



Figure 6: Frequency division circuit

## 3.4 Frequency multiplier circuit

if we analyse the Block diagram of frequency multiplier,a divide by N network is inserted between the VCO output (pin 4) and the phase comparator input (pin 5). Since the output of the divider is locked to the

input frequency fi, the VCO is actually running at a multiple of the input frequency. Therefore, in the locked state, the VCO output frequency fo is given by,




(a) Circuit diagram of freq. multiplier

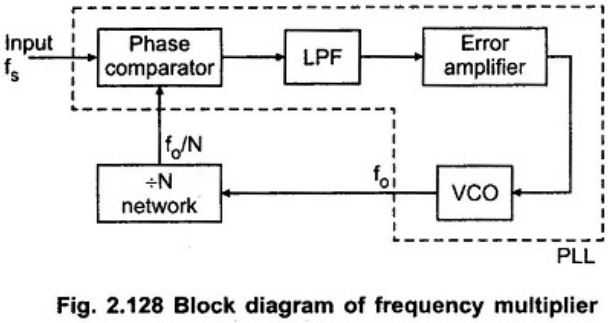



**Fig. 2.128 Block diagram of frequency multiplier**

(b) Block diagram of Frequency multiplier

# 4 Observation/Results

When we introduce the frequency divider(IC-7474),in between phase detector and vco,what happens, the frequency from vco divided by N times(f/N).so when these frequency pass through phase detector it generates some error signal again these signal comeback to input of VCO,so VCO bump up these signal by N times.so signal even after passing through Divider ckt the frequency matches with phase detector.

output of vco-pin4——pin-3 of IC7474

Output of 7474-pin5——pin-5 of IC865

The free running frequency =37Khz

At 14 khz it lock the signal after this we increases the signal slowly and see up which point it lock.,this things happen at Fl2=43Khz; afte this we decrease the frequency and see from which point again capture the signal,the point is fc2=39Khz,and again slowly we decreases and upto which point it is so fc1=21khz.

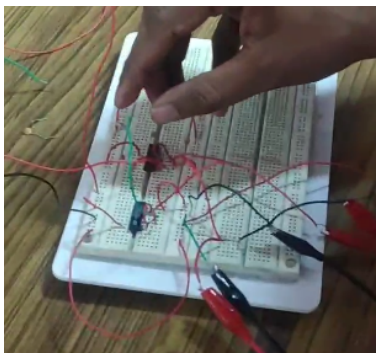
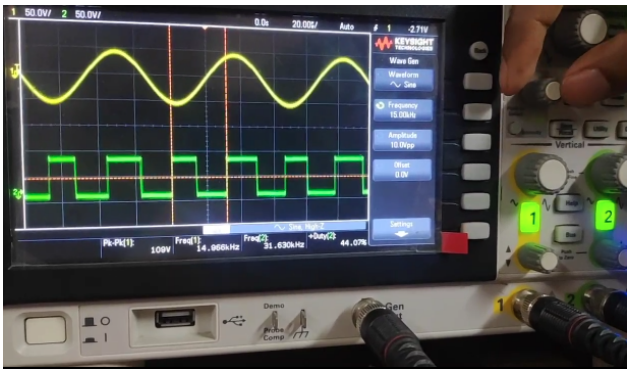


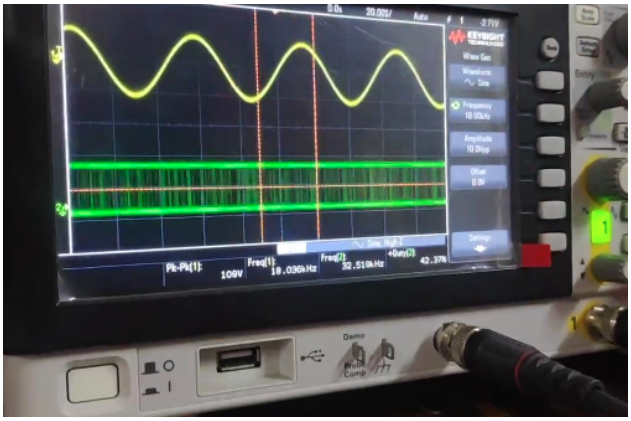
Figure 8: Circuit on Breadboard

When we gave input frequency f=15khz and output frequency is=31.827Khz in figure-11.

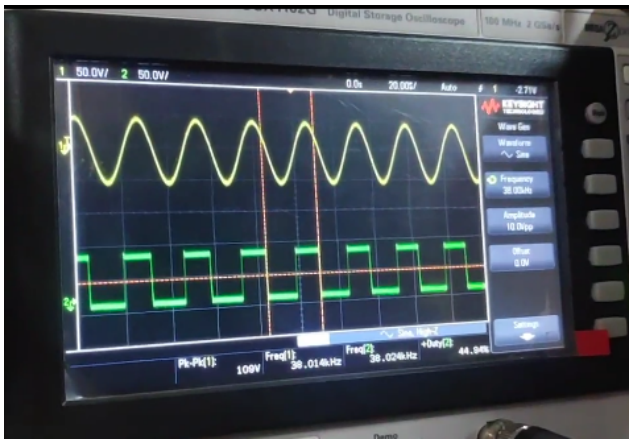


(a) Lock point-1

(b) Lock point-2



(a) Capture point-1



(b) capture point-2

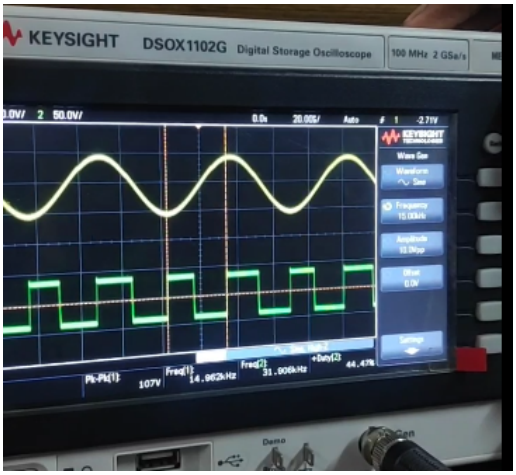



Figure 11: Frequency Multiplied By 2

# 5 Conclusion/Sources of error

So we perform experiment where when we gave input frequency i.e f=15 khz and get output frequency=31.827 khz.here onw thing we observe not exactlly double of input may be due to some parasitic capacitance of ic.

also we should care of one thing,The multiplied frequency range should be within the capture range.so the loop lock on it,otherwise if we apply anything other range,it should not get multiplied,and PLL keep running at free frequency which is 37khz.