

Experiment 5

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1 Objective

- 1.Determine the lock range and capture range of the PLL IC-565
- 2.Demodulate FM signal using the PLL IC-565

2 Components and Equipment Required

IC-565 PLL IC*IC-8038 *DSO *Power supply (variable)*connecting wire *Breadboard *probes *Resistance *DSO *Function generator

3 Theory

3.1 Phase lock loop

Phase-locked loop is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. PLLs operate by producing an oscillator frequency to match the frequency of an input signal. In this locked condition, any slight change in the input signal first appears as a change in phase between the input signal and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match the input signal. The locking-onto-a-phase relationship between the input signal and the local oscillator accounts for the name phase-locked loop. if we analyse the figure there is basically 4 Block.

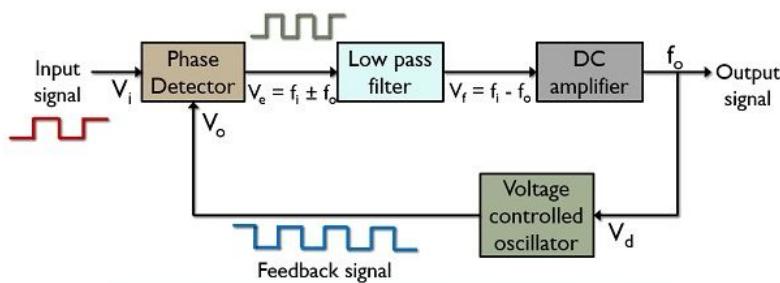


Figure 1: PLL

3.1.1 Phase Detector

A phase detector is nothing but a comparator. It performs a comparison of two frequency component fed at its input and generates a dc voltage. This generated voltage is proportional to the difference in phase of the two frequencies.

3.1.2 Low pass filter

The output of the phase detector is provided to a low pass filter. It eliminates the high-frequency component and noise from the output of the comparator. This low-frequency dc voltage signal is then provided to a dc amplifier which amplifies the signal level. This amplified signal is then provided to the VCO.

3.1.3 Voltage Controlled Oscillator

Voltage-controlled oscillator is electronic oscillator the work of VCO is when we give variable voltage in VCO it generates varying frequency curve(Linear). This thing shown in below Figure The output of LPF acts as a control signal to the VCO. The VCO generates a dc signal, the amplitude of which is proportional to the amplitude of output of LPF. Here the adjustment in the output frequency of VCO is made until it shows equivalency with the input signal frequency.

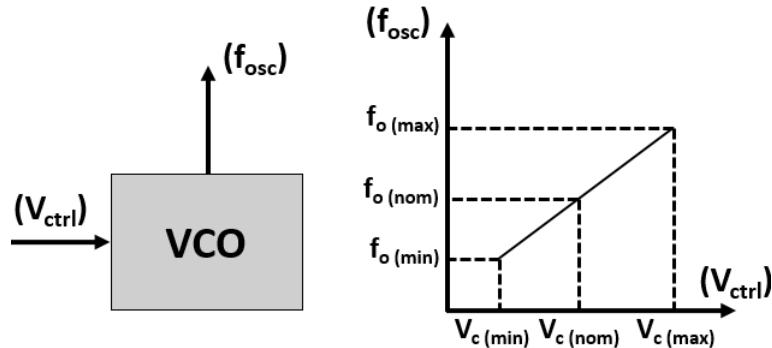


Figure 2: Voltage-controlled oscillator

3.1.4 Dc Amplifier

Amount of gain we getting is very-very less so we use DC amplifier.

Phase Lock Loop basically work in two mode

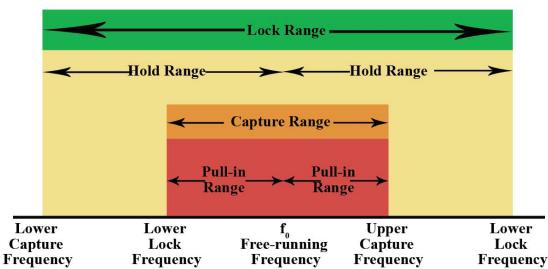
1. Capture range
2. Lock range

1. Capture range

The process of adjusting the VCO frequency and holding it to incoming signals frequency is called capture. The minimum and maximum input frequencies to which the loop can move the VCO as it captures an input signal is called the capture range. The segments of the capture range above and below f_0 are called the pull-in range. The pull-in ranges are not necessarily symmetrical.

2. Lock range

If the input frequency has moved so far that any further change will cause the control signal to move back and the VCO frequency away from the input signal. The loop is no longer locked and the input and VCO frequencies are no longer the same. The range of input frequencies between the value at which the loop is locked is called the loop's lock range. The lock range above and below f_0 are called the loop's hold ranges. The lock range is not always centered on f_0 .



(a) Capture range/ Lock range

Free-running frequency of VCO:

$$f_0 \approx \frac{1.2}{4R_1C_1} \text{ in Hz}$$

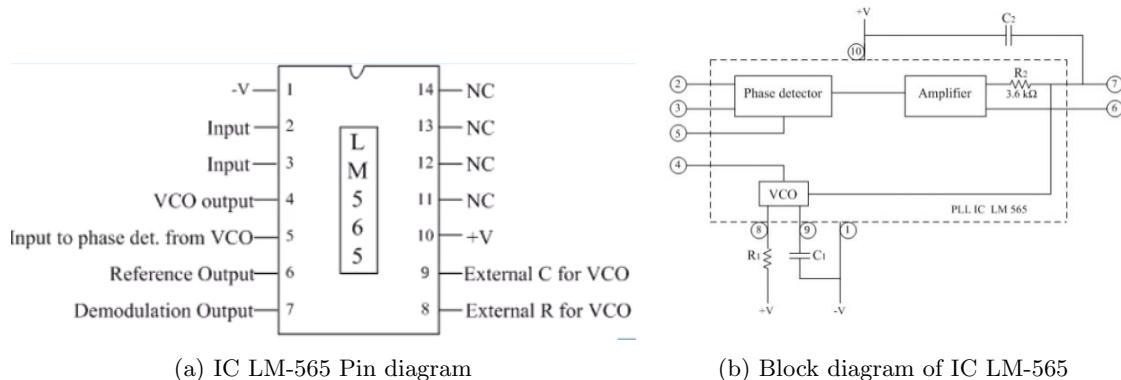
$$\text{Lock range: } f_L = \pm \frac{8f_0}{V_{CC}} \text{ in Hz}$$

$$\text{Capture range: } f_C \approx \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$$

$$\text{where } \tau = (3.6 \times 10^3) \times C_2$$

(b) Free running Frequency of VCO calculatio

3.2 IC LM565 Pin diagram/ block diagram



3.3 Frequency Demodulation

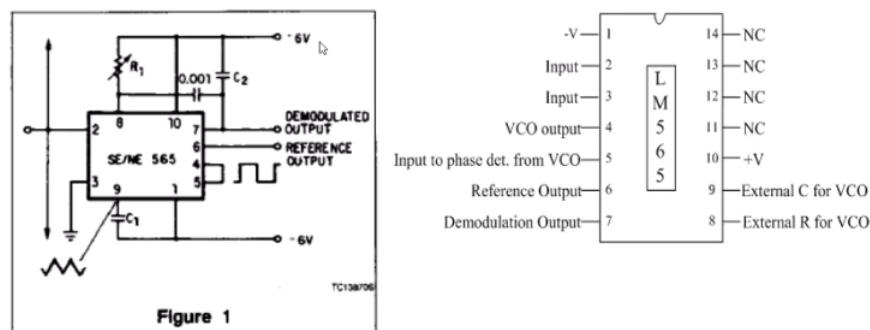


Figure 5: Frequency Demodulation

Circuit Diagram

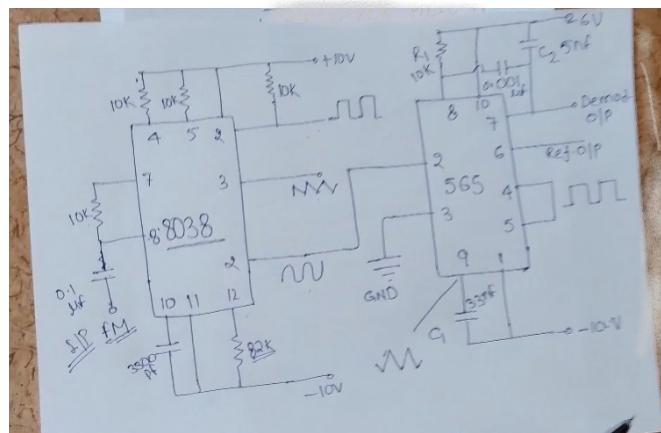
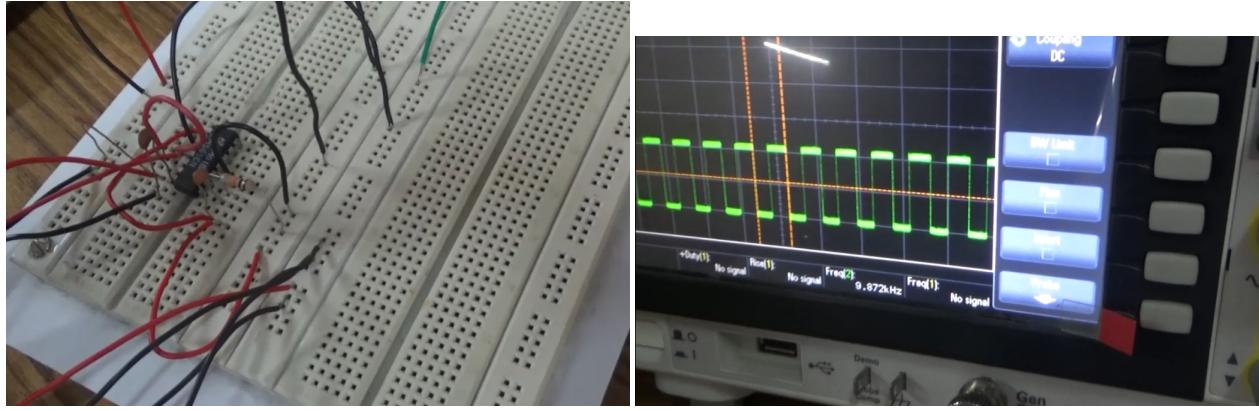


Figure 6: Circuit diagram of demodulation

4 Observation/Results

4.1 Free Running frequency

Output frequency in case of free running VCO is 9.954Khz. This frequency almost equal to incoming signal. After this our aim to select proper value of R and C



(a) Circuit on BreadBoard

(b) Free running Frequency

Free-running frequency of VCO:

$$f_0 \approx \frac{1.2}{4R_1C_1} \text{ in Hz}$$

Lock range: $f_L = \pm \frac{8f_0}{V_{CC}}$ in Hz

Capture range: $f_C \approx \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

Figure 8: Equation for calculation of R and C

$R_1=10\text{Kohm}$ (9.954Kohm By multimeter), $C_1=3.3\text{ nF}$, $C_2=5\text{nF}$

if $R=10\text{Kohm}$ - $f_0=9.09\text{Khz}$

$R=9.54\text{Khz}$ for $f_0=9.529\text{Khz}$

After This we give input signal.frequency= 6.5Khz and see what's the vco output.VCO output frequency is $f=6.499\text{Khz}$,in lower figure.



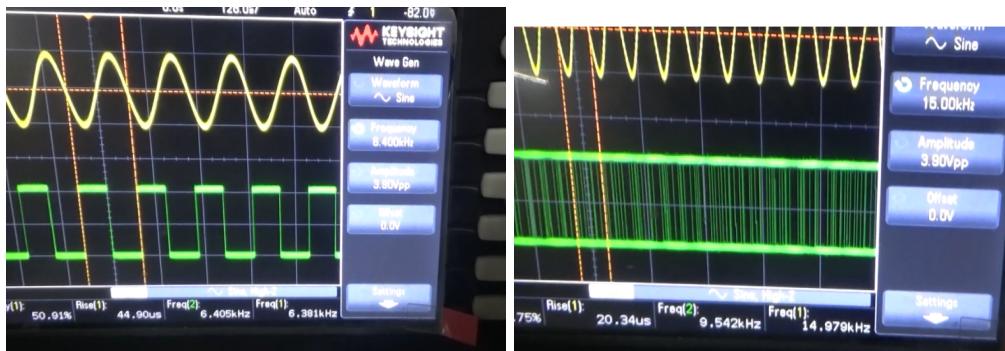
Figure 9: Input at pin-2/and VCO output

After this we want to see in which range it is phase lock.so we first increase the frequency slowly and see where it is lock.it is known forward locking range.

Now we go for backward direction.Backward lock range start at $f=14\text{ Khz}$.Backward lock range stop at $f=6.2\text{Khz}$

so we take common data for capture range i.e 6.3khz-14khz.

and Lock range is 6.2khz-14khz. if we calculate theoretically then
 $f_l=7.962\text{khz}$



(a) forward lock range start at f=6.3Khz

(b) lock range end at f=14.9Khz

$F_c=8.39\text{Khz}$

so we use pll in this range to demodulate our frquency modulated signal.

VCO characteristic

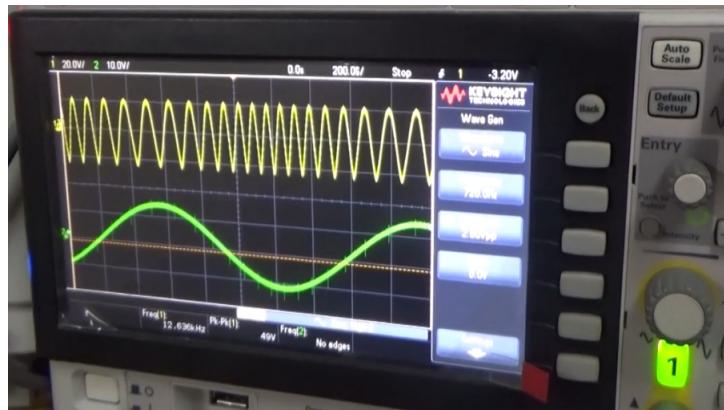


Figure 11: Modulated signal output

This is final output after demodulation

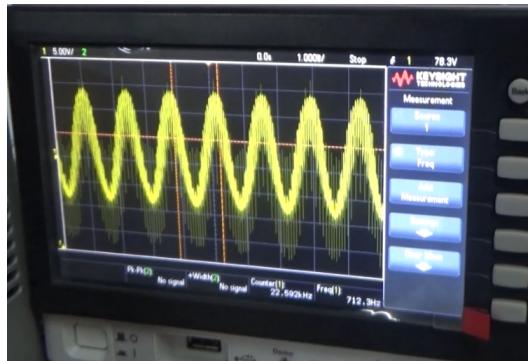


Figure 12: Final demodulated signal

5 Conclusion/Sources of error

If we observe output that means demodulated signal we did not get perfect output like input sinusoidal.because PLL output is square waveform which is not perfect(Gibb's phenomena)

when we observe the demodulated signal frequency it is 712.3 Hz.which is nearer to original Message signal

also when we calculate theoretically Lock range and capture range we found lock range is less then capture range.but we know lock range always higher then capture range.this problem i think due to problem with resistor and capacitor,which is not perfect.