COM2039 Parallel Programming using NVIDIAs CUDA

Content

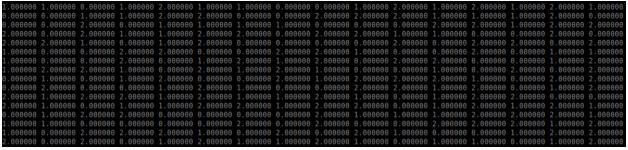
Part 1: Matrix Multiplication	2
Step 1 [5 marks]: Examples of matrices from matrix multiplication program that use global memory	
Step 2 [3 marks]: Added timing event for lab class 3 and 2	3
Step 3 [8 marks]: Progressively scaling the matrix size	3
Step 4 [9 marks]: Results of the experiment	4
Part 2: Reduce	5
Step 1 [15 marks]: Implementation of reduce	5
Step 2 [5 marks]: record and plot set of timings: Execution Times (ms) vs Input Arra	-
Step 3 [5 marks]: Why we repeatedly partition the array into two halves	15
Part 3: Scan	15
Step 1 [15 marks]: Implementation of Hillis and Steele Scan which uses multiple blo in order to handle large input arrays	
Step 2 [5 marks]: Execution times recorded as input array size increases	18
Step 3 [5 marks]: Two proposition in improve performance of the Lab implementation	n18
Part 4: Histogram	20
Step 1 [10 marks]: Implementation of Histogram using kernel from Lecture 11	20
Step 2 [10 marks]: Modified Implementation	22
Step 3 [5 marks]: Differences between the two implementations	24
References:	25

I confirm that this report is my own work and any work that has been used have been referenced appropriately.

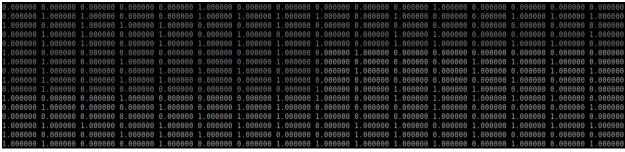
Signed by: Nithesh Koneswaran

Part 1: Matrix Multiplication

Step 1 [5 marks]: Examples of matrices from matrix multiplication program that uses global memory Input A



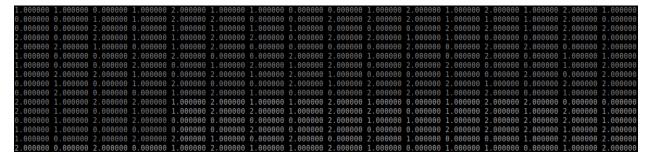
Input B



Input C



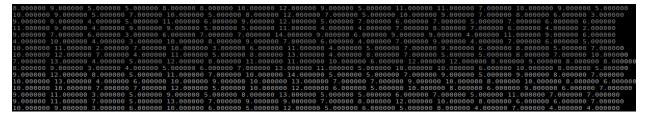
Examples of matrices from matrix multiplication program that uses shared memory. Input A



Input B



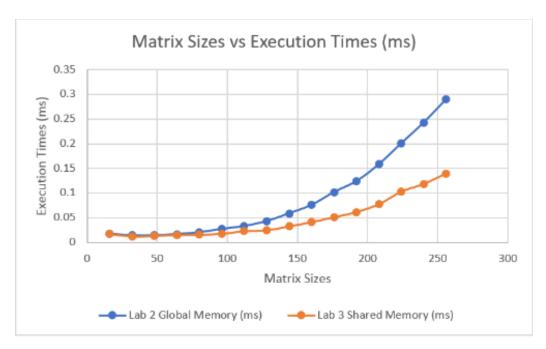
Input C



Step 2 [3 marks]: Added timing event for lab class 3 and 2

Step 3 [8 marks]: Progressively scaling the matrix size

Matrix Size	Lab 2 Global Memory (ms)	Lab 3 Shared Memory (ms)
16	0.017376	0.016992
32	0.014144	0.012288
48	0.014336	0.01312
64	0.016704	0.01536
80	0.02048	0.015616
96	0.027104	0.017728
112	0.032992	0.022944
128	0.043008	0.02496
144	0.058784	0.032512
160	0.075872	0.04112
176	0.101888	0.0512
192	0.124032	0.061568
208	0.158368	0.077568
224	0.200896	0.102784
240	0.24288	0.118432
256	0.290176	0.139616
512	2.349824	1.03744
1024	19.199137	8.708096
2048	153.854813	68.687965
4096	1249.886719	419.366058
8192	13592.4707	3572.080566



Step 4 [9 marks]: Results of the experiment

Note: I tested the execution time for matrices of size 16 to 256 with intervals of 16. In the graph above I ignored matrices with size greater than 256 since the trend was quite clear, the trend being that the program that utilized shared memory had a faster execution time than the program that only used global memory.

Hypothesis: I theorize that as the sizes of the matrices increases the program that uses shared memory would have a faster execution time than the program that uses global memory. This is expected since shared memory (comparable to L1 Cache in a CPU) sits on the streaming multiprocessors providing short access times compared to global memory which sits on the device, off the chip, providing longer access times. Upon further research [1] I found that an 'SRAM cell' (Shared memory) can be clocked much faster than 'DRAM cell' (Global memory) which further backs up my hypothesis that shared memory would perform faster than global memory. A limitation of this experiment is that memory is not infinite, in the Otter labs the computers running GTX 1050ti have 4GB of global memory and 49152 bytes of shared memory, because of this we might find that either shared memory or global memory will run out if the matrix set size exceeds a large number.

The output data, shown in step 3, clearly supports my hypothesis, if we look at execution times for matrices with size 8192 we find that shared memory (3672.08056ms) has a 73.72% decrease in execution time compared to Global memory (13592.4707ms). We can clearly see that Global Memory has a slower execution time compared to Shared Memory, this is because of the physical architecture of the GPU as explained in the hypothesis.

I also noticed that for both programs the execution times seem to get quicker between the range of matrix sizes of 16 to 64. Upon research I ultimately concluded that it may have gone faster due to coalescing memory access which can boost access speeds, an alternative conclusion is that it could simply be an anomaly on the results since the execution times in the labs can be quite different for each execution of the program, there should be a period to wait before executing again. Nevertheless, upon further testing the pattern remained the same.

Part 2: Reduce

Step 1 [15 marks]: Implementation of reduce

```
#include <iostream>
#include <stdiio.h>
#include <stdiio.h

#include <stdiio.h

#include <stdiio.h>
#include <stdiio.h>
#include <stdiio.h

#include <std>include <std>include <std>include <std>include <std include <std in
```

```
shared int mem[BLOCK SIZE/2];
  mem[local index] += mem[local index + halfOfBlockSize];
```

```
d out[blockIdx.x] = mem[local index];
```

```
cudaFree(d in);
```

Program Reduce done on GPU:

```
#include <iostream>
   #include <numeric>
  #include <stdio.h>
4 #include <stdlib.h>
5 #include <math.h>
6 #define ARRAY SIZE 64
     mem[local index] += mem[local index + 16];
     mem[local index] += mem[local index + 8];
     mem[local index] += mem[local index + 4];
     int qlobal index = threadIdx.x + (blockDim.x*2)* blockIdx.x; // Global ID
     int local index = threadIdx.x; // Local ID
```

```
mem[local_index] = d_in[global_index]+d_in[global_index+blockDim.x];
for (unsigned int halfOfBlockSize = blockDim.x/2; halfOfBlockSize >> 32; halfOfBlockSize >>= 1)
  if (local_index < halfOfBlockSize)</pre>
    mem[local_index] += mem[local_index + halfOfBlockSize];
if (local_index<32)</pre>
  warpReduce(mem, local_index);
```

```
if (local_index < halfOfBlockSize)</pre>
   mem[local_index] += mem[local_index + halfOfBlockSize];
 warpReduce(mem, local_index);
if (local_index == 0)
const int SECOND_ARRAY_SIZE = ARRAY_SIZE/BLOCK_SIZE;
```

```
/* Allocates memory for d_in in the GPU */

cudaMalloc((void**) &d_in, INPUT_SIZE);

/* Copies the array from HOST (cpu) to DEVICE (gpu) */

cudaMemcpy(d_in, h_in, INPUT_SIZE, cudaMemcpyHostToDevice);

/* Allocates memory for d_out in the GPU */

cudaMalloc((void**) &d_out, OUTPUT_SIZE);

/* Number of threads per block, we divided it by 2 such that... */

dim3 threadsPerBlock(BLOCK_SIZE/2);

/* Number of blocks*/

dim3 blocks(SECOND_ARRAY_SIZE);

/* Start the timer */

cudaEventRecord(start);

/* Launching kernal with 16 block and 16 threads per block */

shared reduce kernal<<<<br/>
shared reduce kernal<<<<br/>
shared reduce kernal<<<<br/>
shared reduce kernal<<<<br/>
shared reduce kernal<<</br>
```

```
final_reduce_kernal<<<allocatedBlockSize, threadsPerBlock>>>(final_d_out, final_d_in);

cudaDeviceSynchronize();

cudaMemcpy(final_h_out, final_d_out, OUTPUT_SIZE, cudaMemcpyDeviceToHost);

/* Final reduced ve_ue */

printf("Final reduction: %f\n", final_h_out[0]);

/* Outputs the results

for (int n = 0; n < SECOND_ARRAY_SIZE; n++) {
    printf("%f ", final_h_out[n]);

} */

cudaEventRecord(stop);

cudaEventSynchronize(stop);

float milliseconds = 0;

cudaEventElapsedTime(&milliseconds, start, stop);
    printf("Elapsed time was: %f milliseconds \n", milliseconds);

/* Frees the variables */
    cudaFree(d_out);
    cudaFree(final_d_in);
    cudaFree(final_d_in);
    cudaFree(final_d_in);
    cudaFree(final_d_out);

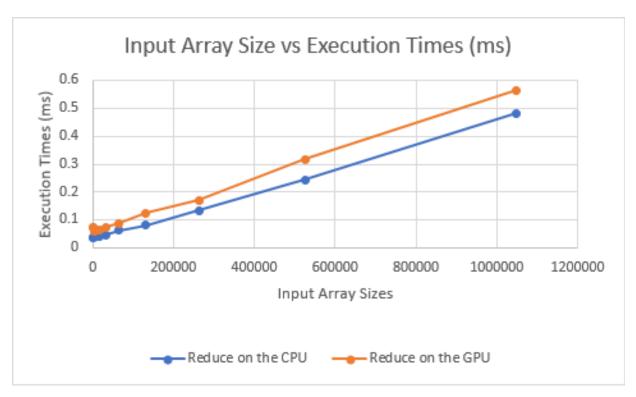
cudaFree(final_d_out);

cudaFree(final_d_out);

cudaFree(final_d_out);</pre>
```

Step 2 [5 marks]: record and plot set of timings: Execution Times (ms) vs Input Array Size

Input Array Sizes	Reduce on the CPU	Reduce on the GPU
1024	0.03904	0.07248
2048	0.0392	0.07264
4096	0.040704	0.062272
8192	0.042176	0.065312
16384	0.043776	0.065696
32768	0.04832	0.074976
65536	0.06416	0.089664
131072	0.082592	0.125632
262144	0.134048	0.171744
524288	0.244864	0.318368
1048576	0.48192	0.56544
2097152	Segmentation Fault	Segmentation Fault

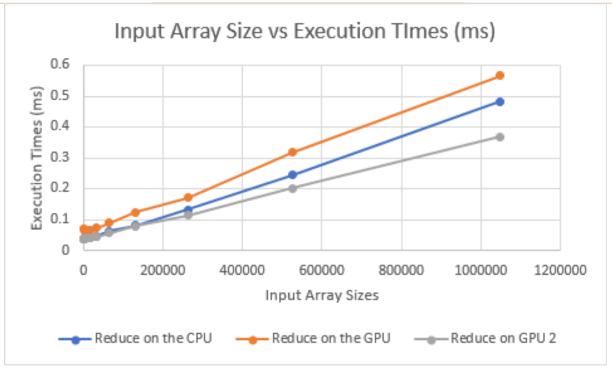


Note: I tested the execution time for Input Array Sizes from 1024 to 1048576 with intervals double the previous values. At array size 2097152 a segmentation Fault error occurred which signified that the GPU most likely ran out of memory. Therefore, I stopped at that point for recording results.

The data gathered from the experiment strongly highlights that the final reduction done on the CPU is faster than the final reduction done on the GPU. This rejects my hypothesis as I had initially thought that the GPU would be faster. This is because, in my implementation my program does a further reduction and then atomically adds the final values together. I thought that by repeating the reduction process we effectively managed to reduce the final number of elements in the array to add together. The results clearly disprove my theory, I believe the reason is because there is bottleneck along the PCI express bus which carries data between the GPU and CPU. The bottleneck being that there is an increase in overhead from sending data back and forth to the GPU, this bottleneck most likely explains the reason

why we are seeing an increase in execution time with the GPU. If this was the case, then perhaps just having the atomic add in the first kernel and not having to call the second kernel will optimize the GPU code further. See below for the results:

Input Array Sizes	Reduce on the CPU	Reduce on the GPU	Reduce on GPU 2
1024	0.03904	0.07248	0.038272
2048	0.0392	0.07264	0.038912
4096	0.040704	0.062272	0.040192
8192	0.042176	0.065312	0.04208
16384	0.043776	0.065696	0.042752
32768	0.04832	0.074976	0.045728
65536	0.06416	0.089664	0.57824
131072	0.082592	0.125632	0.079424
262144	0.134048	0.171744	0.11472
524288	0.244864	0.318368	0.202016
1048576	0.48192	0.56544	0.3688



Here I have updated the data with my third program "Reduce on GPU 2". This program will only call one kernel. The kernel will then lastly execute the atomicAdd function to calculate the final reduced value. Atomic operations are used to prevent race conditions to perform a certain operation, to prevent these race conditions, an operation is executed one thread at a time, essentially making the operation serial and not parallel. Nvidia's atomic operations is optimized and quite fast for variables stored in shared memory but slow in device global memory. Since we are dealing with shared memory atomic operations in shared memory may have contributed to a faster overall execution time compared to the final reduction done on the CPU.

Step 3 [5 marks]: Why we repeatedly partition the array into two halves If we implement reduce with the pattern mentioned in lecture 10 we introduce thread divergence. Thread divergence is essentially where threads perform different operations causing in-synchronization between threads which could effectively lead to unprecedented errors in the results or increase the execution time. We get thread divergence since implementing the pattern requires the use of if statements/for loop which creates conditional branches causing divergence.

```
__shared__ float partialSum[];
int t = threadIdx.x;
for(int stride = 1; stride < blockDim.x; stride *= 2)
{
    __syncthreads();
    if(t % (2*stride) == 0)
        partialSum[t] += partialSum[t+stride];
}</pre>
```

The code above taken from [7] demonstrates the implementation described in the question. We can clearly identify thread divergence here at lines 7 to 8. This is because thread indexes that meet the condition (condition which allows each consecutive pairs to be added together) diverges to execute the code, however for every other thread in a pair would remain in an idle state.

With our current implementation we get less thread divergence, since instead of every other thread in a pair being idle we have every half a block size remaining idle. [7] Upon research I found that all threads in a warp take the same path meaning that the threads are synchronous and does not require and sync barriers. Taking advantage of warps means that there are no thread divergence. Half of the threads within a warp will do the addition operation whilst the other half will skip the statement.

Part 3: Scan

Step 1 [15 marks]: Implementation of Hillis and Steele Scan which uses multiple block size in order to handle large input arrays.

```
#include <stdio.h>
 #include <cuda.h>
 #define ARRAY_SIZE 64
 #define BLOCK SIZE 32
    int global_index = threadIdx.x + blockIdx.x * blockDim.x;
    int local_index = threadIdx.x;
      if (local_index >= offset && global_index < ARRAY_SIZE) {</pre>
```

```
if (local_index < offset) {</pre>
      mem2[local_index] = mem[local_index];
      mem[local_index] = mem2[local_index];
int global_index = threadIdx.x + blockIdx.x * blockDim.x;
int local_index = threadIdx.x;
```

```
/* We finally write the value from shared memory back to global */
idata[global_index] = mem[local_index];

/** Jeclaring pointers,

** idata will contain the results of the first level scan after the first kernal processing

** idata at the end of the execution will contain the results of the final scan

** idata2 will contain the highest most element from each stride equal to block width */

float *idata, *idata2;

/* Begin recording */

cudaEvent_t start, stop;

cudaEventCreate(&start);

cudaEventCreate(&stop);

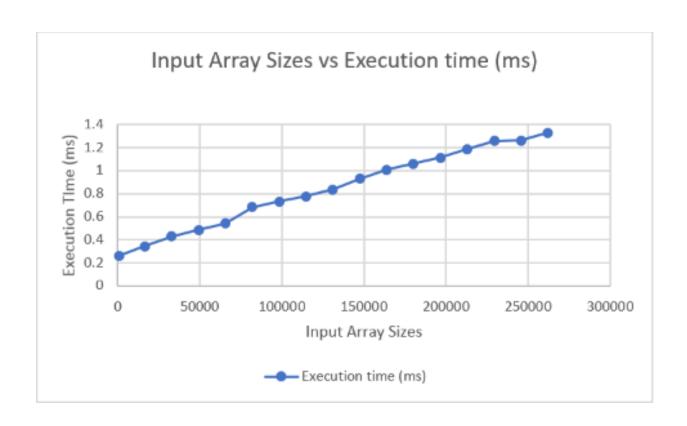
cudaEventCreate(&stop);

cudaEvent_t err;
```

```
cudaMallocManaged(&idata, ARRAY_SIZE*sizeof(float));
for (int i=0; i<grid_size-1; i++) {</pre>
final_scan_kernal<<<grid_size, BLOCK_SIZE>>>(idata, idata2);
cudaFree(idata2);
```

Step 2 [5 marks]: Execution times recorded as input array size increases.

Input Array Sizes	Execution time (ms)	
1024	0.263040	
16384	0.347072	
32768	0.432128	
49152	0.486400	
65536	0.542624	
81920	0.685440	
98304	0.734912	
114688	0.779008	
131072	0.837632	
147456	0.930336	
163840	1.007776	
180224	1.059840	
196608	1.113184	
212992	1.188672	
229376	1.259872	
245760	1.264320	
262144	1.328128	



Step 3 [5 marks]: Two propositions in improve performance of the current implementation.

One proposition in improving performance involves using CUDA's warp-level primitives. [4] Warps are a group of threads that perform a single instruction, in this case [3] we could perform a scan across a single warp of threads then scan across the blocks of threads and finally combine to get the final output. To implement this, we would remove the synchronous barrier since threads within a warp are all synchronous. We can 'unroll' the for loop so that only threads with index between 0 and 31 perform the scan function

Another proposition to improve the performance is to perform scan on different segments of the array. [5] By performing the scan on different parts of the array and then combining the solutions we increase the parallelism of the algorithm. This would be effective for a scan operation involving a large array input, instead of using one large scan we could simply perform many independent scan operations on different segments of the array. To mark where a segment begins we require another array (flag) with the same length as the input array and we add the value 1 to specify where a segment begins.

Two propositions to improve performance of Lab 5 Scan implementation

Using the material from the labs I learnt that the standard scan lab solution had a race condition which was solved using two buffers, one for reading and the other for writing. The race condition arises when a thread adds two elements together and updates its position however, just before it reads an element, another thread may have already updated it to a different value which will affect the scan result. The proposed solution requires two shared memory variables, one will be used to be read by a thread and the other will store the results of the operation after the read. After each iteration it's important that the two pairs switch functions so that we now read from the 'new' buffer and write to the 'old' buffer. This ensures the thread will never do an operation on an updated value. It's important to note that we must sync threads so that all the threads are working at the same pace, this also helps prevent any race conditions. (Note I have already implemented this in my solution for scan).

It's important that we use shared memory when implementing scan. As explained in part A, (quick summary See part A for the differences between shared and global memory) shared memory sits relatively close to threads in blocks compared to global memory. This physical advantage means that you get faster access times. However, as a price shared memory has much less storage and requires a change in thought process when coding since shared memory is only accessible by threads in a block. Essentially to implement shared memory, we assign each block's SRAM cell with a part of the input array such that each block will have access to different parts of an array. We also use another shared mem variable which will be used to load the second level scan output array (used for the map operation at the end) from global memory. After that we can do our map operation on the two arrays and finally moving the results from shared memory to global memory.

Part 4: Histogram

Step 1 [10 marks]: Implementation of Histogram using kernel from Lecture 11

```
#include <numeric>
#define ARRAY SIZE 64
  atomicAdd(&(d_bins[bin]), 1);
  const int BIN COUNT = 8;
  const size_t INPUT_SIZE = ARRAY_SIZE * sizeof(int);
  int h bins[BIN COUNT];
```

```
cudaMemcpy(d_in, h_in, INPUT_SIZE, cudaMemcpyHostToDevice);
cudaMalloc((void**) &d_bins, BIN_SIZE);
cudaEventRecord(start);
simple histogram<<<GRID SIZE, BLOCK SIZE>>>(d bins, d in, BIN COUNT);
cudaMemcpy(h_bins, d_bins, BIN_SIZE, cudaMemcpyDeviceToHost);
cudaFree(d in);
cudaFree(d_bins);
return 0;
```

Step 2 [10 marks]: Modified Implementation

```
#include <stdio.h>
#include <stdlib.h>
#include <cuda.h>
#define BLOCK SIZE 32
#define BIN COUNT 8
global void simple histogram(int *d bins, int *d in) {
  int global_index = threadIdx.x + blockDim.x * blockIdx.x;
   shared int local histogram[BIN COUNT];
      local_histogram[local_index] = 0;
    atomicAdd(&(local_histogram[bin]), 1);
  atomicAdd((int*)&d_bins[local_index], local_histogram[local_index]);
  int *d_bins , *d_in;
```

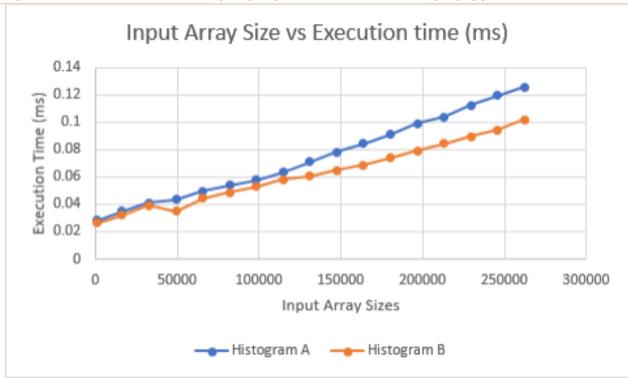
```
cudaMalloc((void**) &d in, INPUT SIZE);
cudaMemcpy(d_in, h_in, INPUT_SIZE, cudaMemcpyHostToDevice);
cudaMalloc((void**) &d_bins, BIN_SIZE);
simple_histogram<<<GRID_SIZE, BLOCK_SIZE>>>(d_bins, d_in);
cudaMemcpy(h_bins, d_bins, BIN_SIZE, cudaMemcpyDeviceToHost);
cudaEventRecord(stop);
printf("Elapsed time was: %f milliseconds \n", milliseconds);
```

```
/* Outputs the results */
for (int i = 0; i < BIN_COUNT; i++) {
    // Now output the resulting array:
    printf("Bin number: %d: Count: %d\n", i, h_bins[i]);
}

/* Frees the variables */
cudaFree(d_in);
cudaFree(d_bins);
return 0;
}</pre>
```

Step 3 [5 marks]: Differences between the two implementations

Input Array Sizes	Histogram A	Histogram B
1024	0.028544	0.026944
16384	0.035328	0.032448
32768	0.041336	0.039776
49152	0.044064	0.035104
65536	0.050240	0.044992
81920	0.054272	0.049312
98304	0.057920	0.053432
114688	0.063968	0.058496
131072	0.071584	0.061056
147456	0.078464	0.065256
163840	0.084544	0.069184
180224	0.091368	0.074364
196608	0.099520	0.079272
212992	0.104000	0.084656
229376	0.112576	0.089736
245760	0.119688	0.094552
262144	0.125728	0.102382



From the set of data, we can see that as the input array size increases the execution times increases. From the two implementations of histogram we can see that Histogram B out performed Histogram A for all input array sizes. This is because Histogram B uses shared memory. [2] Each block will hold their own set of as (local) histogram (a shared variable array with n number of bins) which will, in parallelism, increment the corresponding bin for a value which is retrieved using the current thread's index to access an element from global memory. After all the threads in each block have updated their local histogram the next step is to add up the local histograms. It is because every block has their own set of bins (implemented as shared memory) instead of having just one set of bins (implemented as

global memory) to increment, this makes histogram A not scalable since the atomics used limits the amount of parallelism. This limitation is overcome through incrementing local histograms and then finally adding the histograms together, since this introduces some parallelism since multiple histograms are incremented simultaneously. A suggestion to improve histogram B is to reduce the local histograms together instead of using atomic add, the use of atomics again will limit the amount of parallelism. Using a reduction method to add the local histogram would be ideal.

References:

- [1] "why shared memory is faster than global memory?", stackoverflow [Online], Available: https://stackoverflow.comq/uestions/28804760/why-shared-memory-is-faster-than-global-memory [Accessed: 28/04/19]:
- [2] "Implementing Histogram Using Local Memory", Udacity [Online], Available: https://www.youtube.com/watch?
 https://www.youtube.com/watch?
 https://www.youtube.com/watch?
 https://www.youtube.com/watch?
 v=B_lavYV8C94&list=PLGvfHSgImk4aweyWlhBXNF6XISY3um82_&index=156
 [Accessed: 23/04/19]:
- [3] "Efficient Parallel Scan Algorithms for GPUs", research.nvidia.com [Online], Available: https://research.nvidia.com/sites/default/files/publications/nvr-2008-003.pdf [Accessed: 25/04/19]:
- [4] "Warp-level Primitives", devblogs.nvidia.com [Online], Available: https://devblogs.nvidia.com/using-cuda-warp-level-primitives/ [Accessed: 25/04/19]:
- [5] "Segmented Scan", Udacity [Online], Available: https://www.youtube.com/watch? v=Yp2eDz6dvNA [Accessed: 25/04/19]:
- [6] Lecture 10, "Week4: Evaluating Parallel Algorithms", SurreyLearn [Online], Available: https://surreylearn.surrey.ac.uk/d2l/le/content/172335/Home [Accessed: 23/04/19]:
- [7] "Warps and Reduction Algorithms", Homepages [Online], Available: http://homepages.math.uic.edu/~jan/mcs572/mcs572notes/lec34.html [Accessed: 23/04/19]:
- [8] "Optimizing Parallel Reduction in CUDA", NVIDIA [Online], Available: https://developer.download.nvidia.com/assets/cuda/files/reduction.pdf [Accessed: 18/04/19]: