

Department of Physics and Astronomy
Ruprecht Karl University of Heidelberg

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Ludwig Hoibl
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Frequency-division dc-SQUID Multiplexing based on flux ramp modulation

This Master thesis has been carried out by Ludwig Hoibl
at the
Kirchhoff-Institute for Physics
under the supervision of
Prof. Dr. Sebastian Kempf

For the readout of cryogenic detectors superconducting quantum interference devices (SQUIDs) are often used since they offer an intrinsic compatibility with the detector operation temperature, a near quantum-limited noise performance and a large readout bandwidth. To avoid a linear scaling of the overall system complexity when reading out multi-channel detector arrays, several SQUID-based multiplexing techniques were developed in the past. However, their application is often challenging. Therefore, in this thesis an easy-to-use MHz frequency-division dc-SQUID multiplexing technique was advanced by designing and optimising the readout chain. Additionally, a FPGA-based readout electronics with a custom software package was put into operation. By applying test signals to each SQUID and reading out the multiplexer continuously with the readout electronics, an online flux ramp demodulation could be performed for the first time with effective sampling rates up to 1.2 MHz proving the functionality of the multiplexing system. A noise analysis and crosstalk measurement showed that the multiplexer design can be optimized further to achieve the best possible device performance. The online flux ramp demodulation with high effective sampling rates pave the way for high-statistic, multi-channel spectrum measurements and therefore allow for the first time the application of this multiplexing technique in real experiments.

Dc-SQUID-Frequenzmultiplexverfahren auf der Grundlage von Flussrampenmodulation

Für die Auslesung von kryogenen Detektoren werden häufig supraleitende Quanteninterferenzdetektoren (SQUIDs) verwendet, welche eine intrinsische Kompatibilität mit der Betriebstemperatur des Detektors, ein nahezu quantenlimitiertes Rauschverhalten und eine große Auslesebandbreite bieten. Um eine lineare Skalierung der Systemkomplexität bei der Auslese von mehrkanaligen Detektorarrays zu vermeiden, wurden in der Vergangenheit mehrere SQUID-basierte Multiplexverfahren entwickelt. Deren Anwendung ist jedoch oft sehr anspruchsvoll. Daher wurde in dieser Arbeit ein einfach anzuwendendes MHz-Frequenzmultiplexverfahren für dc-SQUIDS weiterentwickelt, indem eine neue Auslesekette in Betrieb genommen und optimiert wurde. Zusätzlich wurde eine FPGA-basierte Ausleseelektronik mit einem individuell entwickelten Softwarepaket in Betrieb genommen. Durch Anlegen von Testsignalen an jedes SQUID und kontinuierliches Auslesen des Multiplexers mit der Ausleseelektronik konnte erstmals eine Online-Flussrampen-Demodulation mit effektiven Abtastraten von bis zu 1.2 MHz durchgeführt werden, wodurch die Funktionalität des Multiplexverfahrens demonstriert wird. Eine Rauschanalyse und eine Messung des Übersprechens zeigten, dass das Multiplexer Design weiter optimiert werden kann, um die bestmögliche Leistungsfähigkeit zu erreichen. Die Online-Flussrampen-Demodulation mit hohen effektiven Abtastraten ebnet den Weg für mehrkanalige Spektrumsmessungen mit großer Statistik und ermöglicht damit erstmals die Anwendung dieser Multiplextechnik in Experimenten.

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1. Introduction

In recent years, the application of cryogenic detectors, such as transition edge sensors and magnetic micro calorimeters operating at millikelvin-temperatures has become routine in many laboratories [Ens05a]. This development was driven by their high energy resolution due to their low noise as well as their ability to be integrated to arrays of variable scale. These multi-pixel detector arrays are used in many research fields including astronomy [Mau18], nuclear and particle physics [Agn18] and material science [Har09].

The devices of choice for the readout of many of these detectors are superconducting quantum interference devices (SQUIDs) due to their intrinsic compatibility with millikelvin operation temperatures, near quantum-limited noise performance and large bandwidth. However, SQUIDs are intrinsically non-linear devices which shows up for example in the periodic flux-to-voltage characteristic of direct-current SQUIDs (dc-SQUIDs). Since for the readout of a detector a linear relation between the input and output signal of a dc-SQUID is desired, usually additional circuits are employed to linearize the dc-SQUID response. These circuits often implicate system constraints. For example, the dynamic range of a flux-locked loop (FLL) based dc-SQUID readout is limited by the finite voltage range and resolution of the digitizer. Additionally, the FLL circuit requires feedback wires routed from room temperature to each dc-SQUID and therefore to each detector. This increases the overall system complexity and leads to additional heatload on the experimental platform at millikelvin-temperatures.

For this reason, multiplexing techniques are often employed, that allow multiple SQUIDs to be read out in a single readout line. Ideally, these techniques offer a large dynamic range, a linear relation between the input and output signal, a readout bandwidth up to some MHz as well as low power dissipation on chip at cryogenic temperatures. A multitude of SQUID-based multiplexing techniques have been developed and are used today such as time-division multiplexing [Dor15], code-division multiplexing [Mor16], frequency-division multiplexing using GHz carriers [Mat08] and hybrid multiplexing approaches [Rei08, Yu20]. But despite the maturity of fabrication technology and the development of sophisticated readout electronics, the operation of these multiplexing techniques remains challenging and is associated with minor disadvantages. For example, existing time-division multiplexing (TDM) techniques typically readout arrays at the scale of 200 detectors using approximately 40 pairs of wires. However, the bandwidth of TDM is too low to acquire wideband signals without signal deterioration. Frequency division multiplexing using GHz carriers provides enough bandwidth per channel to resolve these issues, but an elaborated cryogenic microwave setup combined with complex readout electronics is required to read out hundreds and in future applications up to one thousand of detectors per coaxial cable [Mat17]. Moreover, existing MHz frequency-division multiplexers that

allow for the readout of up to 160 detectors, employ large on-chip passive filter circuits for each detector limiting the overall channel count per given chip area [dH12]. With the aim of reading out an array of some tens of cryogenic detectors with MHz signal bandwidth, an easy-to-use dc-SQUID based MHz frequency-division multiplexing technique was developed further within the scope of this thesis. This readout scheme relies on a series connection of current-sensing dc-SQUIDs. Each of them is equipped with an input coil for signal coupling and a modulation coil for flux biasing. The modulations coils are connected in series and coupled with different mutual inductances to each dc-SQUIDs. The readout is based on flux ramp modulation, a modulation technique typically used for linearizing the output signal of a microwave SQUID multiplexer [Mat12]. This multiplexing approach bridges the gap between demanding multiplexing methods and simple FLL based individual channel readout of medium-scale cryogenic detector arrays. Moreover, it allows for significantly increasing the dynamic range of a dc-SQUID system [Ric19]. To achieve a bandwidth of some MHz per readout channel signal digitisation with high sampling rates of some hundred MHz is required, generating huge data streams of up to a few GByte per second. Due to high data rates and the missing capability of online flux ramp demodulation, continuous readout of such a multiplexer has so far been limited to short periods of a few seconds. Furthermore, the experimental setup was not impedance-matched which limited the bandwidth per readout channel.

Within this thesis, these challenges were tackled and several improvements of the existing setup have been performed. To optimise the signal transmission, a new readout chain was built which consists of impedance-matched RF components including a new low-cost amplifier chain. In order to reduce the crosstalk between different channels, the mutual inductances between the modulation coils and the dc-SQUIDs were optimised. Furthermore, the wiring on chip was adapted to a optimised sample holder. To allow for a continuos readout of the multiplexer, a customized high-speed electronics based on a field programmable gate array (FPGA), analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) combined with a custom software package offering an online flux ramp demodulation was put into operation. The data processing modules were developed at the Institute for Data Processing and Electronics at the Karlsruhe Institute of Technology.

In chapter 2, the fundamentals of dc-SQUIDs, flux ramp modulation and the used multiplexing technique are discussed.

In chapter 3, the FPGA-based readout electronics is detailed including the hardware components and signal processing by the custom software package. Furthermore, the dc-SQUID and multiplexer design as well as the experimental setup are outlined. The obtained results from the characterisation of the investigated multiplexer chip and the testing of the experimental setup are presented and discussed in chapter 4. Finally, in chapter 5 a summary of the results of this thesis as well as an outlook on potential future work is given.

2. Theoretical background

The multiplexer investigated in this thesis is based on a series connection of direct-current Superconducting Quantum Interference Devices (dc-SQUIDs) and flux ramp modulation. Therefore, the first subsection of this chapter discusses the fundamentals of dc-SQUIDs, followed by an introduction to flux ramp modulation of dc-SQUIDs and in the last subsection the working principle of a flux ramp multiplexer is explained.

2.1 dc-SQUIDs

Superconducting Quantum Interference Devices (SQUIDs) are presently the most sensitive detectors for magnetic flux. In addition, all physical quantities that can be naturally converted into magnetic flux, such as electric current or voltage. Since flux ramp multiplexing is based on a series connection of dc-SQUIDs, their working principle is summarised in this section. An extensive description of SQUIDs can be found in [Cla04].

In Figure 2.1 a schematic diagram of a dc-SQUID is shown. It consists of a closed superconducting loop that is interrupted by two Josephson tunnel junctions, indicated by crosses. The junctions are placed such they form a parallel connection. To each of them a shunt resistor R is connected in parallel preventing hysteretic behaviour of the dc-SQUID. The Josephson tunnel junctions enable magnetic flux to enter or exit the SQUID loop. In application as a magnetic flux sensor the dc-SQUID is typically biased with a bias current I_b , while the voltage V across the dc-SQUID is measured. A magnetic flux change inside the superconducting loop leads to a voltage change across the dc-SQUID. Thus, a dc-SQUID is in essence a flux to voltage converter providing a flux dependent output voltage. One generally is able to detect an output

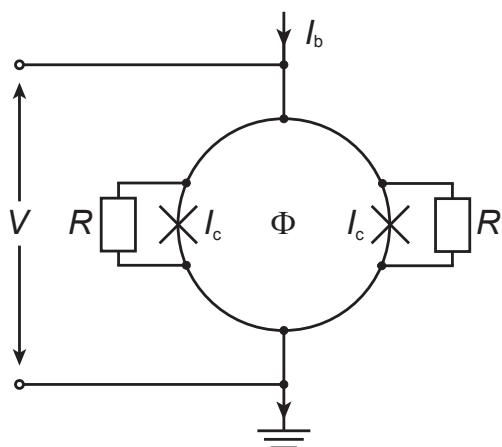


Figure 2.1: Schematic diagram of a dc-SQUID consisting of a closed superconducting loop that is interrupted by two Josephson tunnel junctions with critical current I_c . Each junction is represented by a cross. The shunt resistors R in parallel to each junction suppressing hysteretic behaviour of the dc-SQUID. Adapted from [Fer15]

signal corresponding to a flux change of much less than one magnetic flux quantum $\Phi_0 = 2.067 \times 10^{-15}$ Wb. However, the relation between a change of magnetic flux and output voltage is only linear for small changes of magnetic flux.

The dc-SQUID is based on two physical phenomena: The quantization of magnetic flux in closed superconducting loops [Dol61] and the Josephson effects [Jos62] in Josephson tunnel junctions. In the next section the characteristics of a Josephson tunnel junction biased by an external current source is briefly discussed, since it is a central element of a dc-SQUID. For simplicity, SQUID will be used to refer to a dc-SQUID from this point on.

2.1.1 Josephson tunnel junction

Josephson tunnel junctions are made up of two superconducting electrodes, which are separated by an insulating barrier with a thickness of only few angstrom. The SQUIDs used within the framework of this thesis are based on Josephson tunnel junctions made out of an Nb/Al–AlO_x/Nb trilayer, where the aluminium oxide represents the insulating barrier of the junctions. The thin barrier permits a weak coupling between the superconducting electrodes and therefore enables the coherent tunnelling of Cooper pairs through the barrier, which is called the Josephson effect [Jos62]. When an external current source is connected to the Josephson tunnel junction and a current I is applied, this current can be carried entirely by the Cooper pairs up to a characteristic critical current I_c of the junction. Thus, a supercurrent flows through the junction for $I < I_c$ and no voltage drop occurs across the junction. Increasing the external applied current to $I > I_c$ the Cooper pairs can no longer carry the entire current. The excess current is carried by quasiparticles, which can only tunnel resistively through the insulating barrier resulting in a voltage drop across the junction. For currents above the critical current, a Josephson tunnel junction exhibits an ohmic behaviour, which is called the voltage state of the junction. The characteristic resistance R_N of a junction in the voltage state, is the so called normal resistance. For simplicity, Josephson junction will be used to refer to a Josephson tunnel junction from this point on. The next section summarises the working principle of a SQUID.

2.1.2 Working principle

For the following discussion of the working principle of a SQUID, it is assumed that both Josephson junctions are identical and that the SQUID is biased with a constant current I_b . As long as no external magnetic field is applied to the SQUID loop with loop inductance L_s the supercurrent of the SQUID is given by $I_s = 2I_c$, since a current up to I_c can flow through each Josephson junction without a voltage drop. If, instead, a magnetic field is applied to the SQUID loop, also referred to as washer, the resulting flux Φ threading the washer will induce a screening current I_{cir} . Therefore, the magnetic flux threading the SQUID loop has two components: the

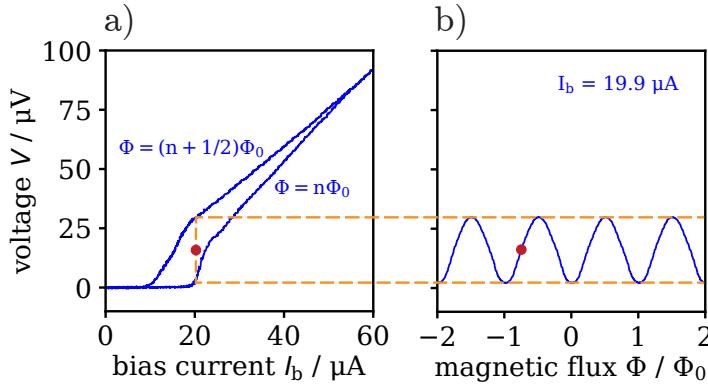


Figure 2.2: a) Exemplary current-voltage characteristics of a dc-SQUID shown for the two extrema of magnetic flux threading the SQUID loop $\Phi = (n + 1/2)\Phi_0$ and $\Phi = n\Phi_0$, where n is an integer. b) Periodic flux-voltage characteristic resulting from an applied bias current of $I_b = 19.9 \mu\text{A}$.

external magnetic flux Φ_{ext} and a self-induced magnetic flux $\Phi_L = L_s I_{\text{cir}}$ resulting from the screening current. If the self-induced magnetic flux exceeds $\pm\Phi_0/2$ the circulation direction of the screening current changes, because this is energetically more favourable than further increasing the screening current. Such, the total flux inside the loop is always kept equal to an integer number of Φ_0 and flux quantization [Dol61] within the SQUID loop is fulfilled. Due to the screening current, the critical of at least one Josephson junction of the SQUID is already reached at $I_b < I_s$. Hence, the supercurrent of the SQUID is reduced with applied magnetic flux. Furthermore, the supercurrent of the SQUID depends periodically on the magnetic flux through the SQUID with a period of Φ_0 , since the circulation direction of the screening current changes, if the induced magnetic flux would exceed $\pm\Phi_0/2$.

In practical applications SQUIDs are usually operated with a constant bias current of $I_b \gtrsim 2I_c$. This results in a quasiparticle current through the shunted Josephson junctions, leading to a finite voltage drop across the SQUID. This mode of operation is the so called voltage-state. In Figure 2.2 a) an exemplary current-voltage characteristic of a SQUID is plotted, illustrating the voltage response of a SQUID as a function of the applied bias current I_b . It can be seen that the voltage as a function of the applied bias current I_b is maximised for a flux of $\Phi = (n + 1/2)\Phi_0$ and minimized for a flux $\Phi = n\Phi_0$, where n is an integer. In Figure 2.2 b) the corresponding flux-voltage characteristic at constant bias current of $I_b = 19.9 \mu\text{A}$ is shown. It can be seen that the voltage across the SQUID depends periodically on the applied magnetic flux with a periodicity of exact one Φ_0 . The flux-voltage characteristic shows, that a SQUID in the voltage state acts as a non-linear flux-to-voltage converter.

The optimum performance of a SQUID is achieved when the working point with highest flux sensitivity is selected, which is indicated in figure 2.2 by the red dot. Sensitivities far better than Φ_0 are achievable. The optimal working point of the SQUID is determined by maximizing the peak-to-peak voltage of the flux-voltage characteristic and subsequently maximizing the flux-to-voltage transfer coefficient by choosing the appropriate current and flux bias for the SQUID. The flux-to-voltage transfer coefficient V_Φ can be determined from the flux-voltage characteristic and is

defined for a constant bias current of the SQUID as:

$$V_\Phi \equiv \left| \left(\frac{\partial V}{\partial \Phi_{\text{ext}}} \right)_{I_b=\text{const.}} \right| \quad (2.1)$$

If the SQUID is instead biased with a constant voltage V the output current will have a periodic dependency on the externally applied magnetic flux with the periodicity of Φ_0 [Che04]. For the operation with a voltage bias the flux-to-current transfer coefficient I_Φ can be determined from the flux-current-characteristic and is defined for a constant bias voltage as:

$$I_\Phi \equiv \left| \left(\frac{\partial I}{\partial \Phi_{\text{ext}}} \right)_{V_b=\text{const.}} \right| \quad (2.2)$$

Is the SQUID operated at the optimal working point, the periodic flux-voltage characteristic shows only a linear relation to additional applied magnetic flux $\delta\Phi$ for small signals of approximately $\delta\Phi \leq \pm\Phi_0/4$. Therefore, the so called open-loop readout offers only limited applications and a small dynamic range. To circumvent this limitation and linearize the SQUID output over a large range of magnetic flux typically a flux-locked-loop (FLL) circuit is used, which is described in the next section.

To induce a magnetic flux Φ_{in} inside a SQUID typically an input coil with inductance L_{in} is magnetically coupled to the SQUID. In this way the SQUID can be employed not only as magnetic flux sensor but also as highly sensitive current sensor. The input coil should be coupled as well as possible to the SQUID to minimize magnetic coupling losses. The coupling strength between the input coil and the SQUID loop with inductance L_s is given by the dimensionless coupling factor κ [Ens05b].

$$\kappa = \frac{M_{\text{in}}}{\sqrt{L_s L_{\text{in}}}} \quad (2.3)$$

Here $M_{\text{in}} = \Delta\Phi_{\text{in}}/\Delta I_{\text{in}}$ denotes the mutual inductance between the input coil and the SQUID, which describes the ratio between the flux change $\Delta\Phi_{\text{in}}$ induced in the SQUID by a current change ΔI_{in} in the input coil.

2.1.3 Flux locked loop

To increase the range in which the output voltage is changing linearly with the applied flux, while at the same time maintaining the sensitivity of the chosen working point, often a **Flux Locked Loop** (FLL) is used. A schematic circuit diagram of the FLL is shown in Figure 2.3. It consists of a differential amplifier, an integrator and a feedback loop, that connects the integrator output V_{out} via a feedback resistor R_{fb} to the feedback coil. The latter one has an inductance L_{fb} and is magnetically coupled to the SQUID via the mutual inductance M_{fb} . At the optimal working point of the SQUID, the bias current I_b is kept constant and the bias voltage at the amplifier V_b is

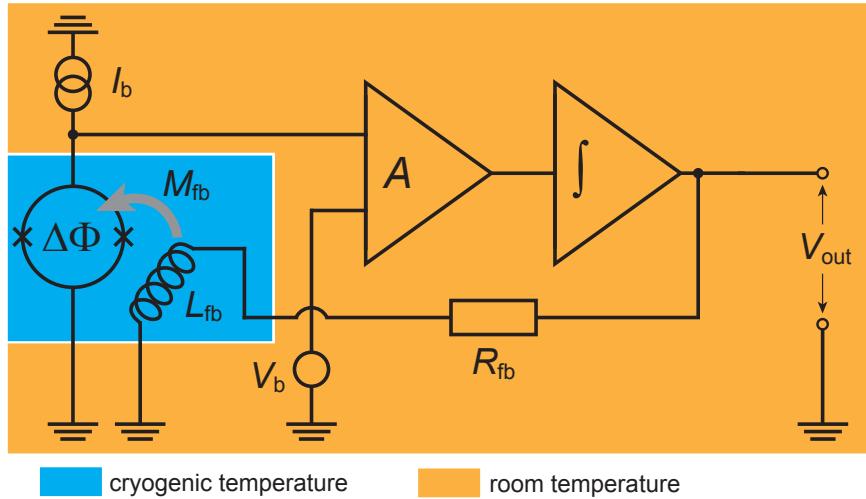


Figure 2.3: Schematic diagram of a SQUID that is read out using flux-locked loop circuit to linearize the output voltage of the SQUID. The output voltage is amplified, integrated, and transformed into a current via the feedback resistor R_{fb} . This current is running through a feedback coil that is coupled via the mutual inductance M_{fb} to the SQUID loop, in order to compensate the initial flux change $\Delta\Phi$.

chosen such the output voltage of the integrator vanishes. If the magnetic flux inside the SQUID changes by $\Delta\Phi$, the resulting voltage drop across the SQUID is amplified and integrated leading to an output voltage $V_{out} = -\Delta\Phi(R_{fb}/M_{fb})$ proportional to $\Delta\Phi$. The feedback resistor converts the output voltage into a current, that runs through the feedback coil. The latter one induces a magnetic flux in the SQUID, that compensates the initial flux change $\Delta\Phi$. Therefore, the flux inside the SQUID loop stays constant and the SQUID remains at the optimal working point with the highest sensitivity during application. Since amplifier and integrator are limited to a maximum output voltage, also the flux compensation is restricted to a finite value in the order of some tens to hundreds Φ_0 , depending on R_{fb} and M_{fb} . Accordingly, the SQUID readout with a FLL circuit has a much higher dynamic range compared to open-loop readout, however it is mainly limited by the used amplifier and integrator. The room temperature amplifier of the circuit introduces additional noise in form of voltage noise $\sqrt{S_{V,el}}$ and current noise $\sqrt{S_{I,el}}$ to the intrinsic flux noise of the SQUID $\sqrt{S_{\Phi,SQ}}$. The measured power spectral density of the apparent flux noise is given by:

$$S_\Phi = S_{\Phi,SQ} + \frac{S_{V,el}}{V_\Phi^2} + \frac{S_{I,el}}{I_\Phi^2} \quad (2.4)$$

Typically, at least one of the noise contributions from the amplifier is dominating over the intrinsic flux noise of the SQUID.

Within this thesis a low noise XXF-1 SQUID electronic of the company Magnicon

GmbH¹ was used to characterise SQUIDs. It contains all necessary current and voltage sources to operate a SQUID, including a FLL circuit. According to [Dru06] the intrinsic voltage noise and current noise of the amplifier of the SQUID electronics are $\sqrt{S_{V,\text{el}}} \approx 0.33 \text{ nV}/\sqrt{\text{Hz}}$ and $\sqrt{S_{I,\text{el}}} \approx 2.6 \text{ pA}/\sqrt{\text{Hz}}$ in the white noise regime above 1 kHz. Assuming transfer coefficients of $V_\Phi \approx 60 \mu\text{V}/\Phi_0$ and $I_\Phi \approx 20 \mu\text{A}/\Phi_0$ the contributions of the amplifier to the measured flux noise are $\sqrt{S_{\Phi,V}} \approx 5.5 \mu\Phi_0/\sqrt{\text{Hz}}$ and $\sqrt{S_{\Phi,I}} \approx 0.13 \mu\Phi_0/\sqrt{\text{Hz}}$. In total this is one order of magnitude higher than the white apparent flux noise of SQUIDs at millikelvin temperatures, that are developed in this group [Kem15].

2.2 Flux ramp modulation

Flux ramp modulation is a modulation technique typically used for linearizing the output signal of a microwave SQUID multiplexer [Mat11, Mat12]. Moreover, this method can be used to linearize the readout of a dc-SQUID [Ric19]. In contrast to the FLL, it is not necessary to bias the SQUID at a particular working point, for which reason the feedback loop is redundant.

In the modulation technique, a ramp that sweeps through multiple flux quanta with a constant rate is applied to the SQUID. Thus the sinusoidal flux-to-voltage SQUID characteristic discussed in section 2.1 is extended over multiple periods. In practice, the flux ramp cannot be infinite, therefore a periodic signal generating consecutively linear ramp segments with a fixed amplitude is used. Within this thesis a sawtooth shaped current with frequency f_{fr} and peak amplitude I_{mod} is applied to the modulation coil, magnetically coupled via the mutual inductance M_{mod} to the SQUID. Such, the flux $\Phi_{\text{mod}}(t) = M_{\text{mod}}I_{\text{mod}}(t)$ is induced in the SQUID loop. Given that the slew rate of the ramp greatly exceeds the one of an input signal applied to the input coil of the SQUID, the additional induced input flux Φ_{in} during a flux ramp window appears like a quasi constant flux offset to the SQUID. That leads to a phase shift $\Delta\varphi$ of the periodic SQUID characteristic, which is proportional to Φ_{in} and is calculated with:

$$\Delta\varphi = 2\pi \frac{\Phi_{\text{in}}}{\Phi_0} \quad (2.5)$$

In figure 2.4 a) two flux ramps with an amplitude of approximately $3\Phi_0$ are shown. The corresponding simulated sinusoidal SQUID characteristics are depicted below. The orange sawtooth is shifted by a small offset that leads to a phase shift of the SQUID response. By continuously measuring the sine shaped SQUID characteristic and tracking the phase, one measures Φ_{in} induced by the input coil. Since the phase shift $\Delta\varphi$ is a linear function of the applied magnetic flux, the SQUID readout is linearized with flux ramp modulation. In this regard the flux-to-voltage characteristic is the carrier frequency, whose phase will be modulated by an input signal.

In case the amplitude of the sawtooth shaped flux ramp does not correspond to an

¹Magnicon GmbH, Barkhausenweg 11, 22339 Hamburg, Germany

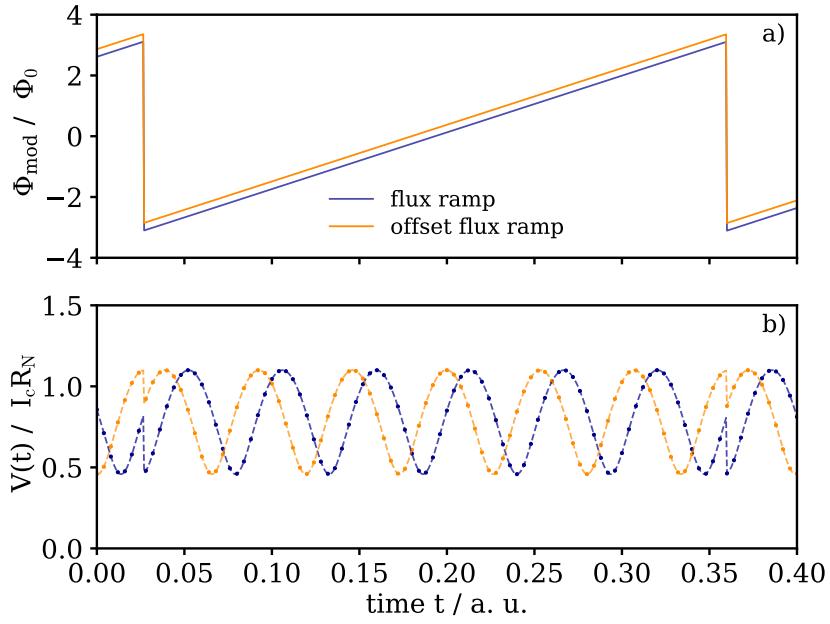


Figure 2.4: Illustration of the functional principle of flux ramp modulation. a) shows two arbitrary sawtooth shaped flux ramps. The flux ramp depicted in orange is shifted by a constant flux offset with respect to the blue one. b) illustrates an ideal SQUID response corresponding to the depicted flux ramps

integer number of flux quanta, transients are introduced at each ramp reset in the SQUID response, as depicted in figure 2.4 b). The transients arise because the flux state of the SQUID is different before and after the ramp reset. This prevents the simple stitching together of the individual ramp segments. Therefore, the carrier frequency phase is determined within windows of high linearity between two consecutive sharp ramp resets, where each window corresponds to one phase value. Thus, the input signal is sampled with the frequency f_{fr} . The amplitude of an input signal can be inferred by determining the phase shift of the SQUID characteristic with respect to the absence of an applied magnetic flux.

A disadvantage of this readout technique is the decrease in measurement bandwidth. Since the SQUID characteristic needs to be sampled properly in order to determine the phase accurately, the measurement bandwidth equal to $f_{\text{fr}}/2$ is several times smaller than the bandwidth offered by the sampling rate f_s of the SQUID response. As already discussed in section 2.1 the flux-to-voltage characteristic is periodic with Φ_0 , therefore the carrier frequency is determined by the derivative of the linear flux ramp divided by Φ_0 :

$$f_c = \frac{2f_{\text{fr}}\hat{\Phi}_{\text{mod}}}{\Phi_0} \quad (2.6)$$

With the peak amplitude of the flux ramp $\hat{\Phi}_{\text{mod}} = M_{\text{mod}} I_{\text{mod}}$. Assuming a flux ramp frequency of $f_{\text{fr}} = 250 \text{ kHz}$ with a peak current of $I_{\text{mod}} = 1 \text{ mA}$ and a mutual inductance of $1/M_{\text{mod}} = 40 \mu\text{A}/\Phi_0$, this results in a carrier frequency of $f_c = 12.5 \text{ MHz}$.

2.2.1 Phase determination

An essential part in the application of flux ramp modulation is the accurate determination of the carrier frequency phase, since the input signal of the SQUID is transduced to a phase shift of the carrier frequency. As explained, for each flux ramp segment one phase value is determined from the corresponding SQUID characteristic. A straight forward way to determine the phase is to perform a Fourier transform for each segment of the SQUID response and evaluate the Fourier coefficients at the corresponding carrier frequency. However, the readout electronics used within this thesis calculates the phase by digital demodulation of the time trace. This method uses fewer resources of the electronics per carrier frequency, which is beneficial in sight of the simultaneous phase determination of multiple carrier frequencies. The carrier frequencies used for the digital demodulation are determined with an algorithm based on a discrete Fourier transform. Both methods are summarised in the following section.

In practice the periodic SQUID response is digitized at a constant sampling frequency f_s , leading to a finite sequence of measurement values X containing N samples per flux ramp. The discrete Fourier transform (DFT) converts such a finite number of equally-spaced samples of a continuous signal into a discrete frequency spectra of the same length. The DFT assumes a periodic continuation of the dataset and transforms the sequences of real or complex numbers X into a sequence of complex numbers Z , defined by:

$$z_k = \sum_{n=0}^{N-1} x_n \exp\left(-i \frac{2\pi kn}{N}\right) \quad \text{with } k = 0, \dots, N-1 \quad (2.7)$$

Each complex output value z_k is called bin and has a corresponding width of f_s/N in the frequency domain. The amplitude A and the phase φ of each bin is calculated with:

$$A_k = \frac{1}{N} \sqrt{\operatorname{Re}(z_k)^2 + \operatorname{Im}(z_k)^2} \quad \text{and} \quad \varphi = \operatorname{atan2}(\operatorname{Im}(z_k), \operatorname{Re}(z_k)) \quad (2.8)$$

Assuming N is an even integer and x_0, \dots, x_{N-1} are real numbers, which is typically the case for samples of a continuous voltage signal, the DFT becomes even symmetric and is completely defined by the bins with the indices $k = 0, \dots, N/2$. They contain the positive frequency terms in rising order up to the maximum resolvable frequency $f_s/2$, according to the Nyquist-Shannon sampling theorem [Sha49]. To get the correct amplitudes of an even symmetric DFT, the value of each bin has to be doubled, since the indices $k = N/2, \dots, N-1$ are omitted:

$$A_{k,\text{cor}} = 2A_k \quad (2.9)$$

The definition of the DFT by equation 2.7 has a computational complexity of $\mathcal{O}(N^2)$, which can be reduced by a fast Fourier transform [Coo65] to $\mathcal{O}(N \log N)$, in order to accelerate the computation especially for large data sets. Therefore in practice a

discrete Fourier transform is often calculated with a fast Fourier transform (FFT) algorithm. The FFT algorithms are based on the DFT and assume as well a periodic continuation of the transformed dataset. In general, this is not necessarily the case, as the measured signal most likely does not correspond to an integer number of periods. These artificial discontinuities introduce frequency components, that are not present in the original signal, which smears out the resulting spectrum. This spreading effect across other frequency bins in the FFT is known as spectral leakage. To suppress any kind of discontinuities at the start and end of the sequence a common method is the weighting of the samples with a symmetric window function $w(n)$ before the transformation. Usually the window is bell-shaped with a maximum in the middle of the interval and tapering away from the extrema towards the boundaries. If a window function is applied to the discrete dataset, this will add a constant term to the phase [dG95], but does not affect the determination of phase shifts. Moreover, the amplitude of the spectrum has to be corrected if a window function is used by a factor of $1/\bar{w}$, where \bar{w} is the mean of the window function.

If carrier frequency ω_c already known, the phase can be determined after [Mat12] by digital demodulation. Given a finite number of samples x_t at times t of the continuous SQUID response, the phase φ of the fundamental frequency is calculated with:

$$\varphi = \arctan \left(\frac{\sum x_t \sin \omega_c t}{\sum x_t \cos \omega_c t} \right) \quad (2.10)$$

The digital demodulation mixes the signal time trace both up and down by $f_c = \omega_c/2\pi$. Any contribution to the sampled signal of the carrier frequency then results in a static, constant signal and a component with frequency $2f_c$. By taking the average of the demodulated signal the influence of the up-converted component is suppressed, while leaving the down-converted, static contribution unchanged. If an integer number of periods of the time trace is demodulated the influence of the up-converted signal vanishes completely. From the static component the phase can be derived using trigonometry.

This method is computational wise fairly simple compared to an FFT algorithm. Furthermore, no knowledge of the precise shape of the flux-to-voltage SQUID characteristic is required. As the FFT, it benefits from a set of samples consisting of an integer number of periods. Accordingly, it is desired that the flux ramp sweeps through a integer number of flux quanta. The digital demodulation method has the disadvantage of discarding information in higher harmonics of a non purely sinusoidal signal. Moreover, it is assumed that the dominant noise at the carrier frequency is added after the SQUID.

2.2.2 Noise degradation

The measured flux noise for flux ramp modulation is enhanced compared to FLL or open-loop readout of a SQUID. In case the data within the flux ramp windows

need to be cut to a fraction α of the whole window, the measured flux noise using flux ramp modulation will increase by a factor of $1/\sqrt{\alpha}$. Furthermore, the flux-to-voltage characteristic of the SQUID has to be measured continuously during the ramp to calculate the carrier frequency phase. This leads to an effective transfer coefficient $\sqrt{\langle V_\Phi^2 \rangle}$, which is lower compared to FFL or open-loop readout, because measurements occur at points of the SQUID characteristic, where it is less sensitive to magnetic flux.

Given a ideal sinusoidal SQUID response function with flux-independent noise, the signal-to-noise ratio is proportional to the slope of the SQUID response and adds for independent measurements in quadrature. The degradation factor after [Mat12] is calculated with:

$$\frac{1}{2\pi} \int_0^{2\pi} \left(\frac{d}{d\phi} \sin \phi \right)^2 d\phi = \frac{1}{2} \quad (2.11)$$

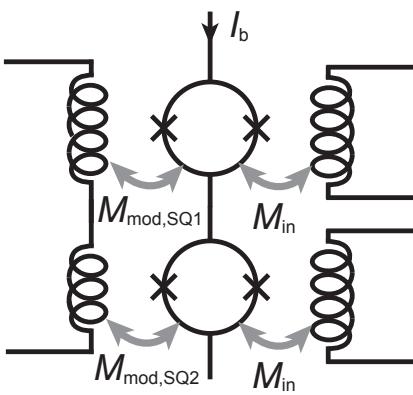
Therefore at least a increase in measured flux noise by a factor of $d = \sqrt{2/\alpha}$ using flux ramp modulation compared to FLL or open-loop readout is expected.

Flux ramp modulation suppresses noise added after the SQUID at frequencies well below the flux ramp repetition rate. This noise appears as a dc offset and does not affect the carrier frequency phase. Furthermore, with flux ramp modulation it is possible to simultaneously linearize the readout of multiple SQUIDs with a single flux ramp signal. Hence, this technique is well suited for the operation in a multiplexer as demonstrated by Mates in a microwave SQUID-multiplexer [Mat11] and Richter in a dc-SQUID multiplexer [Ric19].

2.3 Flux ramp multiplexing

Multiplexing techniques are used in communications technology to reduce the physical communication paths required for a signal transmission. For this purpose, the signals are first combined, then sent simultaneously via a shared medium and

Figure 2.5: Schematic illustration of two channel flux ramp multiplexer. The series connection of SQUIDs is biased with a constant current and each channel is equipped with an modulation coil and an input coil. The input coils are coupled with the same mutual inductance M_{in} to the SQUIDs, while the modulation coils are coupled with different coupling strengths $M_{mod,i}$. Adapted from [Ric17].



separated again at the receiver. Flux ramp multiplexing is based on the idea to use the sinusoidal flux-to-voltage characteristic of a SQUID as a unique carrier frequency, that is modulated with an input signal. If multiple of this carrier signals with clearly distinguishable frequencies are combined together, it is possible to transmit them simultaneously via a common medium, e.g. a coaxial cable. In this manner each input signal is send in a distinct frequency range. Such a method is called frequency-division multiplexing (FDM).

In figure 2.5 a schematic circuit diagram of a two-channel flux ramp multiplexer is shown. The individual SQUIDs are connected in series and biased simultaneously by a constant current source. The identical input coils are coupled via the mutual inductance M_{in} to the associated SQUID and are well separated from the modulation coil to prevent parasitic coupling between them. In contrast to the input coils, the modulation coils are coupled with different strengths $M_{\text{mod},i}$ to the SQUIDs and are connected in series.

Flux ramp multiplexing is based on flux ramp modulation of dc-SQUIDs, which was discussed in section 2.2. In application, a common flux ramp signal is applied to the series connection of the modulation coils. Due to the different coupling strengths of the modulation coils a different number of flux quanta per ramp is induced in each SQUID resulting in distinct carrier frequencies for each channel. Since all SQUIDs are connected in series, their output voltage adds up together as qualitatively depicted in figure 2.6. In this example the first channel is coupled stronger to the flux ramp compared to the second one, hence the carrier frequency associated to channel one is higher than the carrier frequency of channel two as shown in 2.6 b). The beat signal in figure 2.6 c) is the superposition of both carrier signals. As already discussed in section 2.2, an input signal with significant lower slew rate than the flux ramp leads to a phase shift of the associated carrier frequency. The voltage drop of the whole series connection is measured and by simultaneously monitoring the phase of each carrier signal the input signals of all SQUIDs can be inferred. In this manner, a flux ramp multiplexer can be read out

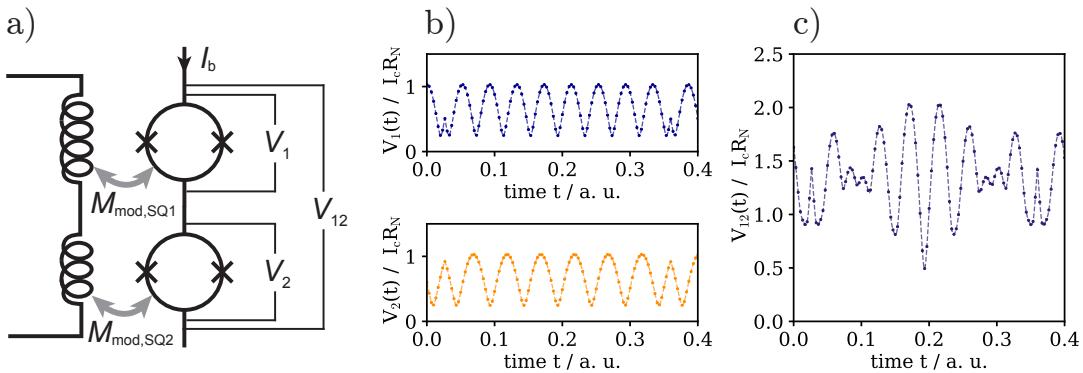


Figure 2.6: Schematic illustration of the functional principle of flux ramp multiplexer. In a) the circuit diagram with two SQUIDS is shown, whose simulated voltage response to a arbitrary flux ramp is depicted in b). Figure c) illustrates the resulting beat signal.

by using only two single readout lines routed from room-temperature to the SQUID column: One for the flux ramp and one for the voltage signal.

The apparent flux noise observed in a flux ramp multiplexer is, similar to FLL based readout, dominated by the contribution of the voltage amplifier connected to the SQUID column. Moreover, the degradation factor introduced by flux ramp modulation raises the noise level further. Compared to FLL readout a factor between two and three is expected [Ric17], depending on the fraction of the flux ramp used for the phase determination and the shape of the carrier signal.

2.3.1 Crosstalk

In transmission systems crosstalk refers to the undesired effect, by which a signal transmitted in a channel couples unfavourable into one or more other independent channels. In order to avoid reducing the achievable signal resolution, all types of crosstalk should be minimised. In the following, only one type of crosstalk that can occur during the operation of a flux-ramp multiplexer is discussed, since crosstalk was not investigated in more detail within the framework of this thesis.

If the carrier signal is sampled in a time window not exactly equal to an integer multiple of the signal period, this will cause the amplitude and phase information to be distributed over multiple bins of the discrete Fourier spectrum. This effect can provoke crosstalk if the carrier frequency are spaced to closely and the bins of independent channels overlap. Therefore the carrier frequencies should be equally spaced in the available bandwidth to minimize the probability of spectral leakage of neighbouring carrier frequencies.

In practice, the carrier signal is not perfectly sinusoidal, therefore alongside the base frequency also higher harmonics arise. To prevent that the carrier frequencies overlap with higher harmonics of other channels, their spacing should be chosen, such it is equidistant between all base frequencies and the first higher harmonic of the lowest carrier frequency.

As discussed before the sawtooth shaped flux ramp is applied simultaneously to all SQUIDs. Accordingly from equation 2.6 follows that the carrier frequency is proportional to the magnetic coupling of the modulation coil to the SQUIDs $f_c \propto M_{\text{mod}}$ and thereby also the carrier frequency spacing is determined by M_{mod} . To achieve equidistant frequency spacing of all carrier signals and their higher harmonics for an N channel flux ramp multiplexer the mutual inductances of the modulation coils need to spaced by M_{mod}^{\min}/N , where M_{mod}^{\min} corresponds to the channel with the lowest carrier frequency.

3. Experimental methods

The flux ramp multiplexing technique presented within this thesis requires current biasing the individual SQUIDs of the multiplexer, the generation of a flux ramp signal as well as the digitization of the multiplexer signal and subsequent demodulation of the carrier signals. The generation of the flux ramp signal, digitization and the demodulation are all realized by readout electronics based on a field-programmable gate array (FPGA). The necessary firmware modules are developed at the Institute for Data Processing and Electronics (IPE) at Karlsruhe Institute of Technology (KIT). Commercially available electronics provide the current bias and test signals that are applied to the input coils of the individual SQUIDs to demonstrate the functionality of the multiplexing technique. In the following section the hardware components of the readout electronics are presented and the signal processing as well as the methods for the data analysis are explained. Subsequently, the design of the flux ramp multiplexer and the used SQUID are outlined. Finally, the whole setup including the readout chain developed within this thesis is presented.

3.1 FPGA-based flux ramp demodulation

For the full readout of a flux ramp multiplexer it is necessary to generate a flux ramp signal and to demodulate the phase of the carrier of each multiplexer channel. We used a single digital processing unit to fulfil these two demands. The readout electronics is part of the custom-made software-defined radio (SDR) system [Kar20] developed at IPE at the KIT for the readout of a microwave SQUID multiplexer in the framework of the ECHo project [Gas17]. Due to similar requirements for the readout of a microwave SQUID multiplexer and a flux ramp multiplexer concerning the digital processing unit, it is possible to share the readout electronics in both projects, however with individual firmware configurations. A detailed description of the firmware modules for the flux ramp generation and the data processing developed at IPE is found in [Wol20]. The readout electronics (compare figure 3.1) is based on a multiprocessor system on a chip (MPSoC) including a field-programmable gate array (FPGA) embedded on an evaluation board. The FPGA generates the flux ramp signal, which is converted into a voltage signal by a digital-to-analog converter (DAC) module. The carrier frequency bandwidth of a flux ramp multiplexer is typically in the range of several tens of megahertz, therefore the sampling rates of commercial high-speed analog-to-digital converter (ADC) evaluation modules are sufficient to digitize the voltage output of the multiplexer. Along the flux ramp signal generation, all essential processing steps, including the phase determination of each channel, are executed in a full custom signal processing chain in real-time by the FPGA. The real-time phase determination of each channel reduces the data

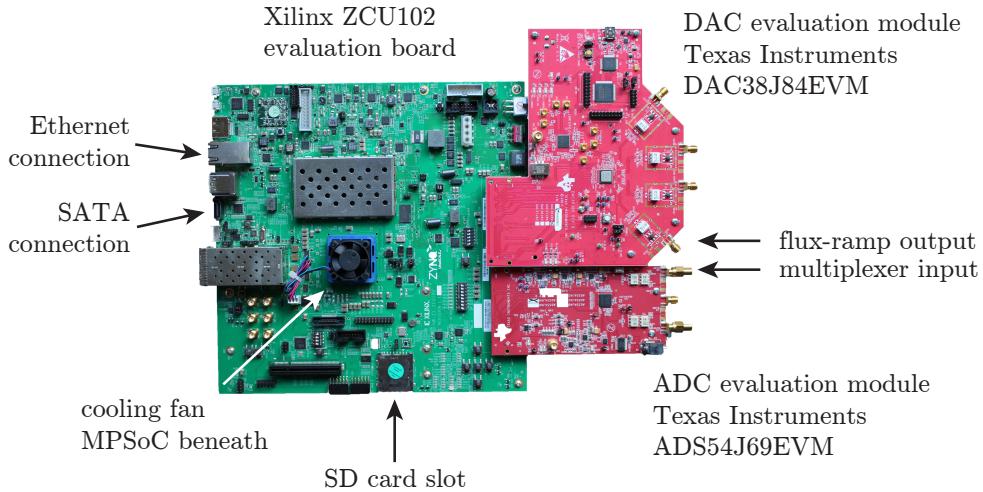


Figure 3.1: Photograph of the Xilinx ZCU102 evaluation board connected with DAC and ADC evaluation module. The multiprocessor system on a chip is located below the cooling fan in the middle of the board.

rate about two orders of magnitude to an amount that can be processed by a storage backend. For the first time, we are thus able to read out a flux ramp multiplexer continuously, whereby the measurement duration is only limited by the available storage space. Moreover, the customised firmware will enable the implementation of application-specific data analysis functions in the future, such as a pulse trigger. In the following all essential hardware components as well as the important data processing steps are discussed.

3.1.1 Hardware components

In figure 3.1 the digital processing unit is shown. It consists of the Xilinx ZCU102 evaluation board connected to a DAC evaluation module and an ADC evaluation module. The evaluation board is equipped with several interfaces including an Ethernet port and a SATA port to allow for a network connection and fast data transfer to a storage device. The custom firmware modules provided by IPE are imported via a SD card interface. The readout electronics is based on a multiprocessor system on a chip (MPSoC) that combines a powerful quad-core ARM Cortex-A53 along with a dual-core Cortex-R5F real-time processor with a Xilinx Zynq UltraScale+ FPGA. The latter performs all signal processing steps and the generation of the flux ramp signal shape simultaneously. The ARM Cortex-A53 performs slow control such as calibration procedures and data transmission to the storage backend. Additionally a Linux system runs on the ARM Cortex-A53 of the evaluation board to allow for remote control via Ethernet. The Cortex-R5F is not used by the implemented firmware. The DAC and ADC evaluation modules are each connected via a FPGA Mezzanine Card (FMC) interface to the MPSoC of the Xilinx ZCU102.

The flux ramp voltage signal is generated on the DAC evaluation module DAC38J84EVM from Texas Instruments¹ depicted in figure 3.1 and can be monitored on the installed SMA connectors. The DAC38J84EVM combines the digital-to-analog converter DAC38J84 from Texas Instruments with onboard clocking and further components required for operation. It offers 16 bit resolution with a sample rate of 2.5 GHz on each of the four ac-coupled output channels. Within this thesis it is operated at 500 MHz, which is sufficient for the generation of a sawtooth-shaped flux ramp in the megahertz range. The flux ramp signal is generated by the superposition of sinusoidal signals with amplitudes and frequencies, given by the Fourier series of the sawtooth-shaped waveform. The contribution of the n th frequency component of this Fourier series is decreased by a factor of $1/n$, where n is an integer. Therefore, the flux ramp shape is still well resolved with a cutoff frequency of the Fourier series of 500 MHz. The differential current signal generated by the DAC38J84 is transformed into a voltage signal by two transformers on the evaluation board. The factory transformers on the module are primarily designed for frequencies in the range of some hundred megahertz, whereas frequencies below 10 MHz are attenuated. However, flux ramp multiplexing requires repetition rates in the range of one megahertz. Therefore, the transformers JTX-2-10TA+ and MABA-007159 have been replaced by two ADTT1-6+ with a frequency range of 15 kHz to 100 MHz. The available voltage range at the analog outputs is $0.5 \text{ V}_{\text{pp}}$.

The multiplexer output voltage is sampled by one channel of the ADC evaluation module ADS54J69EVM from Texas Instruments depicted in figure 3.1. It combines the analog-to-digital converter ADS54J69 with onboard clocking and further components required for operation. A voltage singal can be applied via SMA connections. The ADS54J69 supports sampling frequencies up to 500 MHz with 16 bit resolution on its ac-coupled inputs. The full input scale of the ADC is $1.9 \text{ V}_{\text{pp}}$ peak-to-peak. Both onboard clocks of the DAC and ADC evaluation module are synchronised by a 10 MHz reference signal from a Rubidium Frequency Standard.

3.1.2 Signal processing

Figure 3.2 illustrates the data stream from the generation of the flux ramp signal, the flux ramp multiplexer and the phase demodulation to the storage on a hard drive. Apart from ADC (ADS54J69) and DAC (DAC38J84), also the implemented modules for the data processing on the FPGA are shown. The signal generator module implemented on the FPGA is capable of generating arbitrary signal shapes, which are continuously output by the DAC evaluation module. The flux ramp multiplexer is operated with a repetition rate of the flux ramp in the frequency range of some hundred kilohertz to some megahertz. During operation in this frequency span the ac-coupled outputs distort the signal shape stored in the module by introducing a

¹Texas Instruments Incorporated, Dallas, Texas, U.S.

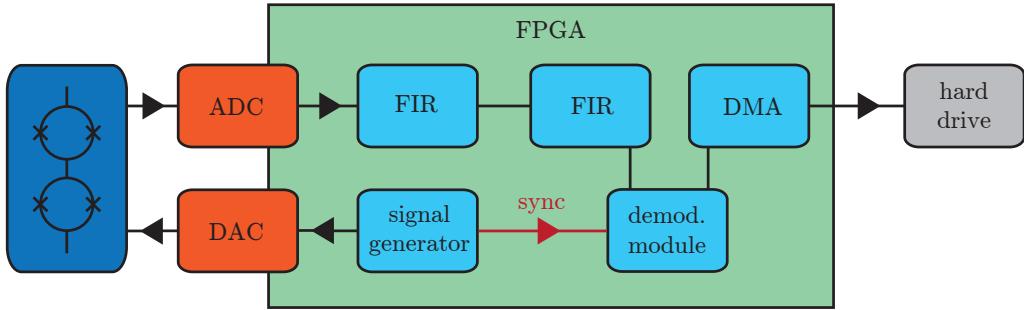


Figure 3.2: Schematic illustration of the data stream in the signal processing chain. Adapted from [Wol20].

phase shift to the low frequency components of the sawtooth waveform. Therefore, a sawtooth shape, corrected for deformation, is used, such that the output signal of the DAC evaluation module provides ramp segments of high linearity.

The ADC evaluation module samples the amplified voltage signal of the multiplexer in one channel with 500 megasamples per second (MSPS) and a resolution of 16 bit. The sampled data is streamed via the JESD204B transmission standard to the FPGA on the evaluation board, which executes the following implemented modules.

First, two finite impulse response (FIR) low pass filters decimate the sample rate each by a factor of 2, such that the Nyquist-Shannon sampling theorem [Sha49] is still fulfilled for the output signal. The downsampling is necessary because in the subsequent demodulation module all N_{ch} channels are processed in time multiplex, therefore only a fraction $1/N_{\text{ch}}$ of the FPGA clock rate of 500 MHz is available for each channel. The FIR filters are implemented as half band filters both of order 50 and attenuate frequencies in the upper half band above the Nyquist frequency. With a cut-off frequency f_{co} after the second filter, given by $f_{\text{co}} = 0.48f_s/4$, follows that the carrier signal bandwidth is limited to 60 MHz, where f_s denotes the sampling rate of ADC evaluation module. Outside the pass band frequencies are suppressed by about 40 dB.

The centrepiece of the digital processing unit is the demodulation module. It performs the phase determination for each multiplexer channel in the time frame of one flux ramp by digital demodulation. Thereby, the start of the data processing in the module need to be synchronized to the beginning of a ramp frame, to ensure only samples within the linear part contribute to the phase determination. Moreover, it is required that the phase determination is tuned to the flux ramp frequency. Thus, the window in which the data is demodulated does not shift with time in relation to the ramp. To allow for synchronization between the flux ramp and the data processing to determine the carrier phase, at the beginning of each ramp the signal generator sends a sync signal to the demodulation module. Due to the runtime in the signal path and the required time of the data processing before the demodulation unit, the sync signal has to be delayed in order to compensate for the introduced shift with respect to the flux ramp.

As depicted in figure 3.3, the demodulation module offers two modes: the demod-

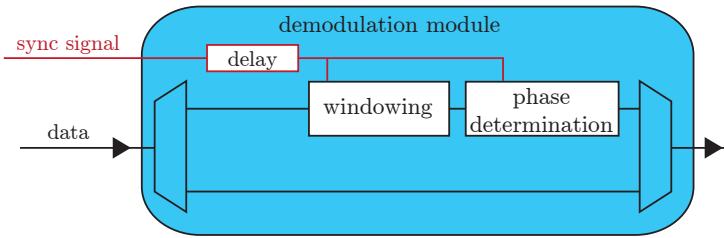


Figure 3.3: Schematic illustration of the demodulation module. Adapted from [Wol20].

ulation mode and the bypass mode. The first one consist out of two submodules: windowing and phase determination. In demodulation mode, once the sync signal from the signal generator is detected, the module starts with data processing of a flux ramp window of N samples. At first the window submodule weights the n th sample with the according factor $w(n)$ of the implemented Blackman window function given by

$$w(n) = a_0 - a_1 \cos\left(\frac{2\pi n}{N}\right) + a_2 \cos\left(\frac{4\pi n}{N}\right) \quad (3.1)$$

with the coefficients $a_0 = 0.42$, $a_1 = 0.5$ and $a_2 = 0.08$. Subsequently, as introduced in equation 2.10, for each channel the samples are multiplied with the sine and cosine of the corresponding carrier frequency and added up together, respectively. At the end of each ramp frame the phase is calculated from the two sums with an arctan-CORDIC [Vol59] algorithm for each given carrier frequency and passed to the next module.

If instead the bypass mode is selected, the filtered raw samples are passed on unchanged. This mode is required to determine the carrier frequencies of each multiplexer channel and the latency of the output signal of the multiplexer with respect to the ramp start. Finally, the direct memory access (DMA) module saves the determined phase values or raw samples with a high transfer rate on a SSD connected to the SATA-port.

The calibration of the evaluation board and control of the FPGA firmware modules is done via Ethernet. The modules are controlled by driver functions embedded in the firmware of the evaluation board and can be executed via the google Remote Procedure Call (gRPC) framework.

3.1.3 Data Analysis

As explained in 3.1.2 the demodulation module implemented on the evaluation board offers two operational modes: demodulation and bypass. In both of them the acquired data is stored in a single binary file after a measurement is completed. The data is not further analysed on the evaluation board. In the following the used methods for the analysis of the acquired data in the different operational modes are described.

If the demodulation mode is selected, a single phase value is determined for each ramp segment of the flux ramp. All phase values of one measurement are read in

from the binary file and converted to radian. Subsequently, the phase is renormalised into a magnetic flux in units of Φ_0 after equation 2.5. With the sampling rate, which is given by the flux ramp repetition rate, we can reconstruct the time trace of the SQUID signal. To perform a noise analysis of the reconstructed SQUID signal an estimator to the power spectral density (PSD) is calculated with a modified Welch's method [Wel67], which will be briefly introduced in the following. A dataset of N samples x_n , sampled with a constant sampling rate f_s , is split up into K smaller data segments with L samples each. The segments overlap with each other by $L - D$ samples. We obtained good results with an overlap of $D = L/2$ samples. For each segment the periodogram $P^k(f)$ with $k = 0, 1, \dots, K - 1$ is calculated according to

$$P^k(f) = \frac{2}{f_s \sum_{j=0}^{L-1} w_j^2} \left| \sum_{j=0}^{L-1} w_j x_{j+kD} e^{-2\pi f j / f_s} \right|^2 \quad (3.2)$$

where w_j are the weights of a window function. For the implementation in the data analysis framework we chose a Blackman-Harris window. The factor of 2 in front of the absolute square arises since we consider the single side band representation of the PSD. Finally, all K periodograms are averaged to get the estimator for the underlying PSD of the dataset.

We modified the basic principle of Welch's method by using multiple segment lengths L_i on the same dataset, to get an estimator with high fidelity that is also able to sufficiently resolve low frequencies. Since the calculation of a single periodogram is based on a discrete Fourier transform, a smaller segment size leads to a reduced frequency resolution of the periodogram. However, a greater number of segments is generated, and thus more periodograms are averaged. Therefore, the fidelity of the estimator is enhanced at the cost of a reduced frequency resolution. With a larger segment size, low frequencies are resolved better, even though with lower fidelity of the periodogram. By using multiple segment lengths L_i and combining the averaged periodograms of the distinct segment sizes in one estimator, we can obtain an estimator to the PSD with high fidelity at high frequencies and sufficient resolution to depict low frequencies.

If the bypass mode is selected, the digital filtered ADC samples are left unchanged by the demodulation module and stored to the hard drive. Initially all rawdata samples are imported by the data analysis framework as binary numbers. The first bit of each sample encodes the sync signal of the signal generator module. Hence, we are able to locate the beginning of each flux ramp in the rawdata time trace. After the position of all flux ramp windows is extracted, the rawdata samples are converted to decimal numbers and the time trace of the multiplexer signal is reconstructed with the sample rate after the FIR filters in the signal processing chain (compare figure 3.2). At this particular point in the signal processing chain the sample rate is given by the clock rate of the FPGA divided by the number of multiplexer channels $f_{\text{FPGA}}/N_{\text{ch}} = 125 \text{ MHz}$. Finally, a spectrum of the multiplexer signal is calculated with a common FFT algorithm to analyse the frequency components of the multi-

plexer signal including the carrier frequencies of the multiplexer channels.

3.2 SQUID and multiplexer design

The flux ramp multiplexer investigated in this thesis is microfabricated in the in-house cleanroom by using the fabrication process for dc-SQUIDs discussed in [Kem15]. In a photolithographic thin-film process the SQUID washer, the input and the modulation coil are sputter deposited from a niobium target. Figure 3.4 shows a

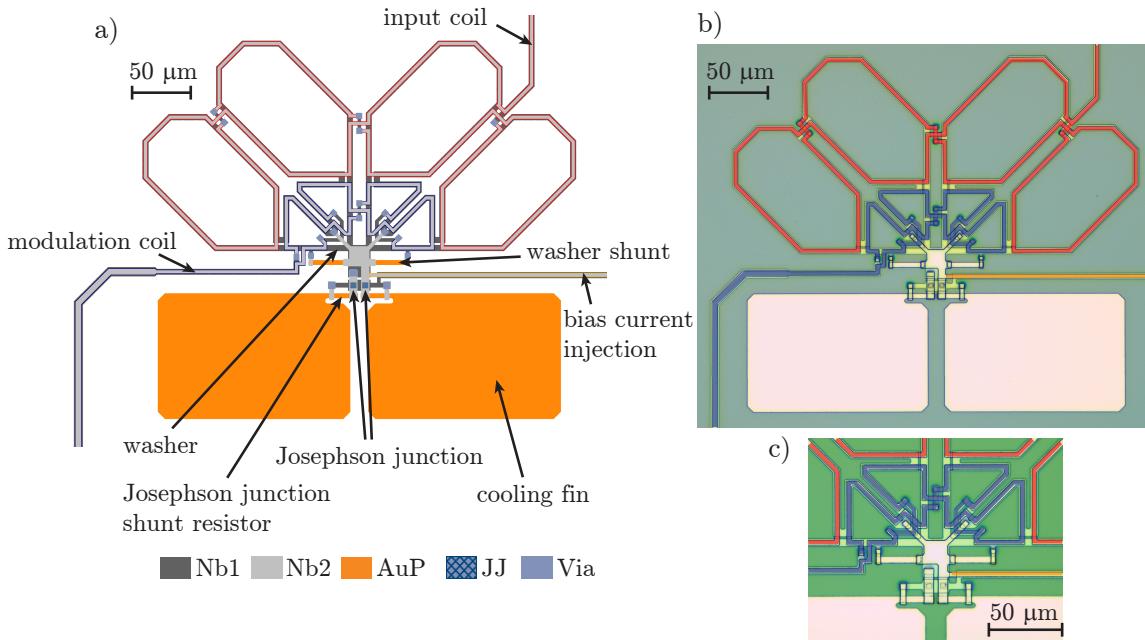


Figure 3.4: a) Design drawing and b) optical microscope picture of the SQUID equipped with a modulation coil optimally coupled to the SQUID loop. c) Magnification of the part of the SQUID loop to which the modulation coil is coupled. For clarity, the SQUID bias current injection, the modulation coil as well as the input coils are colored.

design drawing and image captured with a microscope of the SQUID which is used in the flux ramp multiplexer investigated within this thesis. To suppress parasitic magnetic signals the SQUID washer in the first Niobium layer (Nb1) is designed as parallel first-order gradiometer [Ket78, Zim71]. Four equally large washer loops with two positive and two negative orientations are connected in parallel such that the induced contributions of a homogeneous magnetic stray field cancel each other. The second Niobium layer (Nb2) is galvanically isolated from the first one by a thin insulation layer of SiO_2 . The input coil and modulation coil are placed on top of the SQUID washer to allow for a large mutual inductance. The orientation of both coils is chosen in a way that magnetic flux couples constructively into the SQUID and they run around separated washer holes, to minimize the parasitic mutual inductance between them. The on-chip wiring of the bias current injection, for input

and modulation coil are realized as striplines. This structure has the advantage that the parasitic inductances caused by the feed lines are minimised, as the area between the two conductors is very small. All Niobium lines are designed so narrow that they can still be produced reliably. This prevents flux vortices from being trapped in the wires when cooling below T_c in the earth's magnetic field [Sta04]. In the voltage state a finite current runs through the gold-palladium (AuPd) shunt resistors in parallel to the Josephson junctions, which leads to Joule heating. The dissipated energy has to be transmitted from the hot electrons to the phonon system of the normal conducting substrate to cool the SQUID. Therefore the shunt resistors are equipped with cooling fins to increase the effective contact area to the substrate and the effective electron-phonon interaction volume. Due to the weak electron-phonon interaction at millikelvin temperatures [Ens05c] typically, the electron temperature stays much higher than the corresponding phonon temperature, which is called the hot-electron-effect [Wel94, Fal08].

Moreover, the intrinsic capacitance C of the Josephson tunnel junction and the finite inductance L_s of the SQUID washer form an LC -circuit. The resonances that arise when the resonance condition is fulfilled can lead to a distortion of the flux-to-voltage characteristic of the SQUID resulting in a reduced transfer coefficient V_Φ and therefore a reduced energy sensitivity [Fog89]. In order to dampen the washer resonances a common method, also applied in the depicted design, is resistive damping, where a shunt resistor of gold-palladium (AuPd) is connected in parallel to the loop inductance of the SQUID [Fog89]. The schematic illustration of a dc-SQUID in figure 2.1 shows a symmetric bias current injection, meaning the inductance of both SQUID arms that connect the input feed line to the output feed line is the same. A drawback of this circuit design is fluctuations of the bias current leading to shifts of the working point and resulting in additional magnetic noise during SQUID readout. This effect can be suppressed by attaching the feedlines asymmetrical to the SQUID [Ueh93], as shown in figure 3.4.

As mentioned in section 2.3 equidistant carrier frequency spacing between the SQUIDs on the flux ramp multiplexer chip is important to reduce crosstalk and is determined by the spacing of the different mutual inductances M_{mod} between the modulation coils and the SQUIDs. In general the modulation coil is adapted to the SQUID design as depicted in figure 3.4 to optimize the coupling strength between washer and coil, resulting in a large mutual inductance for a certain SQUID geometry. The SQUID design presented does not allow the coil diameter to be increased further without adjusting the entire geometry. Therefore the mutual inductance is adjusted by reducing the diameter of the modulation coil. Thus, the inductance of the coil becomes lower and the coupling strength to the washer gets weaker, resulting in a reduced M_{mod} after equation 2.3. In figure 3.5 a microscope image of a SQUID with a modified modulation coil is shown. Most of the niobium line runs inside the washer hole. The numerical simulation software InductEx² was used to simulate the mutual inductance of the modified modulation coils. For

²<https://www0.sun.ac.za/ix/>, Stellenbosch University, South Africa

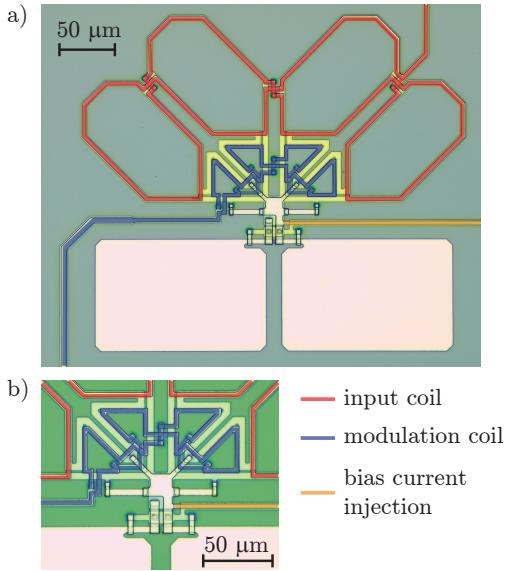


Figure 3.5: a) Optical microscope picture of a SQUID with a modified modulation coil. b) Magnification of the part of the SQUID loop to which the modulation coil is coupled. For clarity, the SQUID bias current injection, the modulation coil as well as the input coils are colored. Compared to the default layout in figure 3.4 the mutual inductance between modulation coil and SQUID is reduced.

each desired M_{mod} the diameter was adjusted and subsequently simulated until the deviation to the desired target value was less than one percent.

In figure 3.6 a microscope image of a full flux ramp multiplexer chip is shown. The flux ramp multiplexer investigated within this thesis consists of a series connection of four SQUIDs, located on a $3 \text{ mm} \times 3 \text{ mm}$ chip together with all required contact pads for characterization and operation. All modulation coils are connected in series to a common modulation line (blue). Via two contact pads $\pm F$ on top of the left side the flux ramp current signal is applied. The contact pads $\pm V$ at the bottom of the left side contact the series connection of the SQUIDs (orange) to measure the voltage drop and to apply the bias current. Moreover, additional voltage taps allow for an individual characterization of each SQUID and the readout of a single multiplexer channel. Each input coil of a SQUID is connected to the according triplet of contact pads (red) on the right side. Their position is matched to the contact pads of a detector chip developed in our group.

It has to be noted, that the presented chip and SQUID design are not fully optimized for the flux ramp multiplexing application. So far, the on-chip wiring is not adapted to the requirements for the transmission of high-frequency signals. Moreover, the SQUID impedance is not matched to the impedance of the transmission line and the flux-to-voltage transfer coefficient of the SQUID layout is not maximised. Therefore, we do not expect an ideal performance of the device.

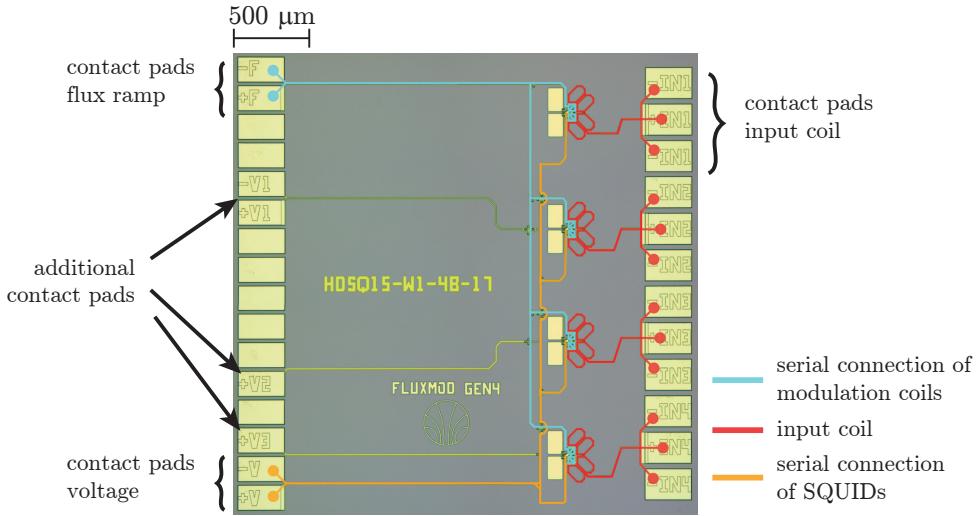


Figure 3.6: Optical microscope picture of the flux ramp multiplexer chip with the circuit design used within this thesis. For clarity, the serial connection of the SQUIDs (orange), the serial connection of the modulation coils (blue) as well as the input coils (red) of the individual channels are colored.

3.3 Experimental setup

A schematic of the experimental setup used for the flux ramp multiplexer readout is shown in figure 3.7. Cryogenic detectors are usually operated in a cryostat at millikelvin temperatures to improve the device performance and reduce thermal noise as much as possible. The superconducting electronics used to read out the detectors typically operate at the same temperature stage. However, the cool-down and warm-up procedures take a lot of time. Therefore, we cooled the devices under test by submersion in liquid helium, which is stored in a transport dewar. This much simpler method offers considerably faster cool-down and warm-up times and typically a constant device temperature of about 4.2 K is reached, well below the critical temperature of niobium $T_{C,Nb} = 9.2$ K.

The flux ramp multiplexer chip is glued onto a custom sample holder manufactured from copper together with a radio frequency (RF) circuit board and an ordinary printed circuit board (PCB) using GE 7031 varnish, shown schematically in figure 3.7. Electrical contact from the chip to the circuit boards is realised with aluminium bond wires. The PCB connects each of the three multiplexer channels with the weakest M_{mod} i.e. the channels two, three and four, to one twisted pair in order to introduce test signals to the multiplexer. The custom design RF circuit board has three coplanar waveguide (CPW) transmission lines with an impedance of 50Ω in order to minimize reflections due to an impedance discontinuity at the interface between the circuit board and the coaxial cable. The layout of the CPWs is adapted to the position of the contact pads on the multiplexer chip, to allow for short bonding wires. On the other end of the CPWs a SMA connector is attached to allow

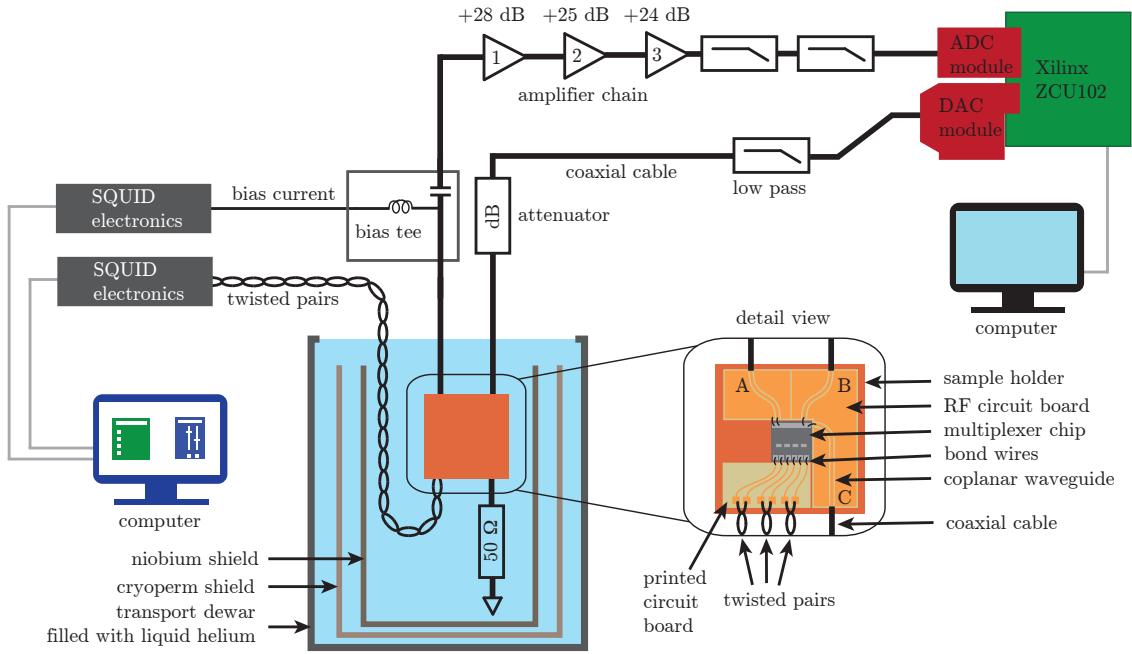


Figure 3.7: Schematic illustration of the experimental setup. The multiplexer chip is glued to a sample holder made from copper and submerged in liquid helium. A radio frequency (RF) circuit board and a printed circuit board (PCB) are used to contact the chip electrically via aluminium bond wires. The PCB connects the desired input coils to twisted pair wires, which are connected to a SQUID electronic to allow for the application of test signals. The RF circuit board connects the ADC and DAC module of the evaluation board to the multiplexer chip. The flux ramp transmission line is terminated by a 50Ω resistor.

for a connection with a coaxial cable. The CPW (A) taps the voltage drop across the SQUID column and is connected to the ADC module with the transmission line consisting of a bias tee, an amplifier chain and low-pass filters. The remaining two CPWs (B) and (C) carry the flux ramp signal. The CPW (B) is connected via an attenuator and a low-pass filter to the DAC module and applies the ramp signal to the modulation coils. The CPW (C) picks up the ramp signal from the chip and connects the flux ramp transmission path to a 50Ω terminating resistor to ground potential in order to suppress reflections of the flux ramp signal. For measurements, the sample holder is closed by a cover to protect the chip and the circuit boards from any mechanical contact. Additionally, it is surrounded by a magnetic soft cryoperm shield and a superconducting niobium shield minimizing the influence of external magnetic fields to the SQUIDs on the chip.

In the upper right corner of figure 3.7 the Xilinx ZCU102 evaluation board with ADC and DAC module, used for the full readout of a flux ramp multiplexer, is shown. The evaluation board with the attached modules is discussed in more detail in section 3.1. A low pass filter with a cutoff frequency of 165 MHz at the DAC output suppresses the coupling of high frequency noise from the DAC into the flux ramp transmission

line. Subsequently, an attenuator converts the sawtooth shaped voltage signal into a current signal that is applied to the chip via a coaxial cable connected to the RF circuit board which in turn contacts the multiplexer chip.

The carrier signals of the multiplexer chip are transmitted by the second room temperature coaxial cable. At the same time, a bias current is applied to the SQUID column with the bias tee ZX85-12G-S+ in the signal path. The voltage signal of the multiplexer is amplified by an amplifier chain consisting of a ZFL-500LN+, a ZFL-500+ and a SX60-43-S+. The bias tee and the amplifiers are manufactured by Mini-Circuits³. In table 3.1 the technical specifications of the amplifiers are summarized. The bandwidth of the amplifier chain has a frequency range from 0.50 MHz to

position	amplifier	gain at 20 MHz	noise figure	bandwidth
		[dB]	[dB]	[MHz]
1	ZFL-500LN+	28	2.9	0.10 – 500
2	ZFL-500+	25	4.2	0.05 – 500
3	SX60-43-S+	24	5.4	0.50 – 4000

Table 3.1: Overview of the technical specifications of the used amplifiers. The gain was measured at 20 MHz, but the values for noise figure and bandwidth were taken from the corresponding data sheets.

500 MHz and the total power gain of the amplifier chain is about 77 dB at 20 MHz, whereby the gain of each amplifier is slightly frequency dependent. Therefore also the total gain of the amplifier chain varies with the frequency. The voltage signal from the multiplexer with an amplitude of roughly $80 \mu\text{V}_{\text{pp}}$ is amplified by the amplifier chain to an amplitude of approximately $560 \text{ mV}_{\text{pp}}$. Hence, the signal range lies well inside the input range of the ADC. To use the full ADC input range the last amplifier in the chain has to offer at least the corresponding output power P_{full} . Usually an amplifier with an maximum output power larger than P_{full} is used to ensure that the amplifier does not go into compression close to the full ADC input range. Therefore, we chose a Mini-Circuits SX60-43-S+ even though it has a higher noise figure compared to the other amplifiers. The second amplifier in the cascade is a Mini-Circuits ZFL-500+. It offers suitable bandwidth and gain in combination with the other two amplifiers. The first amplifier in the cascade is a Mini-Circuits ZFL-500LN+. It offers suitable bandwidth, a large gain and a low noise figure (NF). The noise figure in decibel (dB) is defined as

$$\text{NF} = \log_{10} \left(\frac{\text{SNR}_i}{\text{SNR}_o} \right) \quad (3.3)$$

where SNR_i and SNR_o are the input and output signal-to-noise ratios in dB. The noise figure is a measure of degradation of the signal-to-noise ratio, with lower values indicating better performance. The total noise figure of the amplifier chain

³Mini-Circuits, New York City, United States

can be calculated with Friis formula [Fri44]. With the order of the amplifiers and the corresponding noise figures given in table 3.1 the total noise figure for the amplifier chain results in 2.91 dB, only slightly higher compared to the value given in the data sheet of the Mini-Circuits ZFL-500LN+. This simple calculation shows, that the second and third amplifier have only a minor impact on the total noise figure. Therefore, it is particularly important to choose an amplifier with a low noise figure as first amplifier in the chain. Finally, two low pass filters attached to the ADC module input suppress signals above the Nyquist frequency, preventing aliasing during signal sampling of the ADC. The first filter has a lower cutoff frequency of 93 MHz, but offers only a limited stop band. Therefore, a second filter with a lower cutoff frequency of 165 MHz and an upper cutoff frequency greater than 20 GHz is used to extend the stop band into the gigahertz range. The used SQUID electronics of the type XXF-1 from Magnicon GmbH have three channels. Each of the channels is equipped with a low noise, high precision current source and several current waveform generators. One SQUID electronics is used to bias the flux ramp multiplexer via the bias tee with a bias current. The second SQUID electronics is connected to the three twisted pairs to introduce test signals with the signal generators. Additionally, externally generated test signals can be applied to the multiplexer. The SQUID electronics is equipped with an input for voltage signals, which can be converted to a current signal via an internal resistor and put out on a single channel of the electronic. Both SQUID electronics are controlled by a computer.

4. Experimental results

In this chapter, we present the results obtained in the investigation of the flux ramp multiplexer chip 4C17 from wafer HDSQ15w1. First, the characterisation results of the chip are summarised. Subsequently, we demonstrate the readout of single multiplexer channel and analyse the carrier signal. We also classify the white noise level of the demodulated signal. Finally, we prove that the readout of a flux ramp multiplexer chip with the readout electronics works as intended and discuss the noise spectral density and the signal cross-talk.

4.1 Multiplexer characterisation

Each SQUID on the multiplexer chip is characterized individually by determining the characteristic quantities such as optimal bias current I_b , transfer coefficients V_Φ and I_Φ and mutual inductances M_{in} and M_{mod} . Thus we determine a suitable bias current for the whole SQUID column, are able to calculate the induced magnetic flux by a test signal applied to an input coil with a mutual inductance M_{in} to the SQUID and compare the measured mutual inductance M_{mod} to the simulated values. For the measurements the device is submerged in liquid helium stored in a transport can as already described in chapter 3, which results in a device temperature of 4.2 K. To characterise the individual SQUIDs of chip 4C17 from wafer HDSQ15w1, each of them was contacted via the corresponding additional voltage taps and connected to a XXF-1 SQUID electronics that provides the required FLL circuit and precision current sources. The readout electronics presented in chapter 3 is therefore not suitable for the characterisation. We determined the optimal bias current I_b , the transfer coefficients V_Φ and I_Φ , as well as the mutual inductance of the input coil M_{in} and the modulation coil M_{mod} . The transfer coefficients were measured at the positive slope of the SQUID characteristic, while the SQUID was operated in a flux locked loop, whereas the mutual inductances were quantified in open-loop operation. The results are summarized in table 4.1. In addition, the values for the mutual inductances $M_{\text{mod}}^{\text{sim}}$ simulated with InductEx, are shown for comparison.

As expected the optimal bias currents I_b and the transfer coefficients V_Φ and I_Φ are similar for all SQUIDs. The deviation from I_b of SQ1 compared to the other channels and the variation of V_Φ and I_Φ may arise from variations of the layer thicknesses and lateral variations of structures due to the limited precision of our fabrication process. The determined values for M_{in} vary by less than 1 % as the input coils of all SQUIDs have the identical design. However, they are 3 % to 4 % lower compared to the simulated values. The mutual inductances of the modulation coil M_{mod} agree well with the simulation and are spaced sufficiently equidistant. Except from SQUID four, the measured M_{mod} are 3 % to 5 % lower than the simulated values. The most

HDSQ15w1-4C17	I_b [μA]	V_Φ [μV/ Φ_0]	I_Φ [μA/ Φ_0]	M_{in} [pH]	M_{mod} [pH]	M_{mod}^{sim} [pH]
SQ1	10.7	62.2	12.4	232.6	49.7	51.3
SQ2	11.3	51.6	10.8	232.3	41.6	43.9
SQ3	11.1	57.8	13.2	231.1	35.5	36.6
SQ4	11.5	59.9	12.5	232.1	29.3	29.3

Table 4.1: Overview of the experimentally determined bias currents, transfer coefficients and mutual inductances of the input and modulation coil to the SQUID washer of the investigated multiplexer chip HDSQ15w1-4C17. Additionally the simulated values for mutual inductances of the modulation coil are shown.

likely reason for the differences of M_{mod} and M_{in} compared to the simulation are layer thickness variations of the insulating SiO₂-layer between the SQUID washer and the modulation coil, which have a high impact on the mutual inductances. Furthermore, deviations compared to the design drawing can occur due to fabrication tolerances and the limited resolution of the fabrication process. To adjust the mutual inductance, the diameter of the modulation coils is reduced, which leads to acute angles at the inner corners of the coil. These cannot be completely resolved, which rounds off the inner corners of the coil. Hence the fabricated diameter is smaller than expected, resulting in a reduced M_{mod} compared to the simulation based on the design drawing. However, for a detailed analysis of a systematic deviation not enough chips on wafer HDSQ15w1 have been characterized.

In order to classify the white noise level of the flux ramp multiplexing technique, a noise spectrum was obtained while SQ4 was operated at the optimal working point in a flux locked loop. With a Stanford Research Systems¹ SR770 FFT Network Analyser we measured the voltage noise spectrum at the output of the SQUID electronics and derived the equivalent magnetic flux noise

$$\sqrt{S_\Phi} = \frac{M_{fb}}{R_{fb}} \cdot \sqrt{S_V} \quad (4.1)$$

where $\sqrt{S_V}$ is the measured voltage noise, $R_{fb} = 10\text{ k}\Omega$ is the feedback resistance used in the FLL and $M_{fb}^{-1} = 70.27\text{ }\mu\text{A}/\Phi_0$ is the inverse mutual inductance of the feedback coil. As feedback coil we used the modulation coil of the corresponding SQUID. The measured spectrum is depicted in figure 4.3 and will be discussed in comparison to a noise spectrum obtained by flux ramp modulation readout of the same channel later in this chapter.

The results from the characterisation show that we can expect almost an equidistant carrier frequency spacing in the multiplexer application and we have to set the common bias current to around 11 μA. The SQUID electronics does not allow to set arbitrary values for the bias current, therefore we chose I_b slightly below the average

¹Stanford Research Systems, 1290-D Reamwood Ave., Sunnyvale, 94089 California, U.S.

to $10.8 \mu\text{A}$, which should not compromise the device performance.

4.2 Single channel readout

In this section, the experimental results for the readout of a single multiplexer channel with the bypass mode using the realtime flux-ramp demodulation of the readout electronics are presented. Finally, the white noise level of a flux ramp modulated noise measurement is compared to the white noise level obtained with flux lock loop readout of the same channel.

For the readout of a single SQUID of the multiplexer chip it is required to change the positions of the bonding wires that connect the coplanar waveguide to the voltage taps of the multiplexer chip, thus only the voltage drop across one SQUID is measured. The shortest connection from the CPW to the chip was achieved by contacting channel 4 of the multiplexer via the additional voltage taps. The data presented in the following were measured with a flux ramp amplitude of $0.5 \text{ V}_{\text{pp}}$ combined with an 13 dB attenuator in the flux ramp transmission line and the bias current was set to $10.8 \mu\text{A}$. The appropriate delay of the sync signal depends on the experimental setup and was set manually such that the start of a flux ramp coincides with the sync signal. The shape of the flux ramp was corrected and we chose a repetition rate of 500 kHz .

In figure 4.1 a) a section from the ADC raw sample time trace acquired with the bypass mode is shown and in figure 4.1 b) the corresponding amplitude spectrum is depicted. The SQUID electronic for the test signals was switched off during the measurement. The individual ramp segments are indicated by the red markers that represent the sync signal. The expected periodic carrier signal can be identified clearly. At the beginning of each ramp segment a transient response with high frequency ringing is visible. The voltage transients arise in case the magnetic flux threading the SQUID loop is different before and after the ramp reset. We found experimentally, that the amplitude of the transient ringing effect could be reduced by lowering the slope of the steep falling edge of the sawtooth shaped flux ramp generated by the signal generator module, by increasing the time period t_{re} for the reset to a finite value. With an empirically determined fall time of $t_{\text{re}} = 70 \text{ ns}$ the magnitude could be significantly decreased to the depicted level in figure 4.1. Moreover, a variation of the fall time showed, that the amplitude does seem to depend on the slope of the sharp reset of the flux ramp, but the ringing itself cannot be fully suppressed. Therefore, we decided to cut the first samples of each ramp segment when using the demodulation mode additional to the windowing. Compared to a sinusoidal signal, the measured SQUID characteristic is considerably deteriorated. At this stage of understanding, we believe this is caused by a non optimized device concerning the demands of the flux ramp modulation technique. Since the phase determination by digital demodulation benefit from a sine shaped carrier signal we expect a larger noise level of the demodulated signal.

The amplitude spectrum shown in figure 4.1 b) was calculated from the entirely de-

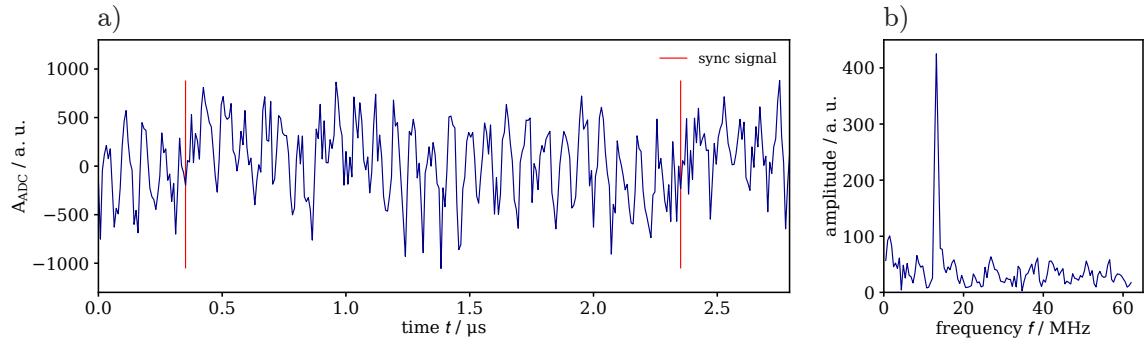


Figure 4.1: a) Section of ADC raw data time trace acquired during a single SQUID readout with the bypass mode. The sync signal is illustrated by the red markers and indicates the beginning of a new ramp segment. A ramp repetition rate of 500 kHz was chosen. b) Amplitude spectrum of the ADC raw data segment indicated by the two sync signals in the depicted time trace in a).

picted raw data segment of 250 samples in figure 4.1 a). Despite the deteriorated carrier signal the spectrum shows a clear peak at 13.2 MHz and a second one significantly weaker at about 26 MHz corresponding to the first harmonic of the carrier frequency. The frequency range of the spectrum is limited to 62.5 MHz because the sample rate after the FIR filters is reduced to 125 MHz. Despite the noisy carrier signal and only 250 raw data samples used for the Fourier transform it is very promising that the carrier frequency can be clearly identified, as the quality of the digital demodulation depends on how accurate the carrier frequency can be determined. To demonstrate the flux ramp modulated readout of a single SQUID with the FPGA based readout electronics we performed a continuos measurement with the demodulation mode, while a test signal was applied to the input coil of the SQUID. The carrier frequency used for the demodulation was set to 13.2 MHz. Due to the observed transient response at the beginning of each ramp segment the first 20 samples were omitted by the demodulation module. With the current wave form generator of the SQUID electronics we applied a sinusoidal test signal with a peak-to-peak amplitude of $I_{\text{pp}} = 2.0 \mu\text{A}$ and a frequency of 27.07 Hz to the input coil of the multiplexer channel 4. This corresponds to an amplitude of $A_{\text{pp,cal}} = I_{\text{pp}} \cdot M_{\text{in}} \approx 224.5 \text{ m}\Phi_0$ in units of the magnetic flux quantum. Figure 4.2 shows the derived magnetic flux from the demodulated phase, averaged over 20 neighbouring samples. The sine-shaped test signal is clearly recognisable. To the data points a fit of the function

$$\Phi_{\text{SQUID}} = \frac{A_{\text{pp}}}{2} \sin(2\pi f + \varphi) + c \quad (4.2)$$

was performed, where A_{pp} is the peak-to-peak amplitude, f denotes the frequency, φ an arbitrary phase offset and c an arbitrary amplitude offset. We find an amplitude of $226.5 \text{ m}\Phi_0$ and a frequency of 27.02 Hz. The amplitude differs only by about 0.9 % and the frequency only by about 0.2 % from the expected value. These fit results show, that we can reliably infer the input signal applied to the multiplexer channel

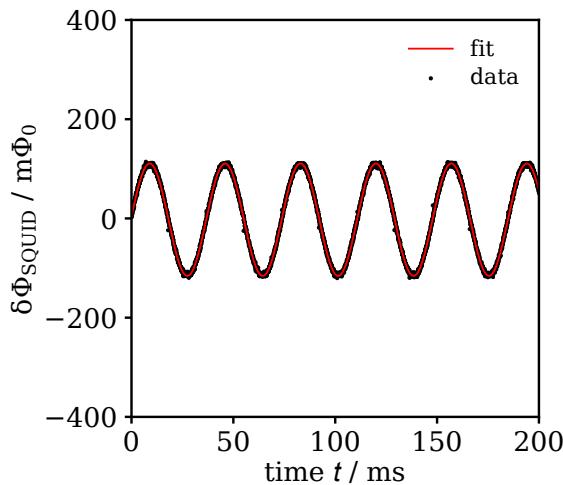


Figure 4.2: Magnetic flux $\delta\Phi_{\text{SQUID}}$ versus time t derived from phase samples acquired in single channel readout with the demodulation mode using a flux ramp repetition rate of 500 kHz. To the input coil of the corresponding SQUID a sinusoidal test signal was applied. The data points result from averaging over 20 neighbouring samples. Moreover, a sine function was fitted to the averaged data.

from the demodulated signal time trace of the demodulation module.

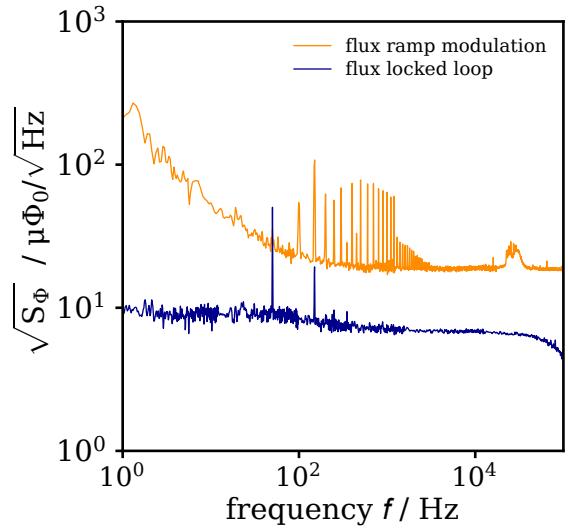
To classify the noise performance for a single SQUID readout with the demodulation mode of the readout electronics we compare the apparent flux noise in the white noise regime to the apparent white noise level of the same channel read out with a flux locked loop. For these noise measurements, no signal was applied to the corresponding input coil. From the whole time trace of a measurement with the demodulation mode the power spectral density is calculated with a modified Welch's method described in section 3.1.3. The FLL noise spectrum is derived from the voltage noise of the FLL output of the SQUID electronics as described in section 4.1. Both noise spectra are shown in figure 4.3.

The FLL noise spectrum was acquired during characterization of the multiplexer channel SQ4. It shows two prominent discrete noise peaks at 50 Hz and 150 Hz. Apart from this two plateaus ranging from 1 Hz to about 90 Hz and from about 600 Hz to 25 kHz are visible. The noise level start to drop above 25 kHz from about $6.8 \mu\Phi_0/\sqrt{\text{Hz}}$ down to $4.6 \mu\Phi_0/\sqrt{\text{Hz}}$ at 100 kHz.

Possible reasons for the noise peaks are, mains hum of 50 Hz, a ground loop in the experimental setup, or noise pickup by the unshielded twisted pairs that connect the SQUID electronics used for characterisation to the SQUID. We did not further investigate the origin of the discrete noise peaks, since we are mainly interested in the white noise level. With the used settings of the SQUID electronics, we calculated a 3 dB system bandwidth of 191 kHz, which explains well the observed decline of the noise level towards 100 kHz. The two noise plateaus in the spectrum are a consequence of the composite preamplifier concept used in the flux locked loop circuit of the SQUID electronics [Dru06]. The apparent flux noise in the plateau of high frequencies at 9 kHz is about $6.85 \mu\Phi_0/\sqrt{\text{Hz}}$.

Additional to the apparent flux noise spectrum acquired for FLL readout, the power spectral density obtained for flux ramp modulation readout with the evaluation board of the same channel is shown in figure 4.3. We chose a flux ramp repetition rate of 500 kHz. The power density spectrum shows a plateau with a white noise level at 9 kHz of $18.6 \mu\Phi_0/\sqrt{\text{Hz}}$, which run over into a $1/f$ -like increase in magnetic flux noise

Figure 4.3: Power density spectra of noise measurements performed in single channel readout of SQ4 with flux ramp modulation and a flux locked loop. For the readout with flux ramp modulation a ramp repetition rate of 500 kHz was chosen.



below about 500 Hz. Apart from a bell-shaped noise bump around 25 kHz several discrete noise peaks between 100 kHz and 3 kHz are clearly visible.

Up to now the source of the bell-shaped noise bump remains unclear. Possibly it is related to the same source as the discrete noise peaks between 100 kHz and 3 kHz. The origin of the noise peaks was intensively investigated and we could successfully reduce their amplitude by optimizing the experimental setup, but not fully suppress them. A more detailed discussion is given in section 4.3. The white noise level at 9 kHz is by a factor of 2.7 higher compared to FLL readout, which is slightly larger than reported factors between 2.1 and 2.6 in [Ric17]. Due to the noise penalty of the flux ramp modulation technique and a not fully optimized multiplexer chip, we expect an increase in apparent flux noise compared to the FLL readout assuming similar amplifier noise.

We can estimate the expected apparent flux noise for flux ramp modulated readout from the apparent flux noise measured in FLL readout with the degradation factor discussed in section 2.2. However we must take into account that the apparent flux noise is dominated by the amplifier noise of the SQUID electronics and that we did not use the same amplifier in both readout techniques. The amplifier noise contribution to the apparent flux noise is determined by the voltage noise and current noise of the amplifier, which is connected to the SQUID. According to [Che04] the contribution of the preamplifier current noise can be neglected because of the low dynamic resistance of the SQUID, given by $R_{\text{dyn}} = V_{\Phi}/I_{\Phi} = 4.8 \Omega$, therefore we will only consider the amplifier voltage noise in the following estimation. If we assume a FLL readout with a Mini-Circuit ZFL-500LN+, an increased apparent flux noise level is expected, due to the about 33 % higher voltage noise of the ZFL-500LN+ of $\sqrt{S_{V,\text{amp}}} \approx 0.44 \text{ nV}/\sqrt{\text{Hz}}$ compared to the SQUID electronics with $\sqrt{S_{V,\text{el}}} \approx 0.33 \text{ nV}/\sqrt{\text{Hz}}$, which would lead to an increased white noise level of about $8.4 \mu\Phi_0/\sqrt{\text{Hz}}$. For the comparison with the flux ramp modulation, we must additionally consider the degradation factor according to [Mat12]. We used 92 % of each flux

ramp window for the demodulation, since the first 20 samples of each segment of 250 samples were omitted due to the observed transients. This results in a degradation factor of at least $d_{\min} = 1.47$, which leads to a theoretical expected white noise level for the flux ramp modulation readout of at least $12.3 \mu\Phi_0/\sqrt{\text{Hz}}$ which is significantly lower than the observed level of $18.6 \mu\Phi_0/\sqrt{\text{Hz}}$. Most likely, the degradation factor is increased by the application of a window function to each ramp segment before the demodulation, but the exact contribution of the windowing remains unknown. At this stage of understanding, we believe the deviation can be also partly explained by the deteriorated carrier signal, which compromises the accuracy of the phase determination by digital demodulation. The lower bound of the degradation factor is only achieved if the carrier signal is purely sinusoidal. However, the obtained raw data time trace depicted in figure 4.1 shows a non-sine shaped carrier signal, hence the degradation factor will certainly be larger than d_{\min} . Taking into account the amplifier voltage noise of the ZFL-500LN+, compared to FLL readout the white noise level at 9 kHz is by a factor of 2.2 higher, which agrees well with the reported factors between 2.1 and 2.6 by [Ric17].

4.3 Multiplexer readout

This section discusses the experimental results obtained by reading out simultaneously all multiplexer channels with the readout electronics. With the bypass mode the final carrier frequency spacing is reviewed. In demodulation mode we demonstrated the full multiplexer readout and analysed the apparent flux noise in each channel. Additionally the crosstalk between different channels was measured.

The data presented in the following were measured with the experimental setup shown in section 3.3. As for the single channel readout we used a flux ramp amplitude of $0.5 \text{ V}_{\text{pp}}$ and an 13 dB attenuator in the flux ramp transmission line and the bias current of the SQUID column was set to $10.8 \mu\text{A}$. The delay of the sync signal remained unchanged and the flux ramp shape is corrected. We chose a fall time of $t_{\text{re}} = 70 \text{ ns}$ and used ramp repetition rates up to 1.2 MHz. In demodulation mode the first 20 samples of each ramp segment were omitted due to the observed transient ringing effect and the samples are weighted by the windowing submodule with the Blackman window function given in 3.1. Test signals have been applied via the SQUID electronics connected to the input coils of the multiplexer channels in two different ways: With the current waveform generator of each channel of the SQUID electronics three signals are applied simultaneously or an externally generated test signal is fed to the voltage input of the SQUID electronics and output on one of the channels.

We recorded a time trace of ADC raw samples with the bypass mode to analyse the raw sample time trace and calculated an amplitude spectrum to verify the carrier frequency spacing. We chose a ramp repetition rate of 500 kHz while no signal was applied to all input coils. In figure 4.4 a) a section from the raw data time trace is depicted and in 4.4 b) the corresponding amplitude spectrum of the shown ramp

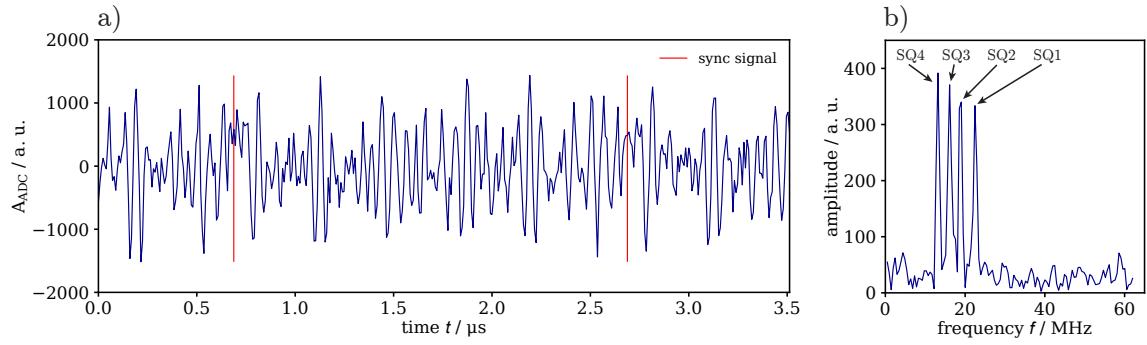


Figure 4.4: a) Section of ADC raw data time trace acquired in full multiplexer readout with the bypass mode. The sync signal is illustrated by the red markers and indicates the beginning of a new ramp segment. A ramp repetition rate of 500 kHz was chosen. b) Amplitude spectrum of the ADC raw data segment in the time trace indicated by the two sync signals.

segment is depicted. The start of the individual ramp segments is indicated by the red markers that represent the sync signal. As expected the the time trace shows a beat signal, which results from the superposition of the four carrier signals. Like the raw data time trace for single SQUID readout depicted in figure 4.1 a) also the beat signal shows a transient ringing effect after a reset of the sawtooth shaped flux ramp. With a fall time of the sawtooth reset of $t_{re} = 70$ ns the ringing could be significantly decreased to the depicted magnitude in figure 4.4. Nevertheless, we decided to cut the first samples of each ramp segment when using the demodulation mode additional to the windowing. The amplitude spectrum shown in figure 4.4 b) was calculated from the depicted raw data segment between the sync signals of 250 samples in figure 4.1 a). The amplitude spectrum shows four well separated distinct peaks corresponding to the four multiplexer channels. Fitting a Gaussian function to the peaks returned the following frequencies: 13.2 MHz, 16.1 MHz, 18.8 MHz and 22.6 MHz. The first harmonic of the carrier frequencies is only hardly visible. The frequency range of the spectrum is limited to 62.5 MHz because the sample rate after the FIR filters is reduced to 125 MHz. The carrier frequencies are spaced as expected from the spacing of the mutual inductances of the modulation coils shown in table 4.1. It is sufficiently uniform and the carrier frequencies are well separated to avoid leakage between neighbouring channels.

We performed a noise analysis of the signal time traces acquired in a simultaneous readout of the four flux ramp multiplexer channels with the demodulation mode of the readout electronics using the modified Welch's method described in section 3.1.3. No test signal was applied to the input coils during data acquisition with a flux ramp repetition rate of 500 kHz. The carrier frequencies were determined by a software module before the measurement, which calculates an amplitude spectrum from a raw data segment and fits a Gaussian function to the peaks corresponding to the multiplexer channels. The frequencies from the fits are used as carrier frequencies for the demodulation and set to 13.2 MHz, 16.1 MHz, 18.8 MHz and 22.6 MHz. In

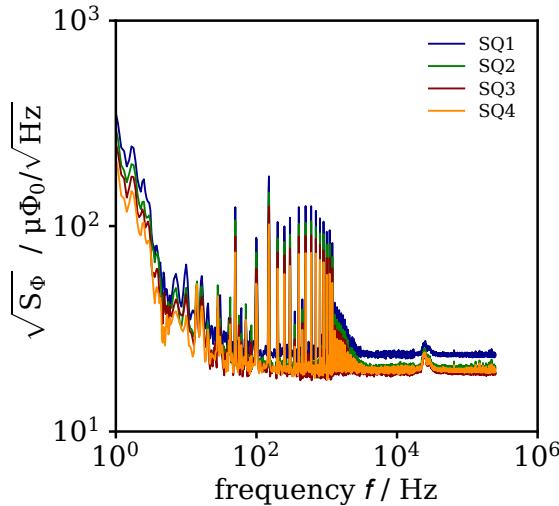
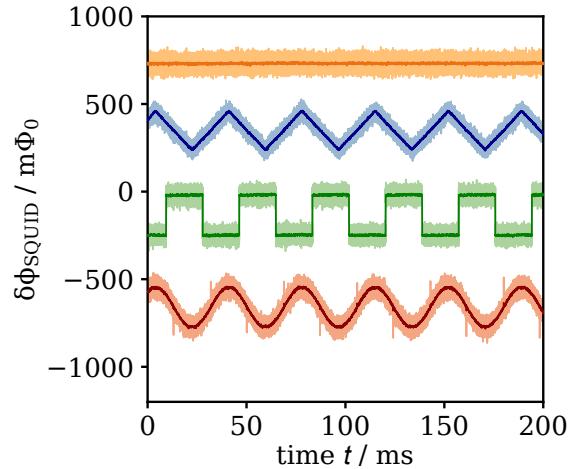


Figure 4.5: Power density spectrum of a noise measurement for full multiplexer readout in demodulation mode with a ramp repetition rate of 500 kHz.

figure 4.5 the power spectral density for each multiplexer channel is shown.

The white noise levels of the channels SQ1 to SQ4 are $23.6 \mu\Phi_0/\sqrt{\text{Hz}}$, $20.4 \mu\Phi_0/\sqrt{\text{Hz}}$, $19.4 \mu\Phi_0/\sqrt{\text{Hz}}$ and $19.8 \mu\Phi_0/\sqrt{\text{Hz}}$. Below about 100 Hz the white noise regime runs over into low frequency $1/f$ -like noise. Additionally, discrete noise peaks between 50 Hz and 1.3 kHz with a spacing of 50 Hz and an amplitude in the range of $100 \mu\Phi_0/\sqrt{\text{Hz}}$ can be seen. The peak amplitude drops at 1.3 kHz and gets progressively smaller until the white noise level is reached at about 3 kHz. As well as for single SQUID readout, a bell shaped noise bump at roughly 25 kHz is observed in all channels. Except for channel SQ1, the white noise levels are similar. The derived apparent flux noise in the white noise regime of the first channel is about 19 % higher than the average of the channels SQ2 to SQ4. The SQUID of channel SQ1 is located at the position of the SQUID column, which is connected to ground via bond wires that connect the voltage tap -V to the ground plane of the RF circuit board. The latter one is connected to the shielding of the coaxial cable to the amplifier chain. It remains unclear to which degree the direct ground connection of the SQUID does further deteriorate the SQUID characteristic, but could explain the increased white noise level. We observed, that at higher ramp repetition rates above 500 kHz the noise peaks in the $1/f$ -like regime below 100 Hz are getting stronger and the bell-shaped noise bump at 25 kHz rises and suspect that this might be due to the decreasing number of samples within a ramp segment for increasing ramp repetition rates, which compromises the accuracy of the digital demodulation. Several approaches to find the noise source of the discrete peaks between 50 Hz and 1.3 kHz were carried out and we could successfully lower their amplitude by optimizing the position of the attenuator as well as the low pass filters in the two transmission lines and by using a custom design RF circuit board adapted to the multiplexer chip layout, but we were not able to fully suppress them. One possible explanation for the noise peaks at multiples of 50 Hz could be a ground loop that runs through the DAC evaluation module and has not yet been eliminated. Alternatively, the noise source of the peaks could be noise pick up by the shielding of the transmission line, that

Figure 4.6: Magnetic flux $\delta\Phi_{\text{SQUID}}$ versus time t derived from phase samples acquired in full multiplexer readout with the demodulation mode, shifted by an arbitrary offset to increase visibility. To the input coils of SQ2, SQ3 and SQ4 a test signal was applied and sampled with a ramp repetition rate of 1.2 MHz. The solid lines result from averaging over 50 neighbouring samples.



couples into the SQUIDs. Further investigations of the noise source and optimisations of the experimental setup are planned for future experiments.

Comparing the power spectral density of channel SQ4 with the PSD for the single SQUID readout in figure 4.3, it is noticeable that the white noise level of channel SQ4 with $19.8 \mu\Phi_0/\sqrt{\text{Hz}}$ is slightly higher than the white noise level of $18.6 \mu\Phi_0/\sqrt{\text{Hz}}$ for single SQUID readout. Moreover, the amplitude of all discrete peaks in the spectrum is as well larger. Additionally, the PSD of channel SQ4 shows a prominent noise peak at 50 Hz and smaller ones in the $1/f$ -like regime. The increase in white noise and peak amplitude does seem to depend on the number of carrier signals that are simultaneously demodulated. For this it is necessary to superimpose the deteriorated carrier signals resulting in a distorted beat signal, which impact the accuracy of the digital demodulation. However, it is important to note, that the experimental setups were not identical, because the bonding wires in single SQUID readout have to contact the appropriate voltage taps to measure only the voltage drop across one SQUID. This may explain why an additional peak at 50 Hz is observed for the full multiplexer readout.

We demonstrate the flux ramp multiplexing technique with continuous online demodulation by applying different test signals to three of the four multiplexer channels. No signal was intentionally applied to the input coil of the first multiplexer channel in order to investigate possible cross-talk from other channels to the first multiplexer channel. The flux ramp repetition rate was set to 1.2 MHz, which is up to now the highest repetition rate used for the readout of a flux ramp multiplexer. The carrier frequencies were set to 31.8 MHz, 38.8 MHz, 45.3 MHz and 54.3 MHz. The triangle, square and sine shaped test signals with frequencies of 27 Hz and peak-to-peak amplitudes of $2 \mu\text{A}$, which correspond to approximately $222 \text{ m}\Phi_0$ for the given inverse mutual inductances of input coils were applied by a second SQUID electronic to the input coils of the multiplexer channels SQ2 to SQ4. In figure 4.6 the derived magnetic flux versus time is shown. The solid lines result from averaging over 50 neighbouring samples.

In all three channels a unique signal is visible. The amplitude and frequency are

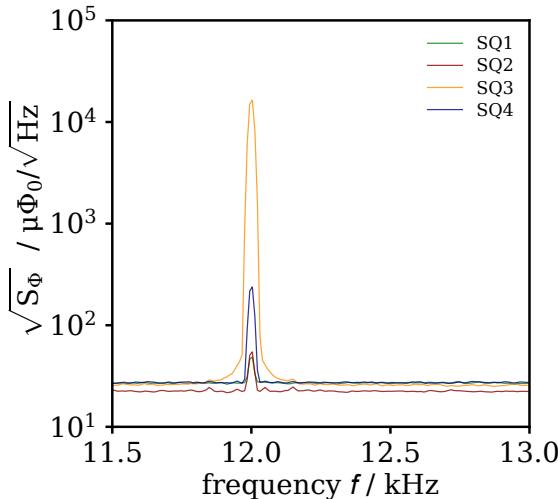


Figure 4.7: Section between 11.5 kHz and 13.0 kHz of the power density spectrum of a full multiplexer readout with the demodulation mode at a ramp repetition rate of 1.2 MHz. Only to the input coil of SQ3 a sinusoidal test signal with an amplitude of $I_{pp} \approx 4.2 \mu\text{A}$ and a frequency of 12 kHz was applied.

as expected and crosstalk between channels is not recognisable. The data points at the edges of the square signal are an artefact of the averaging over 50 samples. The input signals are clearly resolved, which proves that the read out of the flux ramp multiplexer with the readout electronics and implemented software package is performing as expected up to ramp repetition rates in the MHz regime.

We determined the cross-talk between channel SQ3 and the other channels of the multiplexer by only applying a sinusoidal test signal to the input coil of SQ3 and calculating the PSD of the measured time trace with the modified Welch's method described in section 3.1.3. All four channels of the multiplexer where read out with the demodulation mode at a flux ramp repetition rate of 1.2 MHz. With a Rohde & Schwarz² SMA100B signal generator we applied a sinusoidal voltage signal with an amplitude of about $V_{pp} \approx 42 \text{ mV}$ and a frequency of 12 kHz to the input for external signals of the SQUID electronics connected to the input coils. The voltage signal is converted to a current signal via an internal $10 \text{ k}\Omega$ resistor of the SQUID electronic resulting in a current amplitude of $I_{pp} \approx 4.2 \mu\text{A}$ and applied to the input coil of channel SQ3. With the inverse mutual inductance of the input coil of $8.95 \mu\text{A}/\Phi_0$, an amplitude of magnetic flux of $496 \text{ m}\Phi_0$ can be calculated.

In figure 4.7 a section between 11.5 kHz and 13.0 kHz of the calculated power spectral density of each multiplexer channel is shown. The white noise level in this frequency range is flat and has a magnitude of about $20 \mu\Phi_0/\sqrt{\text{Hz}}$. As expected the peak at the test signal frequency of 12 kHz is very prominent in channel three, but appears as well in the other channels. The cross-talk from channel SQ3 to SQ1 is -53 dB , to SQ2 is -50 dB and to SQ4 is -37 dB . The calculated cross-talk levels illustrate, that the cross-talk is higher to channels located next to channel SQ3 on the multiplexer chip, however it is significantly larger in channel SQ4 compared to channel SQ2. The latter one shows a similar level compared to channel SQ1. It remains unclear to which degree the observed magnitudes are attributed to on-chip crosstalk between neighbouring channels. Alternatively, it could simply mean that

²Rohde & Schwarz GmbH & Co KG, Mühldorfstrasse 15, 81671 Munich, Germany

the test signal couples into another twisted pair, since they run close together in the experimental setup. Nevertheless, the determined cross-talk for SQ1 and SQ2 shows, that a cross-talk level below -50 dB is achievable with flux ramp multiplexing. For the readout of a cryogenic detector array the admissible cross-talk is sensitive to the specifications of the application, such as the event rate, arrival statistics, ratio of signal to background events, and more, hence an overall classification of this result is difficult. However, the observed cross-talk is in the order of magnitude, which microwave SQUID multiplexers target [Weg18], which already fulfils the cross-talk requirements for many experiments.

5. Conclusion and outlook

In numerous experiments cryogenic detector arrays of various size are the basis for energy-dispersive measurements with an excellent energy resolution. For the readout of large cryogenic detector arrays, the application of multiplexing techniques is inevitable since the system complexity for single-channel readout scales linearly with the number of channels. However, many existing multiplexing techniques require demanding and expensive electronics, which make the operation of medium scale detector arrays excessively challenging. In view of this, our research group developed a new easy-to-use and low-cost multiplexing technique, which was taken a step towards application within the framework of this thesis.

A new readout system was built consisting of customised readout electronics and commercially available RF components including a low-cost amplifier chain.. The setup is complemented by a custom sample holder and RF printed circuit board which are both designed to match the multiplexer chip layout. For the first time, we read out a flux ramp multiplexer using a FPGA-based readout electronics. The latter consists of a Xilinx ZCU 102 evaluation board that is connected to an ADC and DAC evaluation module and is operated with a custom software package [Wol20] that was developed at the Institute for Data Processing and Electronics at Karlsruhe Institute of Technology. Apart from a current source to bias the serial connection of dc-SQUIDs, all necessary functions for the read out of a flux ramp multiplexer are included on the platform. This includes in particular the generation of the flux ramp signal, as well as digitisation and digital demodulation of the modulated multiplexer signal.

The readout of only one multiplexer channel was demonstrated by applying a sinusoidal test signal to the input coil of the channel. A fit of the appropriate waveform to the derived magnetic flux from the demodulated data returned an amplitude and frequency that differ by about 0.9 % and 0.2 % from the set values.

A spectral noise analysis for the single multiplexer channel showed several prominent discrete peaks and a rather high white noise level of $18.6 \mu\Phi_0/\sqrt{\text{Hz}}$ above 4 kHz. We estimated the factor by which the white noise level for flux ramp modulation readout is increased compared to flux locked loop readout to be 2.2, taking into account the different noise contributions of the used voltage amplifier for flux ramp modulated and FLL readout. This value agrees well with the reported factors between 2.1 and 2.6 in [Ric17], but is slightly higher than the expected degradation factor of 1.47.

An analysis of the carrier signal illustrated the signal's periodicity, but its sinusoidal shape is noticeably distorted. Furthermore, the ADC raw data showed a transient ringing effect after a flux ramp reset, which could be significantly reduced by limiting the slope of the sharp falling edge of the sawtooth shaped flux ramp.

As for single channel readout, the ADC raw data of the beat signal displayed a transient ringing effect after resets of the flux ramp. With a Fourier analysis of the raw

samples, the almost equidistant spacing of the carrier frequencies of the multiplexer was verified and is compatible with the determined mutual inductances of the modulation coils.

By simultaneous reading out all four multiplexer channels, while test signals were applied to the input coils of three channels, we showed that the experimental setup and software package is performing as intended. With the presented flux ramp multiplexer we are able to continuously run the multiplexer.

Similar to the single-channel readout the noise spectral density of a full multiplexer readout showed several prominent discrete peaks. By optimising the experimental setup we could lower this amplitude, but the noise source was not yet eliminated.

We determined a cross-talk level below -37 dB , by applying a sinusoidal test signal to the third channel while measuring the power at the frequency of the applied signal in all other channels and showed, that a cross-talk level below -50 dB is achievable with flux ramp multiplexing.

The chip design has not yet been finally optimised for flux ramp multiplexer applications. Therefore, we did not expect an ideal performance. The noise analysis of the demodulated signal in single channel readout and full multiplexer readout as well as the carrier signal analysis showed that there is still a lot of potential for optimisation. Nonetheless, we demonstrated that our flux ramp multiplexer combined with FPGA-based readout electronics including a custom software package performs as intended and allows for continuously reading out signal sources with MHz signal bandwidth at cryogenic temperatures.

For future applications such as the readout of a cryogenic detector we plan to optimize the overall setup. This comprises replacing the current DACs on the evaluation module to dc-coupled DACs, reducing the voltage noise of the used amplifier cascade, optimizing the on-chip wiring for transmitting high-frequency signals as well as matching the SQUID impedance to the line impedance and maximising the flux-to-voltage transfer coefficient. For future devices, we plan to build two-dimensional $M \times N$ multiplexers for which the N modulation coils within a row and the M SQUIDs within a column are serially connected to each other. The modulation coils within a row will be designed to have nearly identical mutual inductances. Between the M rows the mutual inductances are spaced equidistant as presented to avoid the overlap of carrier frequencies with their harmonics. With this scheme it is possible to suppress voltage transients in the carrier signals that arise when the magnetic flux threading the SQUID loop is different before and after the ramp reset simultaneously for all multiplexer channels. By injecting proper individual flux ramp signals to each row all SQUIDs are modulated with an integer number of flux quanta. Together with the large dynamic range [Ric19] that is comparable to state of the art flux-locked loop setups, the presented technique makes multiplexing accessible for various applications that require an easy-to-use and low cost setup, large signal bandwidth and dynamic range as well as low noise.

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Erklärung

Ich versichere, dass ich diese Arbeit selbständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe.

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(Ludwig Hoibl)

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